DESIGN OF 0.18-µm CMOS MIXER FOR MEDRADIO APPLICATION

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by

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LIST OF ABBREVIATIONS

ADE	Analog Design Environment
AC	Alternating Current
ADC	Analog-To-Digital Converter
CG	Conversion Gain
dB	Decibel
DC	Direct Current
DB	Double Balance
DAC	Digital-To-Analog Converter
GHz	Giga Hertz
HPF	High Pass Filter
IF	Intermediate Filter
IP1dB	Input 1dB Compression Point
IIIP3	Third Order Intercept Point
LO	Local Oscillator
LNA	Low Noise Amplifier
MHz	Mega Hertz
NF	Noise Figure

PA	Power Amplifier
RF	Radio Frequency
SB	Single-Balanced
SNR	Signal-to-Noise

LIST OF SYMBOLS

∞	Infinity
Ω	Ohm
f	Frequency (Hz)
C	Capacitance
F	Noise Factor
G_m	Transconductance of MOSFET
I_D	DC drain current
K_f	Stability factor
R	Resistance
S_{11}	Input Reflection Coefficient (dB)
S_{12}	Reverse Isolation (dB)
S_{21}	Power Gain (dB)
S_{22}	Output Reflection Coefficient (dB)
Z_{in}	Input Impedance
Z_L	Load Impedance
Z_0	Characteristic Impedance
Z_S	Source Impedance

Litar Pencampur Penukar untuk Penguat Penapis Perubatan

ABSTRAK

Tesis ini memperkenalkan komponen transceiver Frekuensi Radio yang dikenali sebagai litar pencampur penukar. Litar pencampur penukar adalah komponen kritikal dalam sistem RF, hasil daripada keupayaan untuk penukaran kekerapan. Petikan ini memberi tumpuan kepada analisis reka bentuk dan simulasi pencampur turun penukaran aktif. Litar pencampur penukar ini diterangkan oleh sifat reka bentuknya yang penting yang terdiri daripada penukaran, linier, angka bunyi, dan pengasingan pelabuhan. Topologi yang diberikan dalam liputan ini dari reka bentuk litar pencampur penukar yang paling biasa diketahui, kepada kaedah reka bentuk implimen yang digunakan untuk membina litar pencampur penukar sifat reka bentuk penting sebagai permintaan teknologi CMOS dan keseluruhan sistem RF meningkat. Topologi litar pencampur penukar telah direka dan disimulasikan menggunakan teknologi CMOS 0.18 μm CMOS dalam Sistem Reka Bentuk Lanjutan, satu sistem ujian yang digunakan terutamanya untuk reka bentuk RF. Reka bentuk ini boleh menghasilkan keuntungan penukaran kira-kira 12.86 dB dan 12.85 dB pada 401 MHz – 406 MHz. NF yang diperolehi dalam topologi ini adalah 11.2 dB pada 401.7 MHz dan mula jatuh di bawah 11.19 dB pada 405.8 MHz. IP1 db dan IIP3 juga dapat memenuhi target spesifikasi rekabentuk. Akhirnya, penggunaan kuasa adalah 6.17 mW pada 1.8 V.

Mixer for Medical Band Amplifier

ABSTRACT

This thesis introduces a component of the Radio Frequency transceiver called the mixer. The mixer is a critical component in the RF systems, as a result of its ability for frequency conversion. This passages focuses on the design analysis and simulation of active down-conversion mixer. This mixer is described by its important design properties which consist of conversion gain, linearity, noise figure, and port isolation. The topologies that are given in this passage range from the most commonly known mixer design, to implement the design methods that are utilized to build the mixer important design properties as the request of CMOS technology and the overall RF system rises. All mixer topologies were designed and simulated using TSMC 0.18 μm CMOS technology in Advanced Design Systems, a test system utilized particularly for RF designs. The design was able to produce the conversion gain about 12.86 dB and 12.85 dB at 401 MHz – 406 MHz respectively. The NF obtained in this topology was 11.2 dB at 401.7 MHz and started to go below 11.19 dB at 405.8 MHz. IP1db and IIP3 was also able to meet the design target specification. Finally, the power consumption is 6.17 Mw at a 1.8 V.

CHAPTER 1

INTRODUCTION

1.1 Research Background

The subject of Radio Frequency circuitry has been ending up more significance all throughout recent years. The topic of radio frequency (RF) communications has taken great steps from cell phones to base stations. All things considered the correspondence business has been upsetting the way the world transmits and gets data with developing interest. With this increase in demand the communication business has been inspired to extend and make more solid and proficient parts.

With a specific end goal to fulfill these objectives there should be an expansion in frequency range, programming, and hardware design. The nature of programming configuration has been steadily incline because of the increase of computing power. An increase in hardware and range can be reached by more complex component design. A case of this is shown via block diagram in Figure 1. This figure depicts simplified diagram of a base station transceiver.

This system consists of a receiver and a transmitter areas. In the receiver section the signal would enter into the antenna. The signal generally ends up noticeably powerless because of noise interference and attenuation at the antenna, and should be appropriately arranged to enter the system. This is reached by utilizing a Low-Noise-Amplifier (LNA). The LNA will amplify the signal while adding as little distortion as possible. At that point the signal is sent to the down conversion mixer and low pass filter (LPF) to be converted and tuned.

This change into a lower frequency is necessary for the signal to be converted for processers purposes. The analog signal is then converted to digital data via the analog- to-digital converter (ADC). Finally, the bits of data are used for processing purposes.

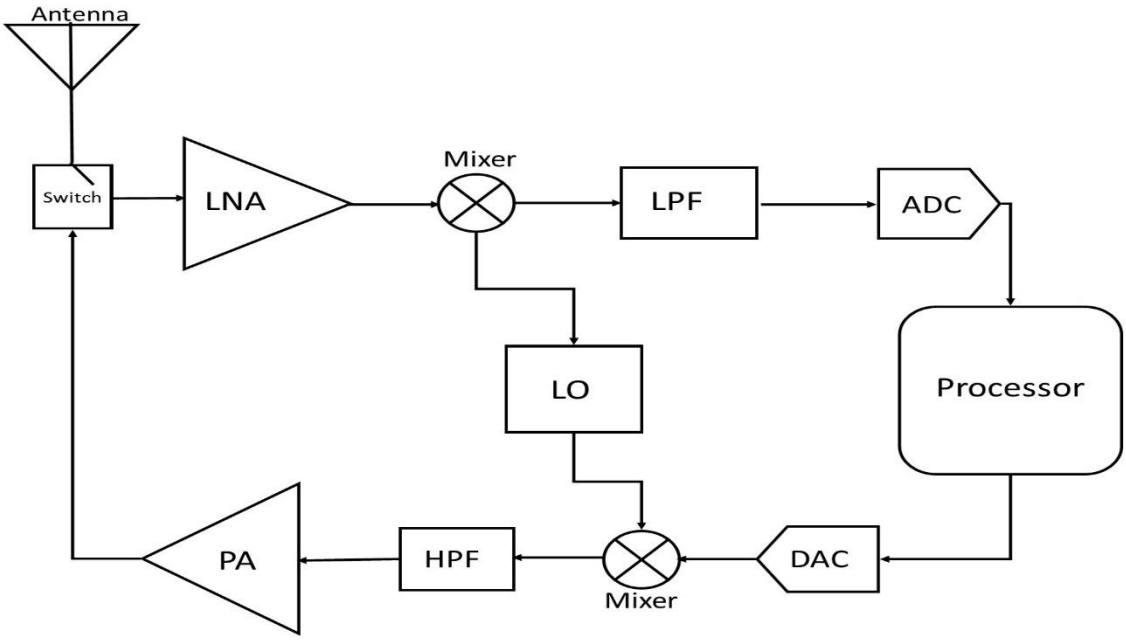

Figure 1: General RF Transceiver Diagram

In the transmission section the bits of information are converted from digital bits to an analog signal by the digital-to-analog converter (DAC). The signal is then sent to an up conversion mixer and high pass filter (HPF), which moves the original frequency to a higher frequency for communication. The new signal is then sent to a power amplifier (PA) to increase the power for the signal, and set up the signal for its distance travel. The signal is then transmitted through the antenna.

1.2 Problem Statements

With multiple mixer designs that can be used in practical applications in today's industry, a designer now has a broader choice of which topologies are better suited to meet system requirements. One of the most popular mixer designs is the Gilbert cell mixer. The reasons for its popularity are its balanced operation, and ability to allow a more clear output. The design gives a moderate gain and linearity at a low LO power while maintaining a low noise figure, and overall power consumption.

1.3 Objectives Research

In perspective of the issues previously mentioned, following objectives are set to clarify the issues. The objectives of this projects are:

- To design single-Balanced Gilbert Cell mixer for MedRadio Band in range 401MHz to 406MHz.
- To optimize the noise figure (NF) and low performances according to the design specification.
- To compare the data from the simulation to other designs specifications.

1.4 Scope of Research

The two signals inserted into the two input ports are normally the Local Oscillator signal, and the incoming (for a receiver) or outgoing (for a transmitter) signal. To deliver another Frequency (or new frequencies) a nonlinear device is required. RF Mixer is fundamentally a device, which is shifting a signal from one to another, keeping the properties of the initial signal (phase and amplitude), and therefore doing a linear operation. A LTI circuit cannot do frequency translation, consequently either a time varying parameter or a non-linearity is utilized. Along with the sum and difference of frequencies, it also produces harmonics of input frequency, LO frequency and their intermodulation products. The basic aim while designing mixer is to suppress these harmonics. The schematic design was conducted in Silterra's 0.18-micron CMOS Process Technology and simulated Cadence SpectreRF.

The power consumption to the entire circuit is preferably small. The schematic design is to be conducted in Silterra's 0.18-micron CMOS Process Technology and simulated using Cadence SpectreRF. This project will not cover until layout design and only concern up to pre-layout simulation due to time and cost. The performance of the proposed mixer will be compared with similar work by others.

1.5 Thesis Outline

This thesis begin with an introduction in Chapter 1. In this chapter, research background, problem statement. The objectives of research and thesis outline are described.

For the second chapter, it is mainly about the theories and equations that are related to the design of mixer. The explanation on performance metrics which include conversion gain, linearity, NF as well as reviews on similar work by others are available in this chapter.

Next, the design analysis are explain in chapter 3. The project and design flow are elaborated in this chapter. The utilization of Cadence SpectreRF in analysis to get the results are discussed. Some flowchart were provided to help understanding of using this software tools.

The simulation results for the schematic design are analyzed in Chapter 4. Discussions about the results are elaborated with the help of figures and table. The performance of the Mixer in this work is then compared with the work by others. The detailed comparison is tabled and provided at the end of the chapter.

The final chapter which is Chapter 5 is about the conclusion of the whole project. The achievement of the research objectives that already stated early in Chapter 1 is evaluated in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter consists of 3 sections, starting from Section 2.1 to Section 2.3. Firstly, Section 2.1 explains the summary and overview of Chapter 2. In Section 2.2, the literature review that consists of previous works of mixer. In the last Section 2.3, will conclude this chapter.

2.1.1 Mixer

The basic configuration of a single mixer is that it has two inputs and one output. It multiplies or 'mixes' the carrier signal, either RF or intermediate frequency (IF) depending on an up conversion or down conversion mixer, with another input from the local oscillator (LO) [1] .The LO signal input terminal is used to assist in the heterodyning process, produces the difference and sum frequencies of the two input terminals of interest. After, the output frequencies come out of the output terminal. This subject is built upon and expanded in more depth in the paragraphs below.

This shows that the mixers consists of the distinction and summation of both input frequencies. A mixer can take into account either output function where the unwanted function can be filtered out. The chosen function, which can be either the distinctions or summation of the input frequencies, receives the term down conversion mixer or up conversion mixer respectively.

In a typical mixer design there are four primary defined specifications that are shown which is Conversion Gain (CG), Linearity and Noise Figure (NF). The CG is a ratio between the output signal and the input signal usually in the measure in decibels (dB) or, milli-decibels

(dBm). The linearity of the mixer is defined as how well the mixer reacts to the mixing of frequencies and ideal law of superposition in the ideal case explained in above text. NF is a ratio of the signal-to-noise ratio (SNR) at the IF output and the SNR at the RF input port.

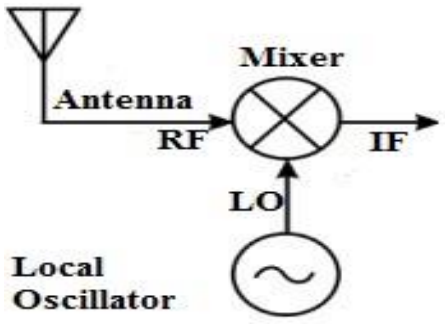

Figure 2.1: Mixer Schematic symbol

METRIC	DESCRIPTION
Voltage supply	The supply voltage should be as low as possible
Power consumption	The mixer with less power consumption is more desirable to prevent excessive energy wastage.
Linearity	High linearity ensures to get the moderate NF.
Noise figure	The lower the noise figure value the better the performance of amplifier, Noise figure will always be greater than one because the output signal to noise ratio will be higher than input.
Frequency	A wide range of frequencies is preferable for mixer in RF design.

Table 2.1: Description of each performance metrics

The Conversion gain, will be further described in the next section. The NF will also elaborated more in later section of this chapter.

2.1.2 Conversion gain

A mixer contains a multiplier circuit that includes MOS transistors designed as a Gilbert multiplier cell without gain resistors such that a first and a second node are directly coupled to a folded cascode output stage. The mixer receives a differential radio frequency (RF) signal and a differential local oscillator (LO) signal, and it creates, at the first and second nodes, a differential intermediate frequency (IF) signal. The mixer additionally includes output and gain/filter stages coupled to the multiplier circuit. The output stage exhibits a low input impedance and a high output impedance, and it produces an output stage differential current equivalent to the differential current of the IF differential signal. The gain/filter stage both controls conversion gain of the mixer, and it filters the high frequency components generated by said multiplier circuit. A capacitor, utilized as the gain or filter stage. [2]

When the RF input transistor M1 operates in the saturation region, then current i_{RF} is given [3]

$$i_{RF} = I_{RF} + gm_1 V_{RF} \tag{2.1}$$

When the LO signal is applied. Then the IF output current can be written as [3]

$$i_{O.}IF = \frac{2}{\pi} gm_1 V_{RF} \cos \omega IF\, t \tag{2.2}$$

If the RF input signal $V_{RF}(t) = V_{RF} \cos \omega IF\, t$. Thus the conversion gain of the single balanced mixer is represented as [3]

$$CG = \frac{V_{IF.rms}}{V_{RF.rms}} = \frac{2}{\pi} gm_1 R_L \tag{2.3}$$

2.1.3 Noise Figure (NF)

Noise figure is on a fundamental level, a simplified model of the actual noise in a framework. A single, theoretical noise component is available in each stage [4]. Thermal noise is a noise that is generated when thermal energy causes free electrons to move randomly in a resistive material [5].

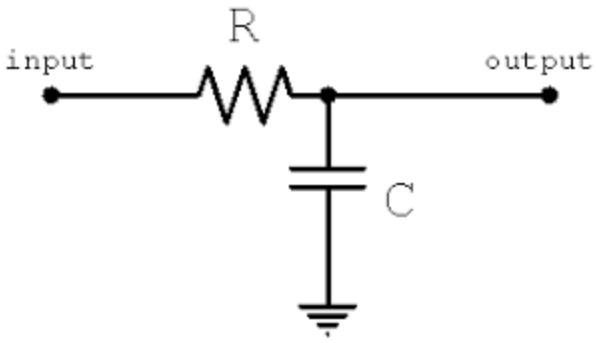

Figure 2.3: Single Pole RC low-pass filter

In any circuit that implements resistors, capacitors, and inductors it will be only the resistors that generate the thermal noise. Total output impedance from figure 2.3 can be expressed [5]:

$$Z_0 = R||\frac{1}{J2\pi fC} = \frac{R}{1 + j2\pi fRC} \tag{2.4}$$

Real part of equation [2.8] can be calculated [5]:

$$Re(Z) = \frac{R}{1 + (2\pi fRC)^2} \tag{2.5}$$

The open circuit rms thermal noise voltage generated by the network in the frequency band from $f_1$and f_2 [5]:

$$V_t = [4kT \int_{f1}^{f2} Re(Z)df]^{\frac{1}{2}} \tag{2.6}$$

Substitute equation [2.5] to equation [2.6] and take the limit from 0 to infinity (∞) will produced equation [2.7] [5]:

$$V_t = [4kT \int_0^{\infty} \frac{R}{(1+(2\pi fRC)^2} df]^{\frac{1}{2}} = \sqrt{\frac{kT}{C}} \quad (2.7)$$

Noise performance in a mixer is measured by the NF. It can be calculated by using the equation [2.9] and is expressed in decibel (dB)

$$NF = 10 \log_{10} F \quad (2.8)$$

The noise factor (F) is measure for degradation of the signal-to-noise (SNR), caused by component in a RF signal chain. Noise factor (F) is defined as [5]:

$$F = SNR_{in}/SNR_{out} \quad (2.9)$$

and SNR can be figured out as follows [6]:

$$SNR_{in} = \frac{Signal}{Noise_{in}} and\ SNR_{out} = \frac{Signal}{Noise_{out}} \quad (2.10)$$

2.1.4 Linearity

Mixer is basically a non-linear circuit and the linearity mainly depends on the non-linearity of the RF stage. The input 3^{rd} orders intercept point (IIP3) and the 1dB compression point (P1dB) are common parameters that are used to measure the degree of linearity. P1dB is a measure of the power of the input signal such that it causes the third order non-linearity to decrease the linear gain by 1dB. Most linear amplifiers have a fixed gain for a particular frequency range. The output power versus input power plot shows a linear relationship (Fig. 2.4). The slope of the line is the gain. As the input power keeps on increasing, at some point the gain begins to decrease. The amplifier goes into compression where no further output increments happen for an input increment. The gain flattens, shows that at high signal levels, the amplifier becomes saturated. Its response progresses toward becoming non-linear and produces signal distortion, harmonics, and potentially intermodulation products.

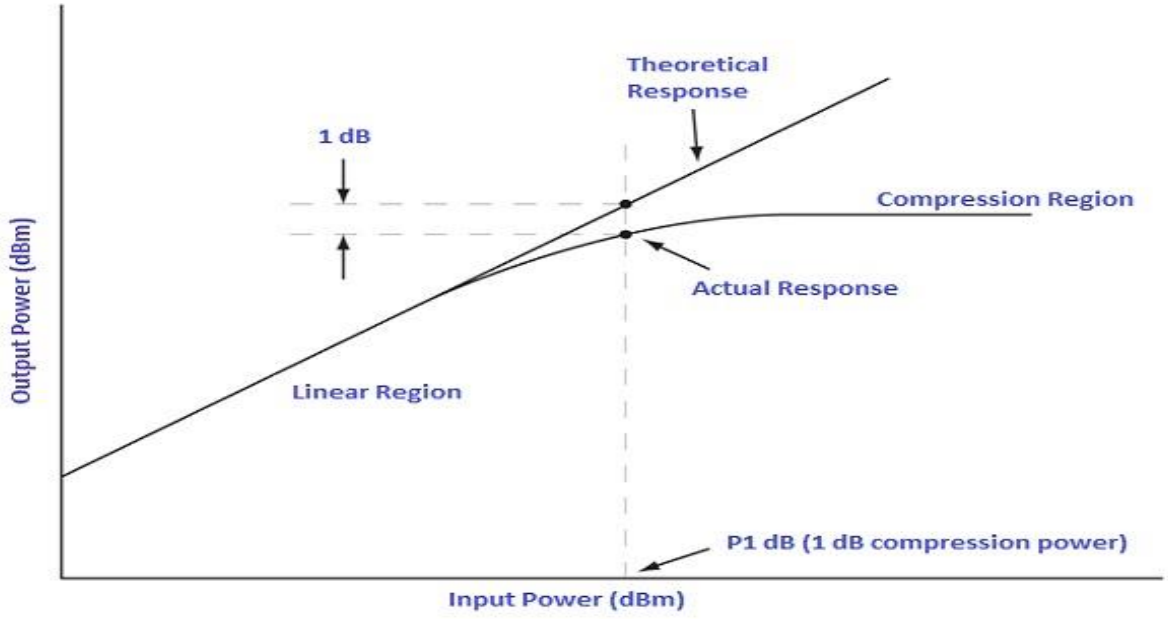

Figure 2.4: 1dB compression point

Third order intercept point is a theoretical value in the linearity diagram. Third order parts of the signals will be created at each enhancement process. Amplifier gain will begin to decline once it achieves the saturation point. If the input power keeps increasing, the fundamental signal power and third order signal power will meet at a specific point. This point is known as third order intercept point. This estimation is utilized to determine the non-linearity behavior of amplifiers during design.

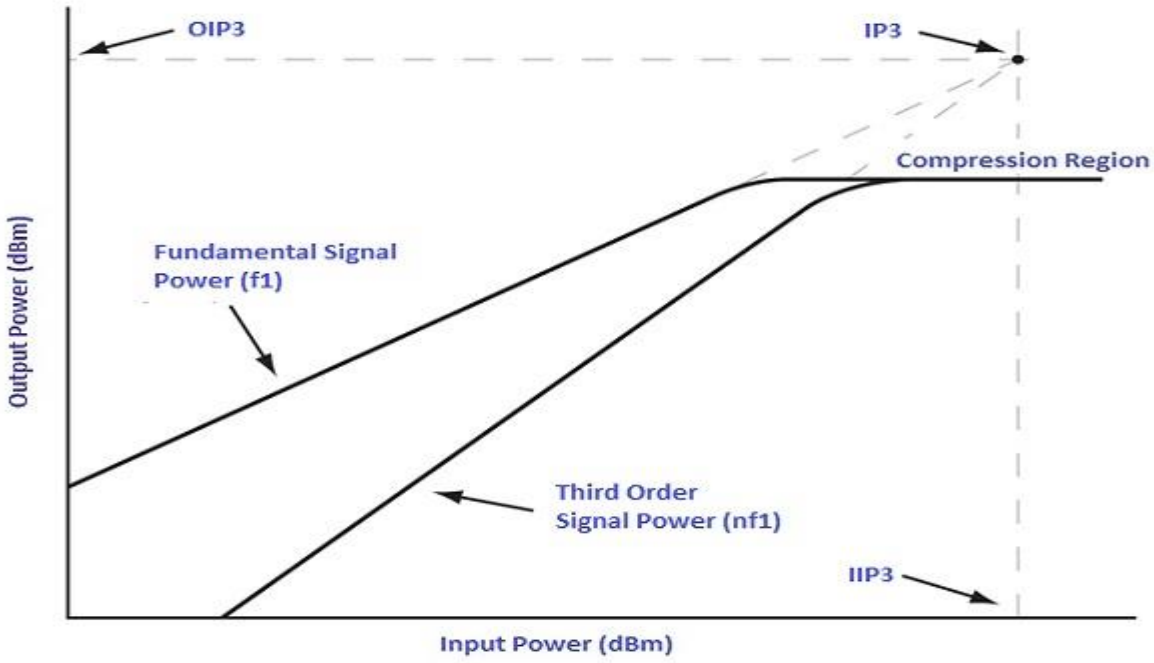

Figure 2.5: Third Order Intercept Point

2.2 Literature Review

In this project, we are focusing on design a Gilbert cell mixer or more specifically a single-balanced Gilbert cell mixer. To achieve our objective, the important aspects that we focused is the simulation of the parameters which are important in design verification of a mixer.

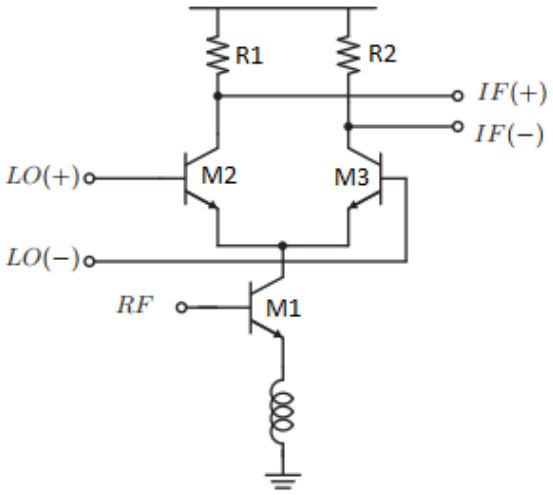

Figure 2.6: Single-Balanced Gilbert Cell mixer

The way that the Single-Balanced Gilbert cell mixer design operates is depicted in Figure 2.6 above. The single wave RF signal first enters into the base of the lower transistor M1, while the LO signal is separated into the based into the base transistors M2 and M3. The input RF signal is then converted into current in the transconductance stage. The current signal is then mixed in with the switching LO signals in M2 & M3. The mixed current is then converted back into voltage via the load, in this case resistors R1 & R2, then the output exits from the respective IF outputs. When this process is taking place the mixer definitions can be controlled and manipulated using particular sections of the layout.

2.2.1 Gilbert cell mixer parameters analysis

Then it comes to CG there is a tradeoff between the resistive load and the drain current in the transconductance stage shown in the following equations below [7]:

$$R_{L=\frac{V_{DD}}{I_{DS_{switch}}}}$$

And

$$CG = \frac{2}{\pi} R_{L\sqrt{K_{nRF} * I_{dsRF}}}$$

Where

$$\mathrm{I}_{dsRF} = \frac{k_n.w}{2 \cdot L} \cdot \left(V_{gs} - V_T\right)^2$$

The resistive load is limited to the supply voltage (VDD) and the dc currents of M2 & M3. Also shown in equation, a mixers CG is directly proportional to RL and I_{dsRF}. A raise in biasing current $I_{DSswitch}$ will disturb the voltage drop on the switching transistors and cause the overall load resistance to decrease lowering the CG. Also for a given VDD, if the bias current in the transconductance stage is raised or lowered the resistive load also needs to be tweaked in order to maintain the voltage biasing conditions of the switching transistors, and not cause a drop in gain.

The linearity, more specifically IIP3, of the Single-Balanced Gilbert cell can be controlled by both the transconductance stage and switching stages. IIP3 is directly proportional to both the drive current and the overdrive voltage shown below.

$$IIP_3 = 4\sqrt{\frac{2}{3} \cdot \frac{I_{dsRF}}{k_n}}$$

and

$$IIP_3 = 4\sqrt{\frac{2}{3}\cdot\left(V_{gs} - V_T\right)}$$

Where the Vgs is the gate voltage of the switching transistors and VT is the threshold voltage of the given Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Also note that the overdrive voltage in equation 2.4 can affect the CG in the previous paragraph. The transistors need enough voltage head room so that the LO amplitude will not swing too high allowing the MOSFET to leave the active regions in the I-V curve and warping the CG.

The NF of the Gilbert cell mixer is mainly affected by the transconductance stage, and secondly by the switching stage via transistor size. The increase in the driver current is inversely proportional to gm, which is inversely proportional to the NF given below [8]:

$$NF = 1O\log\left(1 + \frac{2\gamma_n}{gm\cdot R_s} + \frac{2}{gm^2\cdot RR_s}\right)$$

2.2.2 Advantages and Disadvantages

Given the information stated in the above sections the perfect SB Gilbert cell appears being extremely advantageous. All things considered, every design has this hits and misses. While this design gives moderate good gain at a lower LO power, and low power consumption sometimes these specs can be traded off for other required specifications. Some of those topics include when a designer needs a higher gain as well as the system linearity and is willing traded off power consumption or even NF achieve that design goal. The point that ideally is getting across is that this design isn't sufficiently effective to meet all the numerous mixer design specifications demanded by the communication industry.

2.2.3 Double Balanced Mixer

Despite the fact that the SB Gilbert cell mixer is a solid design and may accomplish the objectives for some design system, it may not be sufficient for designs that call for increased mixer specifications. This is where the Double Balance (DB) Gilbert cell mixer can meet those requirements. DB Gilbert cell mixer is the most commonly utilized active mixer architecture, and contains improvements over other designs including the SB Gilbert cell mixer. The DB mixer can accomplish higher mixer specifications in the area of CG, linearity, and port isolation at the cost of a small increment in NF and overall designs power consumptions.

2.2.3.1 DB and SB Gilbert Cell Mixer Comparisons

With regards to the mixer definitions, the DB Gilbert cell mixer is better in most areas compared to the SB mixer design. The CG is better in DB since it has the ability to maintain a higher transconductance. As for linearity, in the DB Gilbert cell the ports suppress the input frequencies better than the SB mixer permitting better control over harmonics products. In the area of port isolation the DB architecture is higher because of the transistor stacking and schematic setup. This gives better isolation between the input and output ports. The cost of gaining these improvements comes with the cost of higher NF and power consumption. The NF is typically higher in the DB design, because there are more transistors. Additionally the design has a higher probability of noise being created by non-ideal switching transistors. Another sacrifice is a higher power consumption that occurs from an increased supply voltage. This voltage raise is expected to properly operate the multiple transistors that are expected to build the larger DB design.

2.3 Summary

This chapter is reviewed according to the related work for this Gilbert Cell Mixer design. The important terms, equation, methods for consideration and the factors used in simulating this project is presented. The related work is available via books, journals or articles that helps in this project. Selection of a RF power amplifier is depends on numerous factor as stated above. S-parameters of the amplifier might be required for some assessment and design. Well matched amplifiers are critical for effectiveness in signal transmission and receiving systems. Thus, from the literature reviewed and studied in this chapter, the method used in this project is discussed in the next chapter.

CHAPTER 3

METHODOLOGY

3.1 Introduction

Mixer circuits play an important part in defining the performance of the transceivers. In this paper work, planning of a mixer and its performance at high frequencies are discussed in detail based on which the efficiency and quality of the correspondence system will be defined [9]. The off-chip filters are utilized at high frequencies because getting the high Q is very difficult in the case of on chip filters. In the receiver circuits based on the design requirement both active and inactive mixers are utilized. However with high gain and capacity of compensating various losses of the filter sections most of the designers prefer to use the active filters. A detailed analysis investigation on the functionalities of mixer circuits and performance parameters of a mixer circuit in UWB frequencies are clarified in the following section. The significant uses of UWB incorporates into the zone of Communication system for example, remote sound and video transmissions, RF tagging and identification; radar applications and for precision geo-location tracking and localizations [10].

The direction of this work is to design a Single-Balanced Cell Mixer with wide range of frequency from 401MHz to 406MHz. The purpose is to provide amplification with minimum noise added to the whole circuit. To get started with the design, circuit analysis is required to understand how the circuit operates. Besides, to boost up the circuit performance, optimization is needed in achieving the objectives as well as the specification of this work. The user of Cadence SpectreRF should be familiarized with the correct steps to obtain the simulation data for design verification and further analysis.

3.2 Calculated Values of Component

Calculation by hand is a process in which the determination of the initial components' values used in the Mixer circuit is made based on calculation. The passive components such as resistors capacitors as well as the width of the MOSFETs need to be calculated first provide good initial assumption.

3.3 Adaptation to Cadence SpectreRF Working Operation

Cadence SpectreRF is configuration device software that can assist IC design. It covers functions and for somebody who plan to utilize the software, the requirements to be familiar with its functions is compulsory to lead correct simulation and ready to get focused on specifications. The simulation of S-parameters, NF, linearity or other important performance should be possible by utilizing Cadence SpectreRF.

3.3 Targeted Design Parameter

Parameter	Values
Supply Voltage	1.8V
Total Power	< 10mW
Total Current	< 20mA
RF Voltage	0.58V
LO Voltage	1V
Bandwidth (MHz)	401- 406
NF	Around 10dB
IP1dB	< -11dB
IIP3	> -10dB

Table 3.1: Design Parameter Specifications for SB Gilbert Mixer

3.4 Simulation

Once the schematic design of the mixer is finished, the next step is to conduction the simulation to verify the design. This is important to determine that the designs fits in with the specifications set. Through simulation, the difference between the simulation results and the focused on specifications are obviously recognized so that modifications can be conducted on the estimations of the passive active components until the simulation results are coordinated with the targeted specification. Simulation for this work is only limited to the pre-layout where the function of the design is verified and the performance optimized.

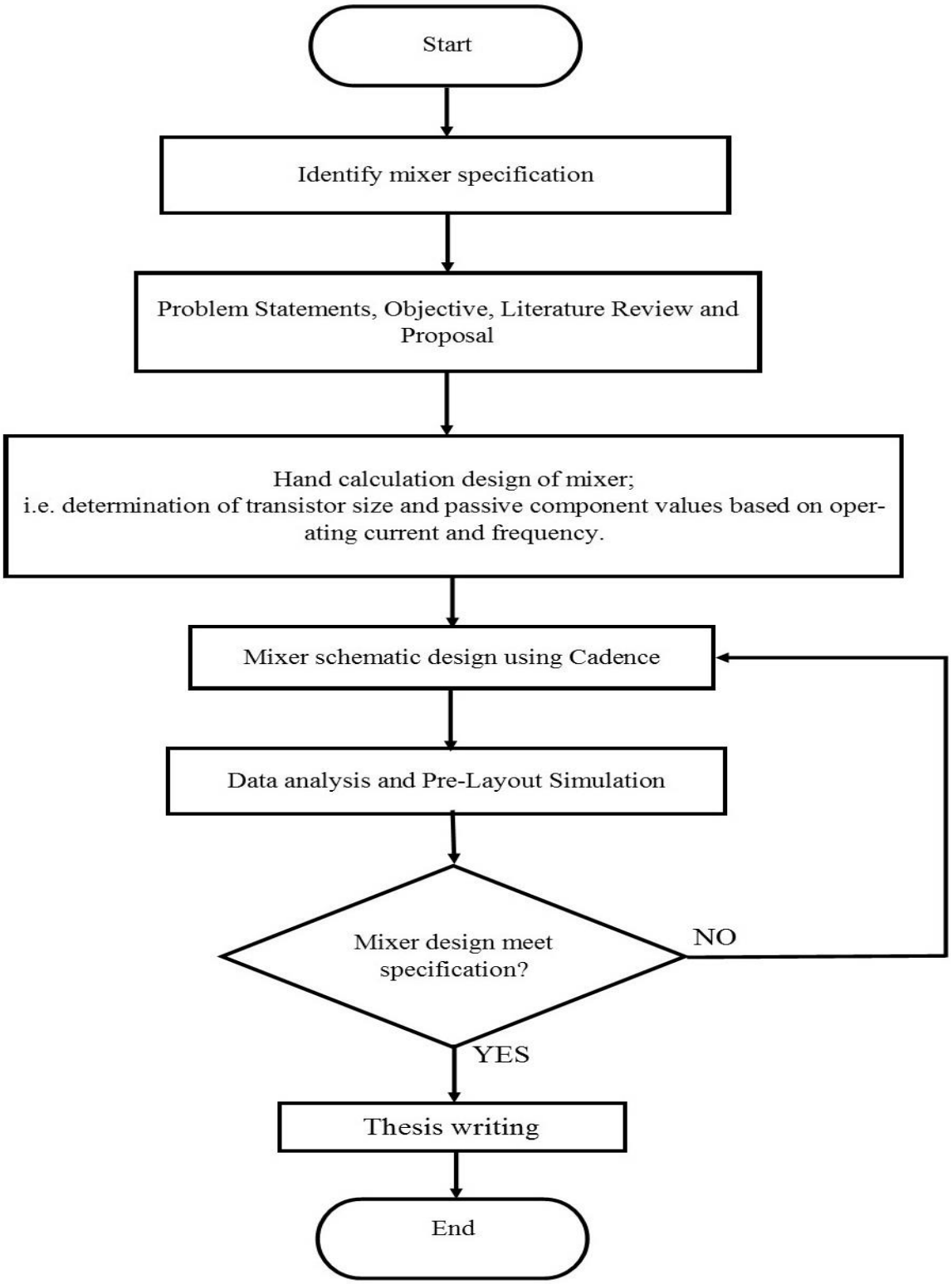

Figure 3.1: Flow chart project implementation

Table 3.2: Component value of the mixer

Component	**Value**	**Component**	**Value**
V_{DD}	1.8V	C_1	60f F
V_{biasLO}	1V	C_2	60f F
R_1	1KΩ	C_3	8p F
R_2	1K Ω	M_1 (W/L)	100µm / 180nm
R_3	50 Ω	M_2 (W/L)	100µm / 180nm
R_4	50 Ω	M_3 (W/L)	180µm / 180nm

Table 3.3: Performance comparison with others work

Reference	[11]	[12]	[13]	[14]
Technology (μm)	0.18	0.13	0.18	0.18
V_{DD} (V)	1.0	0.5	1.8	1.0
Operating Frequency (MHz)	401-406	433	402-405	401-457
Conversion Gain (dB)	28.7	50	25.7	29-31
Noise Figure (dB)	5.5	8.1	10.2	<5.2
P1 (dBm)	n/a	n/a	n/a	n/a
IIP3 (dBm)	-25	-20.5	-17	>-19.5
Current consumes (mA)	n/a	n/a	n/a	n/a
Power consumtion (mW)	0.49	0.3	1.3	0.37

3.5 Method of Simulation and Data Collection

The simulation and data collection for this work are mainly performed by the Cadence SpectreRF analysis. This software is able to simulate the Spectre circuit as it grants the user with the effective computation of steady state solution and circuit simulation involving a wide range of bandwidth.

3.5.1 Direct Current (DC) Analysis

The DC behavior is one of the center of attention in dealing with circuit design. By simulating the DC characteristics, the user gains knowledge in which region the transistors are located, how much current is flowing in the circuit and many more. Thus, DC analysis is the first analysis to be done in this work.

"Tools > Analog Environment" was selected at the menu bar from the schematic window in Cadence SpectreRF. Analog Design Environment (ADE) pops-up on the screen. In the setup menu, choose the Model Libraries and select the library files to be used in the schematic.

In the ADE window, "Variable> Copy" from Cellview was selected followed by the appearance of the design variable. The value was set for each design variable. After that, "Analyses > Choose" was chosen and DC was selected to run the DC analysis. "Save DC operating point" was chosen and "Enabled" function was highlighted before clicking "OK". Last but not least, "Netlist and Run" icon was selected and all the signal DC values will be displayed on schematic. A complete flowchart on performing the DC analysis is shown in Figure 3.2.

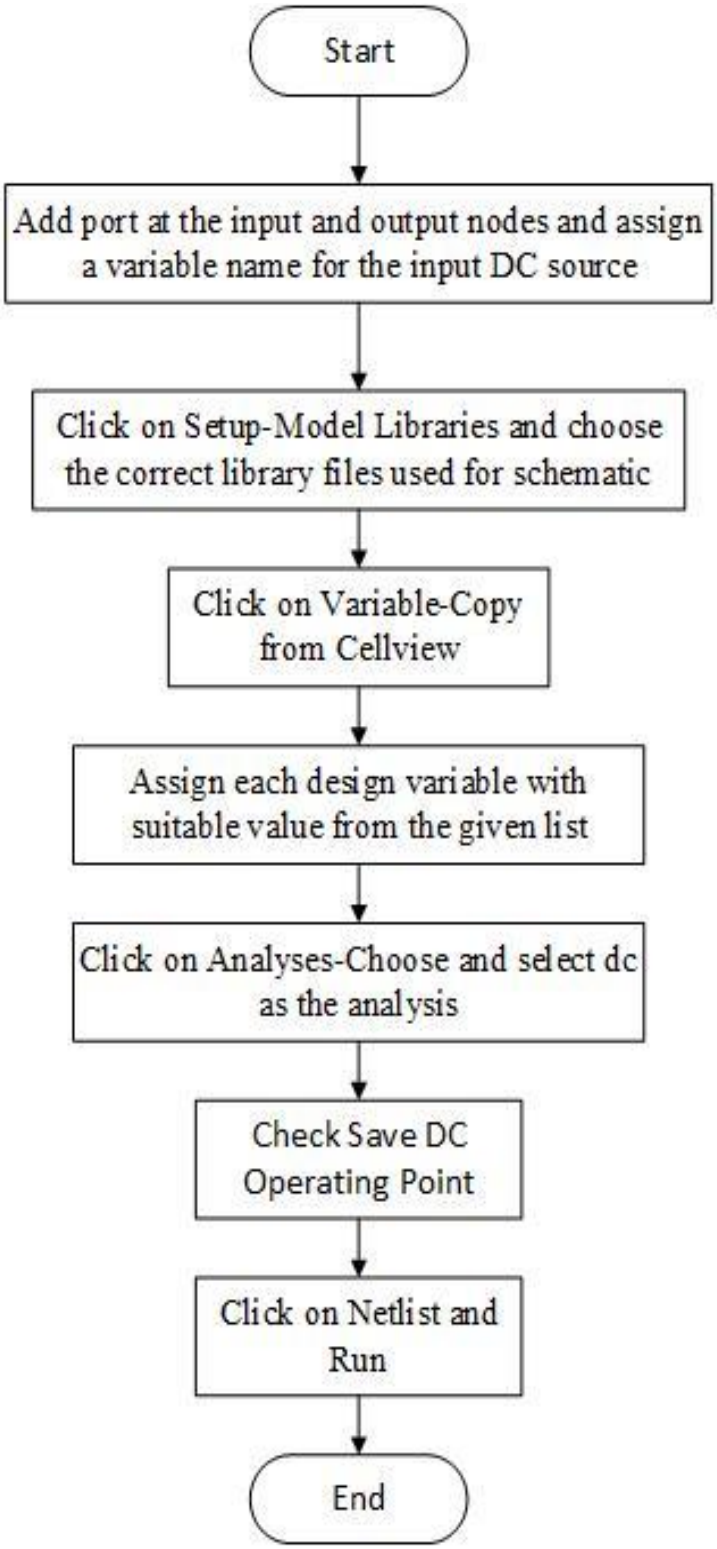

Figure 3.2: Flowchart DC Analysis.