DESIGN OF 0.18-um CMOS VOLTAGE CONTROLLED OSCILLATOR (VCO) FOR 2.45GHz IOT APPLICATION

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DESIGN OF 0.18-um CMOS VOLTAGE CONTROLLED OSCILLATOR (VCO) FOR 2.45GHz IOT APPLICATION

by

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LIST OF ABBREVIATIONS

ADE	Analog Design Environment
AM	Amplitude Modulation
CMOS	Complementary Metal-Oxide Semiconductor
DC	Direct Current
DRC	Design Rule Check
FoM	Figure of Merit
FM	Frequency Modulation
IoT	Internet of Things
LVS	Layout Versus Schematic
MOS	Metal-Oxide-Semiconductor
NMOS	Negative-channel Metal-Oxide Semiconductor
PMOS	Positive-channel Metal-Oxide Semiconductor
RF	Radio Frequency
VCO	Voltage Controlled Oscillator
Wi-Fi	Wireless Fidelity
LR-WPAN	Low-Rate Wireless Personal Area Network

REKA BENTUK 0.18-um CMOS VOLTAN DIKAWAL PENGAYUN (VCO) UNTUK APLIKASI 2.45GHz IoT

ABSTRAK

Ruang pintar dinaikkan taraf sebagai Internet Perkara (IoT) disebabkan oleh pertumbuhan pesat dalam pengecilan peranti elektronik dan integrasinya ke dalam produk harian. Salah satu blok hadapan RF bagi IoT yang mencabar ialah reka bentuk hingar fasa rendah dan litar kuasa rendah. Terdapat keperluan untuk meningkatkan prestasi pemancar-penerima untuk menangani cabaran ini. Pengayun voltan terkawal (VCO) mewakili blok penting untuk menentukan prestasi pemancar-penerima RF. Oleh itu, dalam penyelidikan ini, reka bentuk telah ditekankan pada VCO kuasa rendah. Dalam reka bentuk CMOS VCO, topologi khas yang dilaksanakan ialah VCO tangki LC. Walau bagaimanapun, untuk mencapai prestasi yang sama seperti VCO tangki LC pada penggunaan kuasa yang lebih rendah, VCO CMOS arus diguna semula telah dilaksanakan. VCO arus diguna semula kelas-C ini mempunyai kecekapan penukaran arus DC-RF yang lebih tinggi dan secara keseluruhan lebih baik dalam prestasi berbanding VCO kelas-B. Dalam penyelidikan ini, 0.18-um VCO kelas-C dengan topologi arus diguna semula yang menggunakan kuasa rendah telah dilaksanakan untuk aplikasi Internet Perkara (IoT) 2.45 GHz. Penggunaan kuasa dan hingar fasa adalah masing-masing 1.99 mW dan -110.0 dBc/Hz@1 MHz. Pada akhir kerja ini, prestasi yang dicapai oleh VCO kelas-C arus diguna semula dibandingkan dengan kerja oleh penyelidik lain dalam bidang yang sama.

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ABSTRACT

Smart spaces is promoted as an antecedent to an Internet of Things (IoT) due to rapid growth of miniaturization of electronics and its integration into daily products. One of the challenging RF front ends blocks for IoT are the design of low phase noise and low power circuit. There is a necessity to raise the performance of transceiver to tackle this challenge. The voltage-controlled oscillator (VCO) represents the vital block to determine an RF transceiver performance. Hence, the design will be emphasized on low power VCO. In CMOS VCO design in this research, the typical topology implemented is the LC-tank VCO. However, to achieve the same performance as an LC-tank VCO at lower power consumption, a current reuse CMOS VCO was implemented. The current reuse class-C VCO has higher DC-RF current conversion efficiency and in overall more superior in performance than the class-B VCO. In this work, a 0.18-um current reuse class-C VCO consuming low power has been implemented for use in 2.45 GHz Internet of Things (IoT) applications. The power consumption and phase noise are 1.99 mW and -110.0 dBc/Hz@1MHz respectively. At the end of this work, the performance achieved by the current reuse class-C VCO will be compared with work by others in the same area.

CHAPTER 1

INTRODUCTION

1.1 Research Background

Recently, there is a dramatic rise in Internet of Things (IoT) devices and connected products. Gartner[1] predicts that there will be approximate 20 billion devices connected to the IoT by 2020 and IoT product and service suppliers will amount to a business of $300 billion in revenue. IoT is the network of products that are embedded with nodes to collect and exchange data. A typical IoT node consists of a microcontroller unit (MCU) that processes data and runs software stacks interfaced to a wireless device for connectivity. It should be portable and long lasting. However, issues of power consumption minimization and wireless connectivity range extension are being the present concerns.

To solve these, Bluetooth Low Energy (BLE) has developed which fulfilling low cost narrow-band standards, while maintaining similar communication range. BLE benefits from low-latency, fast connection and small size.[2] BLE has an ultra-low power operative mode suited to shot-range communication. In the applications such as in-door location, remote controls and contactless payments, the delivered power is minimized and the battery life is long.[3] BLE has radio frequency of 2.4GHz, matching the desired frequency of VCO (2.45 GHz).

A wireless transmitter is a crucial part in IoT. It uses radio frequency (RF) connectivity to achieve transmission (TX) and reception (RX) of the data. The frequency of 2.4GHz is a good selection to meet the requirements for transceiver design,

given the high profile of this 2.4 GHz ISM (industrial, scientific and medical) band with many existing wireless standards such as Bluetooth, Wi-Fi and LR-WPAN.

Besides power saving, low cost and reliable, a transceiver should be able to work under various environmental conditions even with the presence of RF interference and noise. An RF VCO is located inside the transceiver. It produces signals that is used for frequency synthesis.[1] There are two main categories in VCOs: ring-based VCO and LC-based VCO. LC-based VCO is more preferred due to better phase noise performance. Despite the ring oscillator consuming lower power, it suffers from poor phase noise above 1GHz frequency. In contrast, LC oscillator can reach lower phase noise with greater power and more area above this frequency.[4]

1.2 Problem Statement

Although there are many types of LC-based VCOs available in the market, the constraints such as phase noise and power consumption that will affect the performance of VCOs still exist. A VCO with phase noise performance superiority may consume high power.[5] In other words, their performances are not yet optimized. Thus, figure of merit (FoM) is used to characterize and compare the overall performance of the VCOs.

Besides that, the sizes of passive components are larger than that of active components. Capacitor, inductor and resistor are the examples of passive components, while transistor is an active component. Too many usages of passive components will increase the fabrication size of VCO. Although utilization of active components are encouraged, for example transistors, they are, however, very open to parasitic effects.

Moreover, the bias current flicker noise happens when the circuit is oscillating.[6] As mentioned previously, higher gate bias is supplied at initial stage to

provide enough transconductance, g_m. The downside encountered is that the quality factor is decreased because it loads the VCO resonator tank.[7]

1.3 Objectives of Research

The main objective of this research is to design a 0.18-um CMOS VCO for 2.45 GHz IoT operation with focus on low phase noise and power consumption performances. This objective can be further detailed out as follows:

- To study on various VCO design and determine the most appropriate topology for IoT application
- To design and construct schematic of the circuit and verify it by using Cadence Virtuoso
- To optimize the overall layout performance of proposed design at phase noise of -110 dBc/Hz @ 1 MHz offset frequency and power consumption of 2 mW

1.4 Scope of Research

This research will focus on design of VCO by applying class-C current reuse technique. Although there are other more popular topologies like the LC-tank, the current reuse class-C VCO is more attractive for IoT application due to its low power consumption. Another requirement set by the project is to implement passive LC only and not trying to design active LCs. Active devices are not suitable for low noise design applications as they contribute relatively to high phase noise.

The phase noise of a CMOS LC VCO is mainly determined by bias noise, active device noise and quality factor of resonant tank. To eliminate bias noise, the transistors

should remain in active region and never enter triode region. Active device noise can be reduced by sizing width over length $\left(\frac{W}{L}\right)$ of transistors properly. Quality factor is a measurement for indicating the energy losses within a resonant element. In resonant tank, only the quality factor of inductor will affect the phase noise. From equation 1[8]:

$$\frac{1}{Q} = \frac{1}{Q_C} + \frac{1}{Q_L} \tag{1}$$

Q_C is contributed by fixed capacitor and variable capacitor. The high value of Q_C makes this term negligible.

The design and verification are done by using Cadence Virtuoso for the schematic design and Mentor Graphics Calibre for the post layout. The design is limit to until post layout simulation only as measurement will not be possible due to time and cost limitations.

1.5 Thesis Outline

This thesis contains five chapters, which are organized as the following. Chapter 1 describes the background and the importance of the study. The objectives of carry out this research and the scope of research are also included.

Chapter 2 discusses on different types of VCO with passive inductor conducted by previous researchers. Current reuse class-C VCO, VCO with eliminated bias transistor, VCO with unique variable-capacitor filtering technique, VCO with closely spaced digitally tuned coarse capacitor bank and VCO with third harmonic tuned LC tank with noise filtering technique are discussed in this chapter.

Chapter 3 describes the methodology that has been carried out in this research. The process involved and the circuitry used in this research are explained in detail in this chapter.

Chapter 4 shows the results obtained from this research. The results are analysed and discussed in this chapter.

Chapter 5 concludes the research. Further improvement and suggestion are proposed.

CHAPTER 2

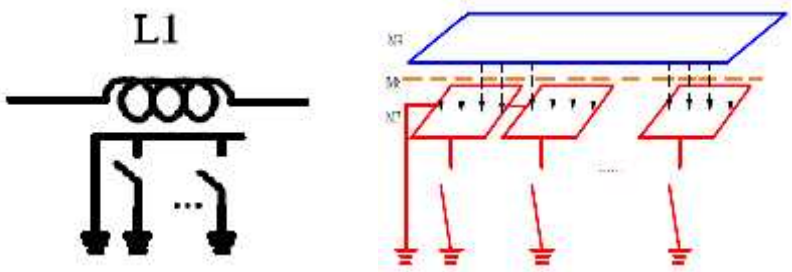
VCO FUNDAMENTALS AND LITERATURE REVIEW

This chapter includes a literature review that covers various VCO designs implemented by other researchers. An oscillator acts as a filtered noise generator and the carrier will be surrounded by noise, equivalent to random AM and FM modulations on the ideal RF sine wave. This external noise is called as phase noise. Oscillation frequency is the number of oscillations per second. Phase noise and oscillation frequency are essential performance metrics of a VCO. To determine them, pss and pnoise analysis must be simulated.

All the VCOs discussed in this chapter are passive LC based. Section 2.1 illustrates switching variable inductor. Section 2.2 introduces about current reuse class-C VCO. Section 2.3 discusses about VCO with eliminated bias transistor. Section 2.4 describes VCO with its unique variable-capacitor filtering technique. Section 2.5 relates to VCO with closely spaced digitally tuned coarse capacitor bank. Section 2.6 presents VCO with third harmonic tuned LC tank with noise filtering technique. Section 2.7 summarizes this chapter.

2.1 Switching Variable Inductor

It is a dual-cross couple LC-tank VCO with adjustable ground-plate inductor. The top metal is used as inductor. The ground point can be varied in order to get different value of inductor. As ground area changes, the cut of magnetic flux exists and the inductor value changes.[9]



(a) *(b)*

Figure 2.1: (a) Adjustable inductor with variable ground-area. (b) Schematic diagram of adjustable inductor.[9]

The complementary cross-coupled have the pros of relaxed start-up condition, differential-ended, easy implementation and more balanced output. Its cons are poor phase noise performance and lower energy transfer efficiency. Therefore, switched-modes variable inductor is added into circuit. This circuit composes of complementary cross-coupled pairs (M1/M2 and M3/M4) that provide negative resistance for oscillation. Varactors (C1 and C2) function are for fine-tuning, which are tuned by applied voltage V_t. There are complementary buffers at outputs (V_a and V_b) for output matching and protecting external effect. Figure 2.2 depicts the schematic of VCO based on adjustable inductor with MOS-inversion varactor combination.[9]

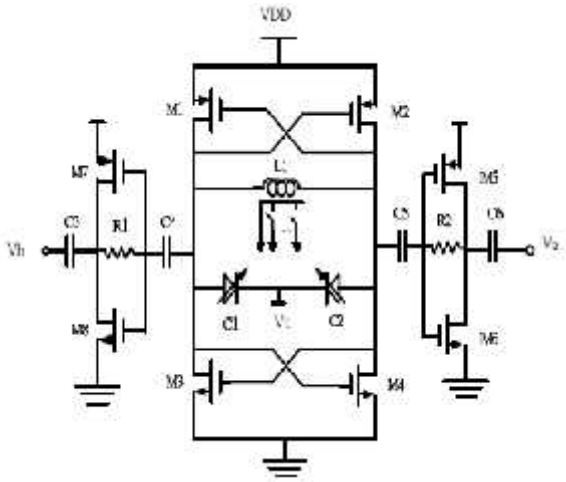


Figure 2.2: Schematic of variable inductor VCO.[9]

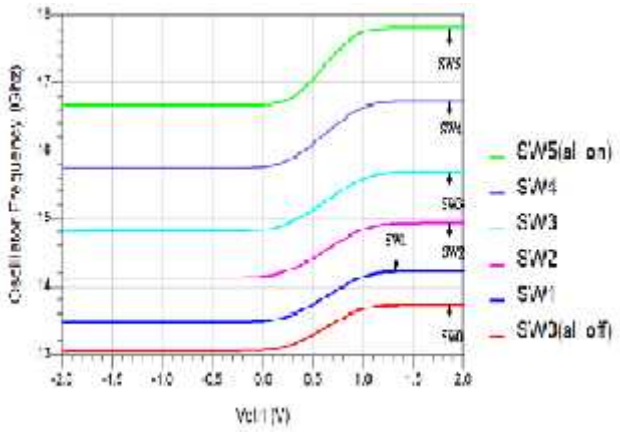


Figure 2.3: VCO frequency versus varactor voltage with various switch operations.[9]

2.2 Current reuse class-C VCO

This is a low power current reuse class-C VCO with dynamic biasing for NMOS and PMOS transistors to provide robustness in oscillation startup (initial state) and large oscillation swing at the steady state.[10] It comprises of three main components: a core VCO and dynamic bias circuits for NMOS and PMOS transistors. The core VCO is built up of a pair of cross-coupled PMOS and NMOS transistors, while two modified current mirrors represent the dynamic bias control circuits. Both NMOS and PMOS should remain in active region to prevent current-reuse VCO enters voltage-limited region.

To ensure oscillation start-up, higher gate bias for NMOS, $V_{g,n}$ and lower gate bias for PMOS, $V_{g,p}$ are applied. The circuit operation is explained as follows. Before VCO starts oscillation, $I_{REF,n}$ and $I_{REF,p}$ determines initial gate biases of NMOS and PMOS transistors. Oscillation condition is met when enough transconductance is supplied by the current in core VCO. At this time, output voltage will swing across V_{tune} . At the steady state, $V_{g,n}$ and $V_{g,p}$ adaptively changes its value to become lower and higher, respectively, to maximize oscillation swing in a current-limited regime. Class-C

VCO is chosen since it has higher DC-RF current conversion efficiency can provide a theoretical 3.9 dB lower FOM comparing to conventional Class-B VCO.[10]

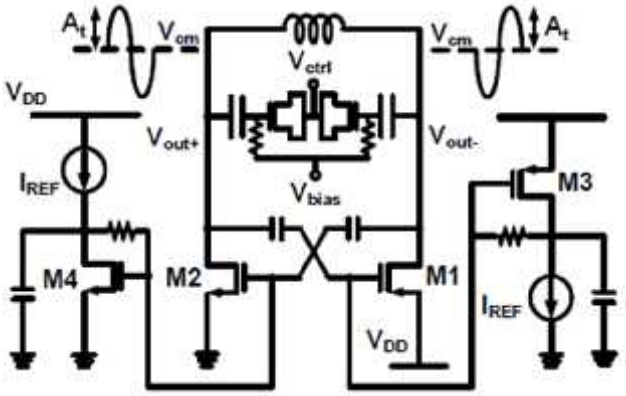
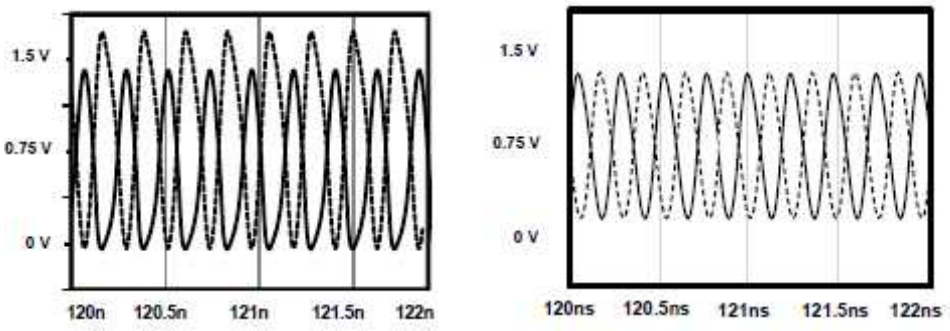


Figure 2.4: Schematic of current reuse class-C VCO.[10]



(a) (b)

Figure 2.5: (a) Output amplitude without dynamic bias control circuits. (b) Output amplitude with dynamic bias control circuits.[10]

2.3 VCO with Eliminated Bias Transistor

This is a modified cross-coupled transconductance VCO, where the bias transistor is eliminated. In this circuit, MOS capacitors are inserted between two cross-coupled connecting paths to form capacitive divider networks. Large $\frac{W}{L}$ ratio keeps the transistors in triode region so that less flicker noise will be generated than that in

saturation region. Trapping and detrapping of carriers in the oxide layer generates flicker noise in CMOS transistors.

There are two factors reducing the possibilities of carrier trapping. First, a weak inversion channel is formed under the oxide layer when a transistor is in triode region, where the carrier concentration is lower than that in the strong inversion channel established when the transistor is saturated. Second, due to the smaller V_G , the vertical electric field over the gate is smaller in the triode region than that in the saturation region.

Since the MOS capacitors eliminate DC feedback paths from the output nodes of VCO to the gate of transistors, the resistor networks R1, R2 and R3 are implemented to bias the transconductors. To alleviate the effect of circuit noise on the phase noise, the transconductors should be biased below the threshold voltages of the transistors to make the conducting drain current approximately at the zero crossing points of the output waveform, where it is most sensitive to noise perturbation. Nevertheless, this design contains too many passive components that will take up a lot of fabrication space. In addition, it is mainly reducing flicker noise, which is insignificant in high frequency VCO designs.[11]

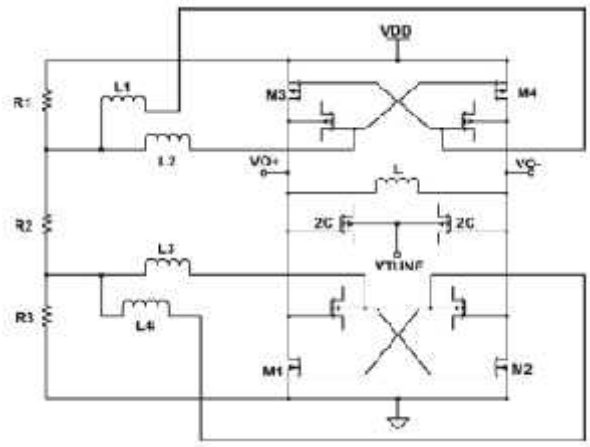


Figure 2.6: Schematic of VCO with eliminated bias transistor.[11]

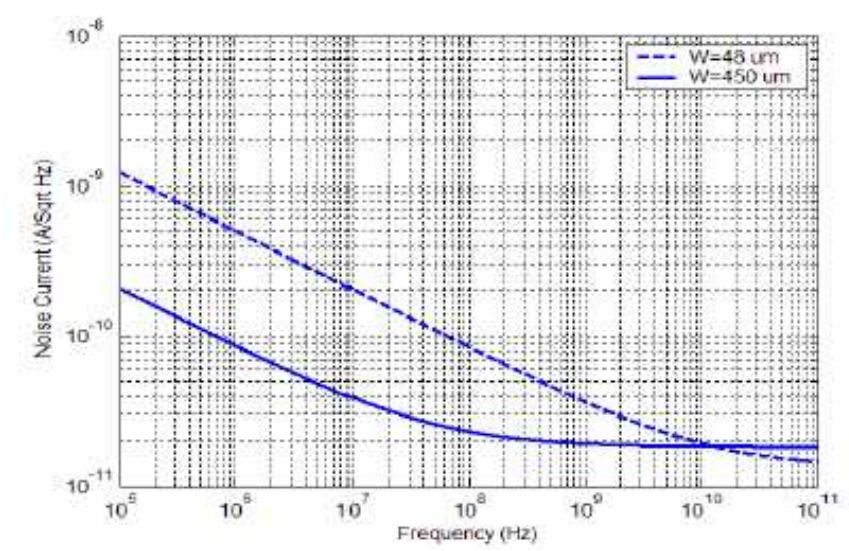


Figure 2.7: Noise spectral density of two NMOS transistor with the same drain current, one in the saturation region (W=48µm), the other in the triode region (W=450µm).[11]

2.4 VCO with Unique Variable-capacitor Filtering Technique

The concept of this design is two identical LC-tanks will produce lower phase noise than single LC-tank. It does not have top current source, meanwhile low phase noise and low power consumption can be achieved. For the resonator part, it contains a fixed capacitor (C), an inductor (L) and a pair of advanced-CMOS (A-MOS) varactor diodes. A-MOS technology is chosen to increase voltage-tuning range. The loss of LC tank is compensated by negative impedance generation from cross-coupled NMOS (M1, M2) and PMOS (M3, M4) transistor pairs. PMOS supresses flicker noise and controls current consumption.[12]

The weight to length ratios $\left(\frac{W}{L}\right)$ of transistors are adjusted to obtain appropriate g_m. The quality factor, Q of the tank circuit will greatly affect the oscillator phase noise. The higher the quality factor, the lower the phase noise. Thus, usage of high Q inductor is prioritized. The effects of third and higher order harmonic signals

from LC resonator are negligible, but that of second order must be taken into considerations. To solve this, a new filtering technique has been introduced where the inductor and variable capacitors are involved. When there is a change in oscillation frequency, the capacitance of variable capacitors (C_{var}) can be set to suitable value.[12]

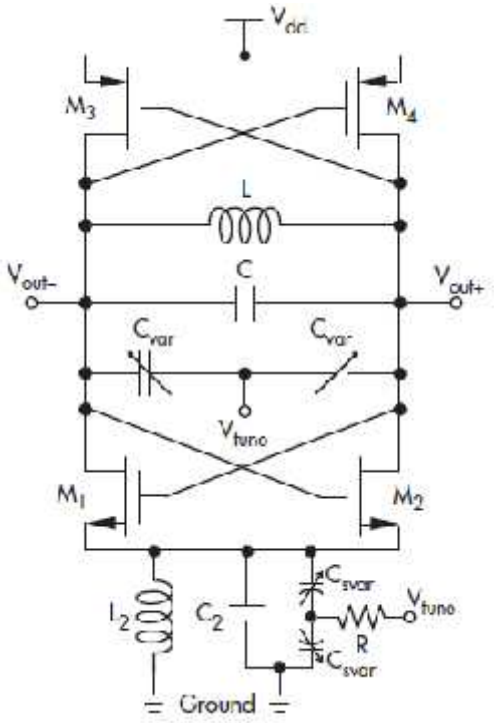


Figure 2.8: Schematic of VCO with unique variable-capacitor filtering technique.[12]

2.5 VCO with closely spaced digitally tuned coarse capacitor bank

In this circuit, using a single varactor to reach the frequency of 2.4GHz would lead to the problem of large fixed capacitance, where it will reduce the inductance needed for resonance, thereby increasing power. Hence, a closely spaced digitally tuned coarse capacitor bank that centres the VCO reaching its required frequency. Complementary cross-coupled architecture is applied to this low voltage VCO with the intent of minimizing power. A challenge for low voltage operated VCO is the transistors are operating in subthreshold region and bringing large sizes and parasitic capacitance problems. Current for the similar transistors are increased by applying body

biasing to the transistors to reduce the transistor sizes, but power limitation occurs while providing bias voltages separately for NMOS and PMOS transistors. Consequently, self-body-biasing scheme is proposed where the bodies of PMOS and NMOS are tied together. The body diodes self-bias at half of V_D . The forward current in the body diodes becomes negligible, reduction of transistor sizes are achieved and thus reducing parasitic capacitance. In short, it is suitable for low voltage design to increase current, meanwhile it is high power consuming.[13]

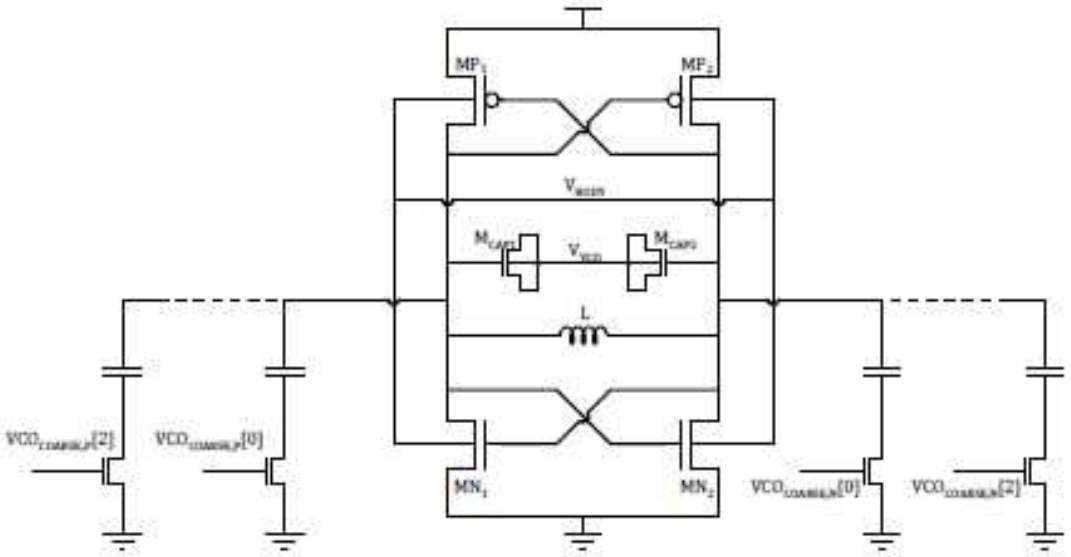


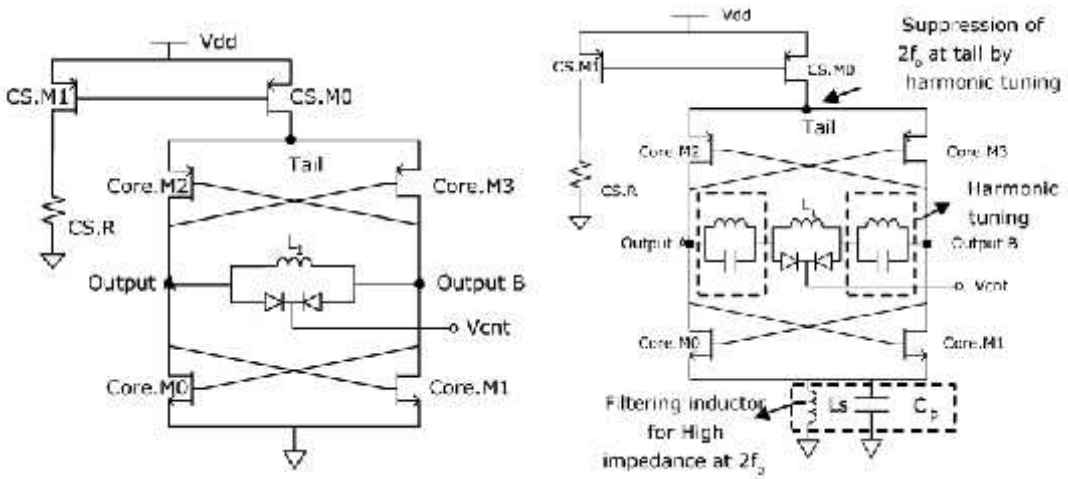
Figure 2.9: Schematic of low-voltage VCO with self-body-biasing and coarse frequency tuning.[13]

2.6 VCO with Third Harmonic Tuned LC Tank with Noise Filtering Technique

This design adopts third harmonic tuned LC tank in corporation with noise filtering technique to effectively improve the phase noise performance.[14] The harmonic tuning is able to increase the slope of output voltage wave at the zero crossing point, therefore reducing the switching time from on to off state of the negative g_m. The difference between standard-top biased VCO and optimized harmonic tuned VCO is in

their NMOS transistors connection. As shown in Figure 2.11 (a), the source node of NMOS transistors (M0 and M1) are connected to ground. One of the NMOSs will be in the triode region when the differential oscillation voltage crosses V_T. Thus, the decrement of resonator Q factor has degrading phase noise performance.

The filtering, by an inductor (L_s) and a parasitic capacitance (C_p) create parallel resonation.at $2f_o$ frequency at the source nodes; prevent differential pair FETs in the ohmic region from loading the resonator, maintaining high resonator Q factor. The thermal and flicker noise can be significantly reduced by practising this technique which has independent phase noise reduction effect and combination techniques.[14]



(a) (b)

Figure 2.10: (a) Schematic of standard VCO. (b) Schematic of optimized HT VCO.[14]

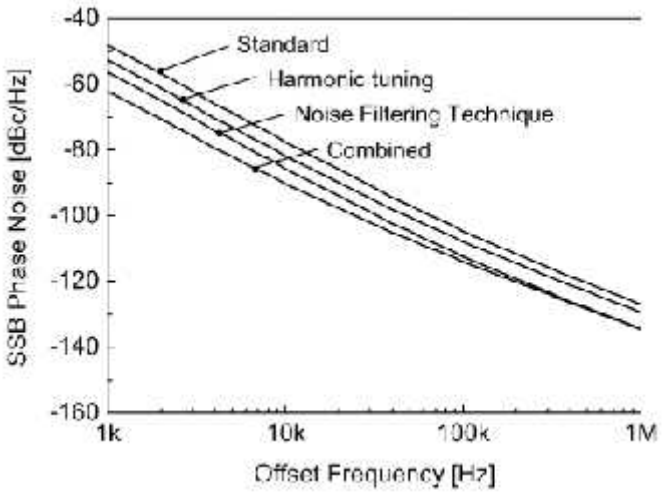


Figure 2.11: Comparison of phase noise performance between all the techniques.[14]

2.7 Summary

Table 2.1 includes the performance benchmark of all the VCOs discussed above. The switching variable inductor performs well but in the model library used in this work, there is no such component. The elimination of bias transistors technique is because it involves too many inductors that will occupy large fabrication size. For closely spaced digitally tuned coarse capacitor bank technique, it is mainly for low frequency designs. Figure of merit (FoM) of all the designs are almost the same, but the performance of current reuse class-C technique still have the biggest potential to be optimized if considering other metrics.

Table 2.1: Comparison of VCO designs

Matrices	[9]	[10]	[11]	[12]	[13]	[14]
Technique	Switching variable inductor	Current reuse class-C	Eliminat-ion of bias transistor	Variable-capacitor filtering	Closely-spaced digitally tuned coarse capacitor bank	Third Harmonic Tuned LC Tank with Noise Filtering
Process (µm)	0.09	0.18	0.18	0.18	0.065	0.13
Supply voltage (V)	1.2	1.5	-	1.6	0.68	1.8
Frequency (GHz)	13.35-15.6	4.6	-	2.5	2.4	2.17
Gain, K_{VCO} (GHz/V)	-	-	-	0.025-0.27	0.087	-
Phase noise (dBc/Hz) at 1MHz	-115.03	-119	-109	-127.6	-110	-132
P_{DC} (mW)	6	2.4	-	8.24	-	5.92
Figure of Merit (FOM)	-190.56	-189	-	-186.4	-	-189.5

CHAPTER 3

METHODOLOGY

This chapter is to present the methodology on VCO design using Cadence Virtuoso. Initially, the proposed schematic circuit is drawn. This project continues with running pre layout simulation and constructing VCO layout. Before proceeding to further steps, Design Rule Check (DRC) is required to make sure the design meets the respective foundry's design rule. Figure 3.1 depicts the flow of project development.

Section 3.1 explains about the structure of the schematic. Section 3.2 introduces about the pre-layout simulation. Section 3.3 describes how the layout is done. Section 3.4 and section 3.5 illustrate the importance of design rule check (DRC) and layout versus schematic (LVS). Section 3.6 summarizes this chapter.

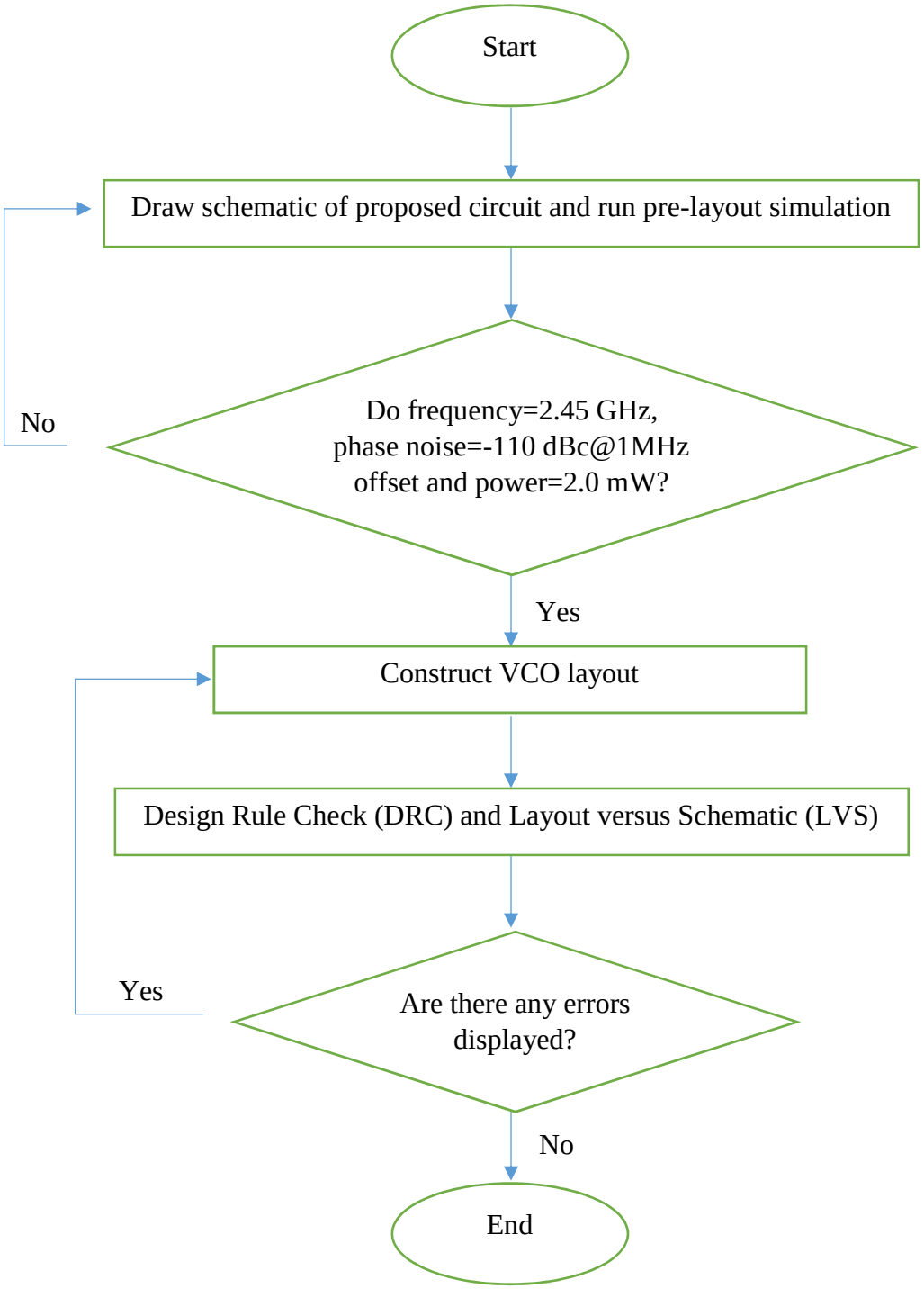


Figure 3.1: (a) Overview of methodology

3.1 Schematic

The proposed schematic is displayed in Figure 3.2. This design is basically the current reuse class-C VCO[10], as previously discussed in Section 2.2, but some

modifications had been done to boost its performance. To reduce the parasitic capacitances, the capacitors at the resonant tank were removed and the varactors were replaced by its passive components, instead of using transistors to construct varactors. Consequently, V_b and the resistors that used to bias the transistors were not needed anymore. Current reuse technique was applied in this design, where the same current had been used in the middle part of it, especially when there were inductor, which shorted DC current, and PMOS transistor in core VCO as current generator. Current flowed from PMOS, passed through inductor and finally reached the source of NMOS transistor in core VCO.

This circuit comprised of three main components: a core VCO and dynamic bias circuits for NMOS and PMOS transistors. The core VCO was built up of a pair of cross-coupled PMOS and NMOS transistors, while two modified current mirrors represented the dynamic bias control circuits. Capacitors (C0, C1) and resistors (R0, R1) built up the class-C structure. Resistors (R2, R3) performed as reference current at the startup stage. Tuneable voltage, V_{tune} controlled the frequency output by varying capacitance of varactors. In the dynamic bias control circuits, the transistors were used to provide same V_G values to the transistors in core VCO. The capacitors (C2, C3) acted as bypass capacitors to filter out V_D noise.

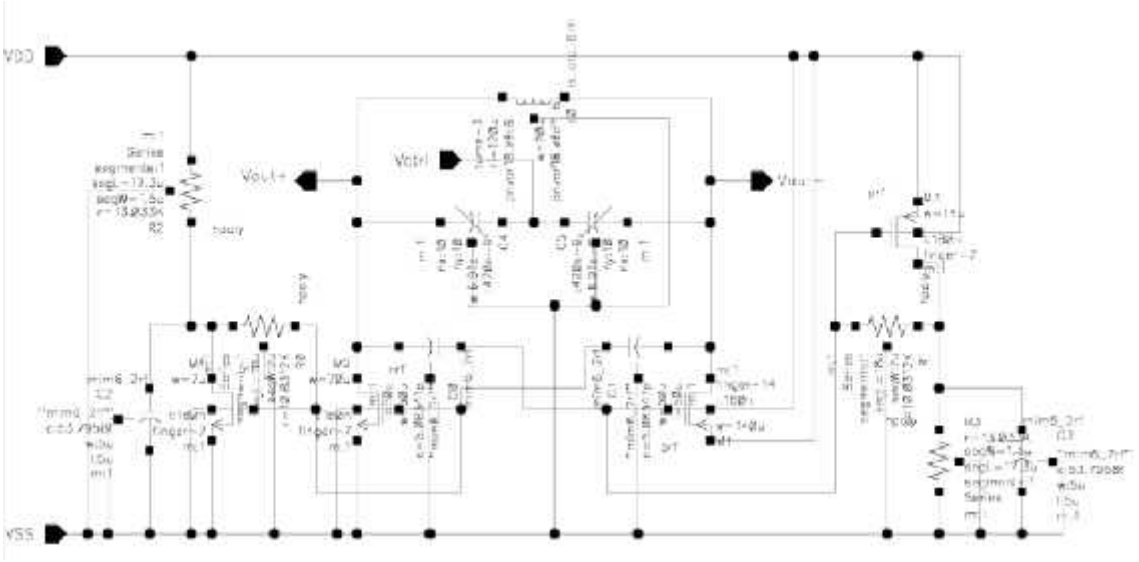


Figure 3.2: Schematic of proposed circuit

3.1.1 Calculations for Each Component

$$I_D = \frac{\mu_n C_o}{2}\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2 \tag{3.1}$$

For current mirror transistor M4:

Using equation (3.1)[15],

$$68\mu = \frac{0.039(9.45 \times 10^{-3})}{2}\left(\frac{W}{0.18 \times 10^{-6}}\right)(0.6 - 0.5)^2$$

$$W = 6.64 \times 10^{-6}\ \mu m$$

Theoretically, the size of PMOS is the double the size of NMOS, as mobility of the PMOS is roughly half of the mobility of an NMOS.

$$I_D = \frac{\mu_n C_o}{2}\frac{W_n}{L}(V_G - V_{th})^2 \tag{3.2}$$

$$I_D = \frac{\mu_n}{2}\frac{C_o}{2}\frac{W_p}{L}(V_G - V_{th})^2 \tag{3.3}$$

Assuming $I_D = I_D$,

$$\frac{\mu_n C_o}{2}\frac{W_n}{L}(V_G - V_{th})^2 = \frac{\mu_n}{2}\frac{C_o}{2}\frac{W_p}{L}(V_G - V_{th})^2$$

$$W_p = 2W_n$$

The current mirror transistor M3 width is:

$$W = 6.64 \times 10^{-6} \times 2 = 13.28\ \mu m$$

Total power dissipation:

$$P = I \quad (3.4)$$

Apply equation (3.2),

$$2.4m = I(1.5)$$

$$I = \frac{2.4m}{1.5}$$

$$= 1.6\,m$$

$$1.6m - 0.068m - 0.068m = 1.464\,m$$

Current at each branch: $\frac{1.4\ m}{2} = 0.732\,m$

$$= 732\ \mu A$$

For NMOS (M2):

Using equation (3.1) again,

$$732\mu = \frac{0.039(9.45 \times 10^{-3})}{2}\left(\frac{W}{0.18 \times 10^{-6}}\right)(0.6 - 0.5)^2$$

$$W = 71.5\ \mu m$$

For PMOS (M1):

$W = 71.5\mu m \times 2 = 143\ \mu m$

Desired frequency = 2.45 GHz. To compute values of inductor (L0) and varactors (C4, C5)[9]:

$$f = \frac{1}{2\pi\sqrt{L}} \tag{3.5}$$

$$2.45 \times 10^9 = \frac{1}{2\pi\sqrt{L}}$$

$$L = 4.22 \times 10^{-2}$$

From the properties in Cadence, inductor (L0, with cell name lct_otc_6lm) $L = 4.54\,n$.

$$4.54n \times C = 4.22 \times 10^{-2}$$

$$C = 0.9295\,p$$

The capacitance of varactors (C4, C5) are calculated as in series, so each capacitance is:

$$C_4 = C_5 = \frac{0.9295p}{2} = 0.4648\,p$$

For resistor R2 and R3:

$$R_2 = R_3 = \frac{1.5 - 0.6}{68\mu} = 13\ k\Omega$$

where 1.5 V is the power supply and 0.6 V is the initial startup voltage at gate terminal, and 68 µA is the reference current.

3.1.2 Component Settings in Cadence

Non-ideal components were implemented in this design since the design will proceed to the layout stage. These components are available in silterraC18G library.

Instead of defining their values, their values were adjusted by modifying their CDF parameters.

3.1.2.1 Inductor

Figure 3.2 represents the properties for the inductor. The target frequency was set to desired frequency of this design, 2.45 GHz. The metal width, number of turns, inner radius and tap width when varied gives differential inductance and differential quality factor. These parameters were adjusted until a maximum value of differential quality factor is obtained.

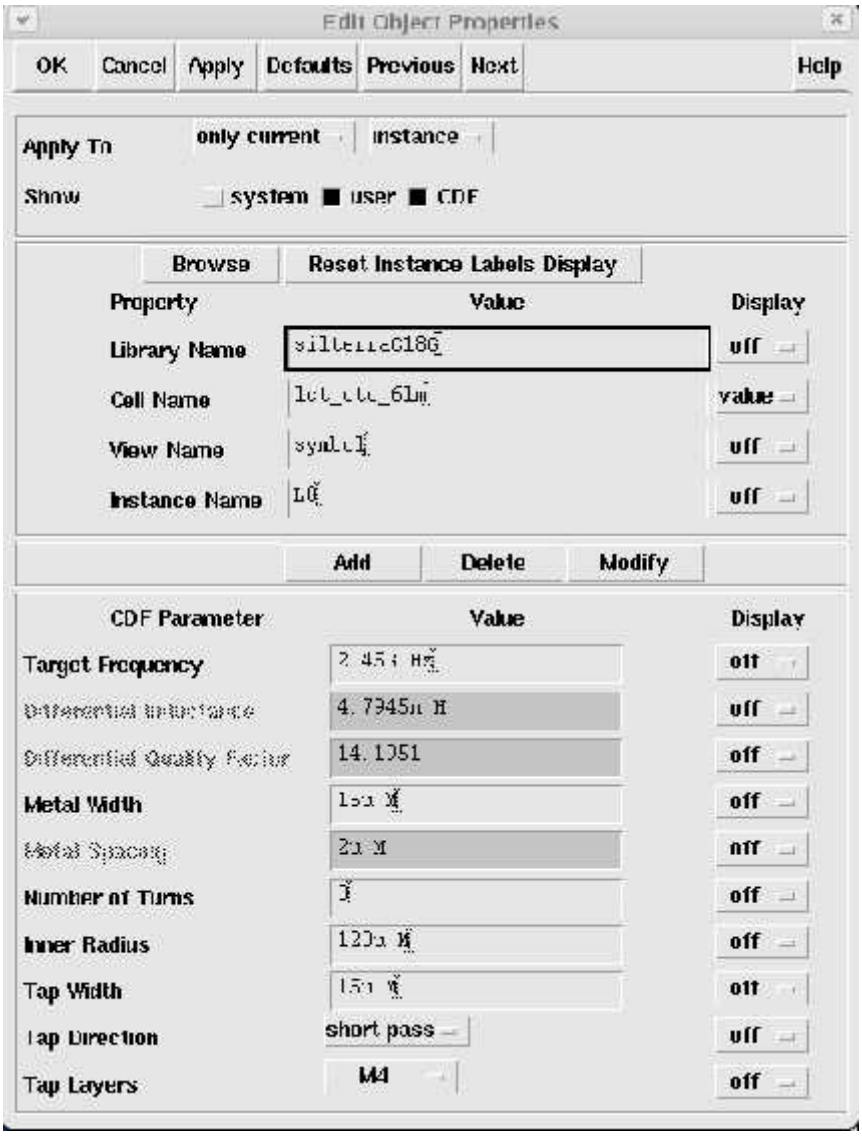


Figure 3.3: Properties of inductor

3.1.2.2 Varactor

In varactor, the allowed multiplier numbers are from 1 until 100. Capacitance of varactor will rise with the increment of multiplier number. Varactor behaves like capacitor, by adding the number of multiplier, the capacitors will be connected in parallel and hence increasing the capacitance. From equation (3.3), the suggested capacitance of each varactor is 0.4648 pF. Thus, the parameters will keep on being adjusted until it reaches approximately the calculated value. Next in ADE, "Results"→ "Print"→ "DC Operating Points" should be clicked, then only varactor was selected to view its capacitance. The setting of varactor properties is shown in Figure 3.3.

To obtain the fundamental frequency of 2.45 GHz, the finger width can be adjusted up to two decimal places. The ranges of finger width and finger length are 5 µm-20 µm and 420 nm-3 µm, respectively, while that of finger in Y (column) and finger in X (row) is 1-25.