DESIGN OF 0.13-µm CMOS LNA WITH FLAT GAIN FOR COGNITIVE RADIO APPLICATION

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by

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LIST OF ABBREVIATIONS

ADE	Analog Design Environment
AC	Alternating Current
CD	Common Drain
CG	Common Gate
CS	Common Source
CR	Cognitive Radio
dB	Decibel
DC	Direct Current
FET	Field Effect Transistor
GPS	Global Positioning System
GHz	Giga Hertz
IIIP3	Third Order Intercept Point
LNA	Low Noise Amplifier
MHz	Mega Hertz
MOS	Metal Oxide Semiconductor
IP1dB	Input 1dB Compression Point
RF	Radio Frequency
SNR	Signal-to-Noise
SP	Scattering Parameter

UWB Ultra-Wide Band Technology

LIST OF SYMBOLS

μ_n	Charge-carrier effective mobility
∞	Infinity
Ω	Ohm
f	Frequency (Hz)
C	Capacitance
C_{gs}	Gate to Source Intrinsic Capacitance
C_s	Source Capacitance
C_{ox}	Gate oxide capacitance per unit area
F	Noise Factor
G_m	Transconductance of MOSFET
I_D	DC drain current
K_f	Stability factor
L	Length
L_C	Shunt-Series Peaking Technique Inductor
L_S	Source Inductance
nH	Nano-Henry
pF	Pico-Farad
Q	Quality Factor

R	Resistance
S_{11}	Input Reflection Coefficient (dB)
S_{12}	Reverse Isolation (dB)
S_{21}	Power Gain (dB)
S_{22}	Output Reflection Coefficient (dB)
V_{ov}	Overdrive Voltage
W	Width
Z_{in}	Input Impedance
Z_L	Load Impedance
Z_0	Characteristic Impedance
Z_S	Source Impedance

REKA BENTUK LNA CMOS 0.13-µm DENGAN DAPATAN RATA UNTUK APLIKASI RADIO KOGNITIF

ABSTRAK

Tesis ini membentangkan reka bentuk penguat hingar rendah (LNA) jalur lebar dengan gandaan tinggi bagi aplikasi ultra-wideband (UWB) dari 300 MHz hingga 10 GHz. Dalam melaksanakan reka bentuk LNA, reka bentuk itu mesti berupaya menyediakan jalur yang lebar dengan gandaan tinggi yang sekata sementara metrik prestasi yang lain dioptimumkan kepada spesifikasi sasaran. Dalam projek reka bentuk ini, LNA menggunakan transistor masukan dengan topologi Get Sepunya (CG) untuk mendapatkan masukan jalur lebar dikaskad dengan topologi transistor sumber sepunya (CS) untuk peningkatan gandaan dan bertindak sebagai penguat arus untuk mengurangkan penggunaan kuasa. Daripada projek sebelum ini, dengan menggunakan topologi yang dicadangkan, penguat hingar rendah jalur lebar 300 MHz hingga 10 GHz diperolehi menggunakan komponen pasif ideal. Dalam penerusan projek ini pula, reka bentuk ditukar daripada komponen pasif yang ideal kepada komponen pasif RF. Perisian cadence Specter RF dengan teknologi proses Silterra CMOS 0.13-µm digunakan dalam simulasi reka bentuk LNA untuk mempamirkan keputusan metrik prestasi LNA yang dicadangkan. Gandaan yang diperolehi berada di atas 10 dB dalam lingkungan 2.4 GHz – 9.2 GHz), S_{11} berada dibawah -10 dB (2.5 GHz - 8.7 GHz), S_{12} juga dibawah sepanjang linkungan frekuensi, -40 dB, S_{22} dibawah paras -10 dB, angka hingar (NF) 5.4-7.2 dB (3 GHz – 7.2 GHz) dengan IP3dB pada -6.47 dBm. Penggunaan kuasa adalah 8.3 mW pada 1.2 V. Pada RF yg telah dioptimumkan untuk frekuensi 300 MHz – 10 GHz, gandaan yang diperolehi berada di atas 10 dB adalah 1.193 GHz - 3.847 GHz, walau bagaimanapun metrik prestasi lain adalah baik seperti S11 -10 dB (732 MHz - 8.03 GHz), S12 di bawah -50 dB, S22-10 dB (476 MHz - 9.82 GHz. Penggunaan kuasa adalah 8.3 mW pada 1.2 V. Berdasarkan keputusan simulasi litar yang telah dioptimumkan, didapati litar dengan komponen pasif RF yang pertama mempunyai prestasi lebih baik bagi operasi 3 GHz – 10 GHz.

DESIGN OF 0.13-µm CMOS LNA WITH FLAT GAIN FOR COGNITIVE RADIO APPLICATION

ABSTRACT

This thesis presents the design of a wide band low noise amplifier (LNA) with high gain for ultra-wideband (UWB) application ranging from 300 MHz to 10 GHz. In implementing the LNA design, the design must able to provide wide bandwidth with high flat gain while the performance metrics optimized to the target specifications. In this design project, the LNA utilizes the input transistor with the Common Gate (CG) topology to obtain wideband input cascaded with a transistor of Common Source (CS) topology for enhancement in gain and act as current amplifier to lower the power consumption. In a previous study, by using the proposed topology, a wideband LNA of 300 MHz to 10 GHz was obtained using ideal passive components. This work is a continuation of the above mention project, whereby the design is converted to using RF components. Cadence Spectre RF software with Silterra's 0.13-µm CMOS process technology is used in simulation of the LNA design to present results of the performance metrics of the proposed LNA. The LNA with RF components achieved gain above 10 dB for the range of 2.4 GHz – 9.2 GHz, S_{11} -10 dB (2.5 GHz - 8.7 GHz), S_{12} below -40 dB, S_{22} below -10 dB and noise figure (NF) is between 5.4-7.2 dB (3 GHz – 7.2 GHz) with IP3dB of -6.47 dBm. The power consumption is 10.1 mW at 1.2 V. As for the RF optimized for 300 MHz -10 GHz, the gain was only achievable at the range of 1.193 GHz - 3.847 GHz, however the other performance metrics shows good result, S_{11} -10 dB (732 MHz - 8.03 GHz), S_{12} below -50 dB for the whole 300 MHz to 10 GHz, S_{22}-10 dB (476 MHz - 9.82 GHz). The power consumption is 8.3 mW at 1.2 V. Based on the results of the optimised circuit, it can be seen that the first circuit with RF components gives better performance for 3 GHz – 10 GHz operation.

CHAPTER 1

INTRODUCTION

1.1 Background Overview

The growth in wireless communication is expanding exponentially over the years where many organizations are attempting to extend the bandwidth of operating frequency. Due to this, ultra-wideband technology (UWB) was introduced. Ultra-wideband (UWB) wireless communication is a revolutionary technology for transmitting large amounts of digital data over a wide frequency spectrum using short-pulse, low powered radio signals. In 2002, the Federal Communication Commission authorizes the use of UWB in 3.1-10.6 GHz, whish intended to provide efficient use of scarce radio bandwidth while enabling high data rate wireless connectivity, longer range, low data rate applications, radar and imaging system

This project is to design a CMOS low noise amplifier (LNA) with flat gain for cognitive radio application.

In receiving radio frequency, LNA is the first stage in all processes. LNA should be able to amplify the signal that it receives with good and adequate gain while producing least noise as it can. Therefore, the performance of the LNA is very crucial as it affects the gain and the noise figure (NF) of the system.

The main target for this project is to obtain a flat gain more than 15 dB with a wide band ranging from 300 MHz to 10 GHz. However, in designing an LNA that is capable to amplify with flat gain over a wideband frequency is quite challenging as there are several parameters that need to be satisfied. In order to meet up to the desired performance, some trade-off will occur at the end. The parameters such as the input and

output reflection (S_{11} and S_{22}), reasonable power gain (S_{21}), good reverse isolation (S_{12}), low NF, low power consumption and possessed good linearity need to be considered in designing an LNA.

1.2 Project Motivation

Nowadays, technology is getting more advanced and more new technology devices are designed for mobility. Therefore, in order to fulfil the demands in communication, many researches on LNA were conducted and due to massive frequency spectrum usage, the development on LNA keeps increasing and their performance are constantly to be optimized.

For an LNA to be considered superior compared to other amplifier, there are several important characteristics of the LNA to be at the optimum state. It is very challenging in designing an LNA that can achieve high gain over a wide bandwidth. For a start, the designed LNA should be able to produce flat gain to avoid signal distortion. Next, the LNA is able to generate high gain while using low power consumption.

Although there are many researched topologies available for the LNA, it is important to choose the most suitable topology for UWB LNA as each of the topology has it merits and demerits as trade-offs between the metrics. Thus, detailed investigation is made among the suitable topologies for the UWB LNA.

1.3 Problem Statements

To get optimum RF receiver, the design LNA specification must achieved the maximum value it can afford. However, it is known that to achieved the desired specification, some compromise must be made as to the trade-off between the performance metrics is unavoidable.

Based on the work by Zulhilmi (2016), the CG stage cascade with CS stage is implemented was able to provide good input and output matching across the whole 4 GHz to 12 GHz frequency range as the design can be easily match with 50 Ω. The design was able to achieve high flat gain for more than 18 for the above mention frequency and the NF is lower than 5.8 dB within the bandwidth. It is important to obtain such a high flat gain at high bandwidth.

However, in this project the design must be able to support wider bandwidth ranging from 300 MHz to 10 GHz and all of the designed component are in spectreRF. It is a huge advantage to be able to design an LNA that is able to be utilized across wider bandwidth with adequate high flat gain and as low NF as possible.

1.4 Objectives

a) To design an LNA for cognitive radio application which provide ultra-wideband operation.

b) To obtain high flat gain at wideband operation ranging from 300 MHz to 10 GHz.

c) To study the effect of the use of RF components in the LNA design.

1.5 Project Scope

This design is focused on UWB LNA that can operate from 300 MHz o 10 GHz with flat gain with all components used from the RF library. The design has the input transistor connected to the Common Gate (CG) in controlling the input matching supervene by a Common Source (CS) transistor in charge of controlling the gain of the design and finally a Common Drain (CD) transistor that act as buffer which help to fulfil the output impedance matching. This project will not cover the post-layout simulation because the only concern is up to pre-layout simulation due to cost and time constraints. The performance of proposed LNA topology will be compared with similar work by others.

The proposed wideband LNA after much detailing is to be operated from 300 MHz to 10 GHz following the frequency range applicable for UWB operation. The gain should be above 10 dB the least and as flat as possible throughout the specified frequency range. As the LNA will commonly be used in mobile application, it is preferable for its power consumption to be low as possible. The instrument in designing the schematic is by using Silterra's 0.13 μm CMOS Process Technology and simulated using Cadence Spectre RF.

1.6 Thesis Outline

This thesis consists of five chapters and starts with an introduction in Chapter 1. The first chapter describes the overview, problem statements, objectives, project scope and organization of the thesis.

In Chapter 2, are explained about the theories and equations related to the design and analysis of the LNA are explained. The design topologies and comparison with work by others are dissertate in this chapter. Also included in this chapter is the explanation on the performance metrics, linearity, NF and work by others in similar area.

Chapter 3, is on the methodology in designing the LNA. The topology used in this work is the CG structure as the input stage supervene by a CS transistor that serves as current reuse technique which helps in reducing the power consumption. Lastly, at the output, a CD transistor was used to drive 50 Ω output impedance. Circuit Optimization to obtain the best performance for each performance metric is also elaborated in this chapter. The component which contribute most to the performance metric is identified and relate to the theory or equation concerned.

CHAPTER 2

LNA FUNDAMENTALS AND LITERATURE REVIEW

2.1 Background

This chapter will describe the performance metrics of an LNA and some literature review on similar work by other in term of LNA design and. The performance metric includes Scattering Parameter or S parameter which are commonly used in RF and microwaves amplifier analysis as well as P1dB, power consumption and most importantly the noise figure (NF).

2.1.1 Low Noise Amplifier (LNA)

A low noise amplifier (LNA) is an electronic amplifier that amplifies a very low-power signal without significantly degrading its signal-to-noise ratio. LNAs are designed to minimize the additional noise when amplifying occur as it amplified the signal while at the same time the noise. In designing to minimize the noise, consideration of trade-offs must be included such as impedance input matching, technology of CMOS and low-noise biasing condition.

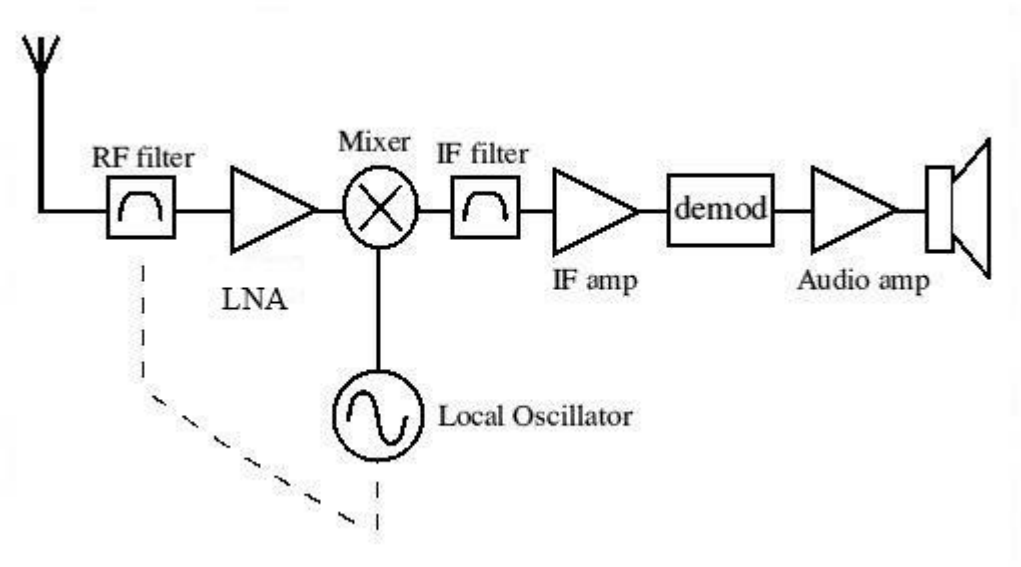

Figure 2.1 Block Diagram of RF Receiver

RF receiver transforms all incoming carrier signals to a common intermediate frequency (IF) where the signals are amplified using common tuned amplifiers. The RF filter act as a bandpass filter to discriminates against image and intermediate frequency signal and provides amplification in the LNA section. The is then signal multiplied with the local oscillator signal in a mixer to change the carrier frequency to the predetermined intermediate frequency. However, in this work only covers till LNA section.

2.1.2 LNA Performance Metric

In designing UWB LNA, the achievement of the performance metric is of utmost importance and the design has to achieve the desirable specification. The general performance metrics are elaborated as below:

- Gain

Gain is the increase of power of a signal from the input to the output. A high consistent gain but stay across the frequency bandwidth of the system is required.

- Frequency

A wide range of frequencies is preferable especially for LNA in cognitive radio and for UWB application. For this work, the frequencies in use range from 300 MHz to 10 GHz

- Supply Voltage

The supply voltage should not exceed the specification determined for the CMOS technology used. Which is maximum of 1.2 V for this CMOS technology

- Linearity

A relationship of input power to output power. Higher linearity ensures the LNA can maintain a linear operation to minimize the intermodulation distortion.

- Noise Figure (NF)

NF is the degradation of the signal-to-noise ratio (SNR) which lower values indicate better performance. The LNA must be robust to noise as it dominates the overall receiver noise. This is obtained by low NF.

- Power

The LNA with lesser power consumption is most desirable to prevent excessive energy waste. For example, 10 mW is much more preferred compared to 20 mW as lower power consumption is better.

a) Scattering Parameter (SP)

S-parameter are regularly utilized in circuit analysis of RF and microwave. The incident, reflected and transmitted waves that provide a complete description of the network seen at *N* ports of the system are represented by the S parameter. This can be seen in Figure 2.2

Figure 2.2: Two-port network (Azizan and Zainol Murad. 2005)

Based on Figure 2.2, a_1 and b_1 can be related to the port voltage of v_1 and v_2 and the current of i_1 and i_2 as below:

$$a_i = \frac{v_i^+}{\sqrt{Z_o}} \tag{2.1}$$

$$b_i = \frac{v_i^-}{\sqrt{Z_o}} \tag{2.2}$$

Where a_i represents an incident wave and b_i represents a reflected wave from the port (Pozar, 2011). The overall voltage and current at the *i*-th port can be written as in Equation (2.3) and (2.2).

$$v_i = v_i^+ + v_i^- \tag{2.3}$$

$$i_i = i_i^+ + i_i^- = \frac{1}{Z_o}(v_i^+ + v_i^-) \tag{2.4}$$

Substituting Equation (2.3) and (2.4) into Equation (2.1) and (2.2) yields Equation (2.5).

$$v_i = v_i^+ + v_i^- = \sqrt{Z_o}(a_i + b_i) \tag{2.5}$$

$$i_i = \frac{1}{Z_o}(v_i^+ + v_i^-) = \sqrt{\frac{1}{Z_o}}(a_i + b_i) \tag{2.6}$$

From Equation (2.5) and Equation (2.6), the a1and b1 can be expressed as below.

$$a_i = \frac{v_i^+}{\sqrt{Z_o}} - b_1 \tag{2.7}$$

$$b_i = a_i - i_i\sqrt{Z_o} \tag{2.8}$$

Substituting the Equation (2.7) into the Equation (2.8), yields Equation (2.9).

$$2a_i = \frac{v_i^- + Z_o}{\sqrt{Z_o}} \tag{2.9}$$

Equation (2.9) also yield the Equation (2.10) and (2.11).

$$a_i = \frac{v_i + i_i Z_o}{\sqrt{Z_o}} \tag{2.10}$$

$$b_i = \frac{v_i - i_i Z_o}{\sqrt{Z_o}} \tag{2.11}$$

Where the value of *i* is corresponding to the port number, Z_0 is known as characteristic impedance which is purely resistive and has a standardized impedance value of 50 Ω in most of the RF circuit design. The matrix form also can be used to symbolize the two ports relation as in Equation (2.12). Equation (2.13) and Equation (2.14) are obtained from the given matrix.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.12}$$

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.13}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.14}$$

All of the equations have been simplified and each of them are related between the reflected and incident waves at the network ports 1 and 2. In order for load impedance ZL to be equal to Z_0 (Z_L=Z_0), input port driven together with the output port should be terminated by Z_0. Meanwhile a_2 is set equal to zero. This enables the value for S_{11} and S_{21} to be obtained, i.e. (Adhyaru, 2007) as shown in Equation (2.15) and Equation (2.16) respectively.

$$b_1|_{a_2=0} = S_{11}a_1$$

$$s_{11} = \frac{b_1}{a_1} \tag{2.15}$$

$$b_2|_{a_2=0} = S_{21}a_1$$

$$s_{21} = \frac{b_2}{a_1} \tag{2.16}$$

The same method can be used to obtain $Z_S = Z_0$, where the output port is driven together with the input port ad being terminated by Z_0. At the same time, the value of a_1 is set to zero ($a_1 = 0$) in order to determine the value of S_{12} and S_{22} as shown in Equation (2.17) and Equation (2.18) respectively.

$$b_1|_{a_1=0} = S_{12}a_2$$

$$s_{11} = \frac{b_1}{a_2} \tag{2.17}$$

$$b_2|_{a_1=0} = S_{22}a_2$$

$$s_{22} = \frac{b_2}{a_2} \tag{2.18}$$

Based on the statements mentioned, it is clear that for the input and output port to be matched, the value of $a1$ and $a2$ should be equivalent and this only happens when Z_S =Z_0 and Z_L=Z_0. The S-parameters are defined in equation below.

$$\boldsymbol{S_{11}} = \frac{\boldsymbol{b_1}}{\boldsymbol{a_1}}\Big|_{\boldsymbol{a_2=0}} \qquad (2.19) \qquad\qquad \boldsymbol{S_{21}} = \frac{\boldsymbol{b_2}}{\boldsymbol{a_1}}\Big|_{\boldsymbol{a_2=0}} \qquad (2.20)$$

$$\boldsymbol{S_{12}} = \frac{\boldsymbol{b_1}}{\boldsymbol{a_2}}\Big|_{\boldsymbol{a_1=0}} \qquad (2.21) \qquad\qquad \boldsymbol{S_{22}} = \frac{\boldsymbol{b_2}}{\boldsymbol{a_2}}\Big|_{\boldsymbol{a_1=0}} \qquad (2.22)$$

S_{11} = power reflected from the input / power incident on the input

S_{12} = power delivered to the load / power available at the source

S_{21} = reverse transducer power gain with Z_o load and source

$S_{22.}$ = power reflected from the input / power incident on the output

Each of the S parameter can be explained with S_{11}, the input return loss which is defined as the ratio of the reflected voltage wave to the incident voltage at the input port with load impedance matched to Z_0. S_{21} is known as forward transducer power gain as it is the ratio of the reflected voltage wave at the output port to the incident voltage applied at the input port, provided the output port termination in Z_0 b. S_{12} is known as reverse isolation as it is the ratio of the reflected wave at the input port to the incident voltage wave at the output port, provided the input port termination in Z_0. S_{22} is the output return loss that is described as the ratio of the reflected voltage wave to the incident voltage wave at the output port, with the source impedance, Z_S matched to Z_0.

S-parameters are commonly expressed in the unit decibel (dB) as shown by Equation (2.23).

$$S_i(dB) = 20log_{10}S_{\mathrm{I}} \tag{2.23}$$

Where *i* represent by 11, 12, 21, and 22. The typical value of S-parameters for LNA are S_{11} and S_{22} <-10 dB, S_{21} > 10 dB and S_{12} < -40 dB (Molavi, 2005), which may vary according to the application. Having a magnitude of 10 dB for S_{11} and S_{22} in most RF design is considered to be sufficient. Based on performance characteristic of RF and microwave transistor in (Pozar, 2011), the typical gain value for CMOS transistor is 10 dB to 20 dB. A good amplifier should possess a large S_{21} to achieve high gain, small S_{11} and S_{22} to possess good input and output matching, and small value of S_{12} to ensure stability and reverse isolation.

b) Noise Figure (NF)

Noise Figure (NF) is defined as the ratio of the total output noise power to the output noise due to the input source (Swamy, 2013). Namely, there are several types of noise mentioned in (Pozar, 2011) which is thermal noise, shot/quantum noise, burst noise and flicker/pink noise.

Thermal noise will only be generated from resistor in any circuits that implemented the use of resistors, capacitors and inductors.

Noise Figure can be calculated by using equation (2.24) and expressed in decibel (dB). By using this, an LNA noise performance can be calculated.

$$NF = 10log_{10}F \tag{2.24}$$

The noise factor (F) defined by Leach (1994) is measurement for the degradation of the signal-to-noise (SNR), caused by component in a RF signal chain:

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.25}$$

Whereby, SNR at the input and output are defined as (Molavi et.al,2005):

$$SNR_{in} = \frac{Signal}{Noise_{in}} \tag{2.26}$$

and

$$SNR_{out} = \frac{Signal}{Noise_{out}} \tag{2.27}$$

c) Linearity

Linearity is an essential performance metric for designing LNA. The common parameters to measure the linearity are usually the input 3rd orders intercept point (IIP3) and the 1dB compression point (P1dB)

i. 1-dB Compression Point

P1dB is a power measurement of the input signal which is at 1 dB below the nominal value. As shown in Figure 2.3, it is indicated that the gain is equal to line slope. At one point, the gain of the amplifier starts to enter compression region where there is no further output power increment even though more input power is fed. This indicates

that at the compression region, flat gain can be seen as the amplifier becomes saturated and the response becomes non-linear, resulting in distortion in the signal itself.

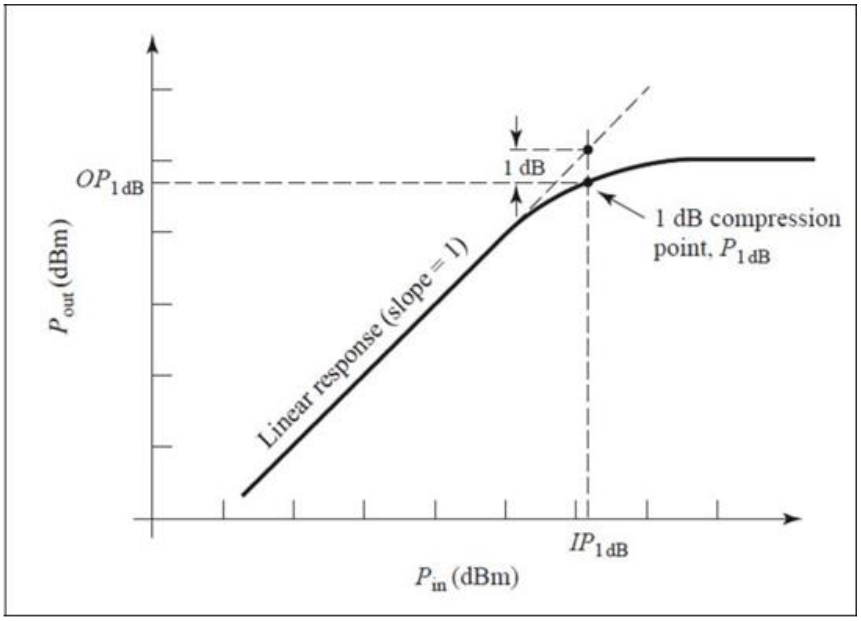

Figure 2.3: 1-dB compression point (Pozar, 2011)

ii. Third-Order Intercept Point

Figure 2.4 shows the input power level, IIP3, which determines the power of the input when the power of 3rd order power is equal to the power of 1st order output. The size of the amplified signal can be measured by the value of intercept point (IP3) indicated before intermodulation distortion (IMD) occurs. Maximum output power that can be produced by an LNA before the process of signal degradation is represented by output intercept point (OIP3).

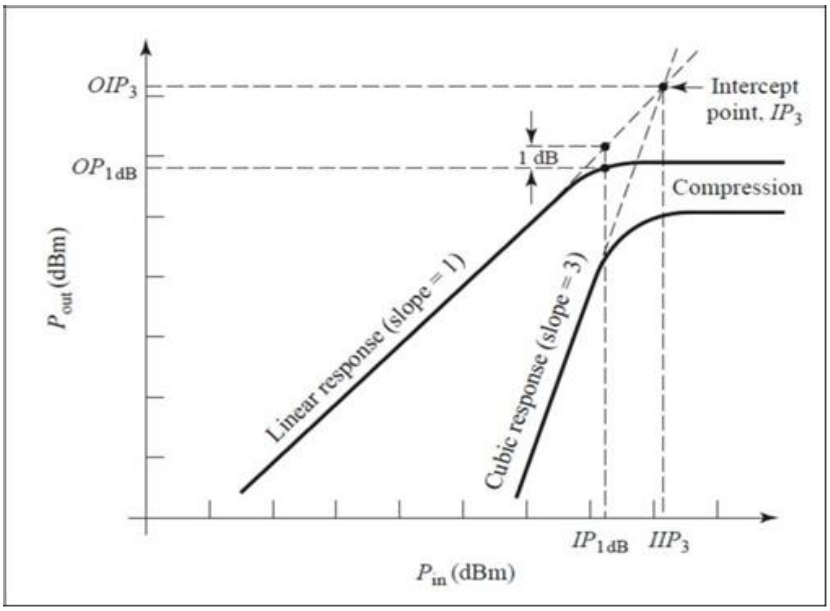

Figure 2.4: Third-Order Intercept Point (Pozar, 2011)

iii. P1dB vs IIP3

In designing LNA, IIP3 is much more important than P1dB because IIP3 gives the designer the idea on how large the amplifier can handle. The higher the IP3 than the P1dB, lesser the amplifier will be distorted

2.2 Literature Review

There are various types of topologies of LNAs which are available and had been improved in time by researchers and the industries in accordance with the advancement of technology. In designing this LNA, focus will be of the technology only in improvement of the design and with respect to its gain performance while other performance metrics are kept to its specifications.

Five different designs have been selected as references to compare on their LNA performances which are Liao (2005), Mirvakili (2009), Pourjahafarian and Mafinezhad (2015) and Zulhilimi (2016), as shown in Table 2.3.

Table 2.3: Comparison of LNA performance. (Zulhilmi, 2016)

Performance metrics	Liao (2005)	Mirvakili (2009)	Pourjahafarian and Mafinezhad (2015)	Zulhilimi (2016)
Topology	Noise Cancelling LNA	Noise Cancelling LNA	CG cascode with CS topology	CG cascode with CS topology
Bandwidth (GHz)	3.0-10.6	4.7-11.7	2.7-10.6	3-10
S_{11} (dB)	<-10	<-11.9	<-10.24	<-10
S_{21} (dB)	<10	12.4	11.2-14.8	13.75-19.23
Power (mW)	20	13.5	13.5	10.20
CMOS Technology Process (nm)	180	130	180	130
NF	4.5-5.0	2.88-3	3.12-4.3	4.65-5.33
IIP3 (dBm)	-	-3	-3	-6.78

*Measurement of IIP3 at 6GHz

Assessing each topology, they all provide different value for the performance metric such as gain, bandwidth, NF, power consumption. Based on Table 2.3 from the work Pourjahafarian and Mafinezhad (2015) and Zulhilmi (2016) which both using the CG cascode with CS topology but different CMOS technology. It can be seen that both obtained high gain, low NF and the power consumption of LNA is reasonable. As

known from the power equation that the higher the current, the higher is the power consumed. Hence, this is the trade-off between gain and power consumption as the design must possessed the minimum power supply to be able to amplify.

$$\mathbf{P = IV \ \ OR \ \ P=I^2R} \qquad (2.28)$$

2.2.1 Circuit Topologies

Commonly, Common Gate (CG), Common Source (CS), noise cancelling technique, resistive feedback and inductive degeneration are widely used to meet the wideband amplifiers specification. The following topologies are suitable for bandwidth ranging to a few Gigahertz. Several techniques of UWB LNA will be review in this section.

All electronic devices conducting electricity will generate noise. Therefore, in order to reduce the noise, circuit in Figure 2.7 is implemented. This circuit consists of two stages which are the CG topology at the first stage and the CS as the second stage. At the first stage, the CG topology provides high gain and wideband input matching. However, in increasing the range as the bandwidth increases the NF also becomes high. Thus, CS is implemented at the second stage to cancel out the noise. Figure 2.5 to 2.9 shows several designs works by others in similar area.

i. Noise Cancelling LNA

a)

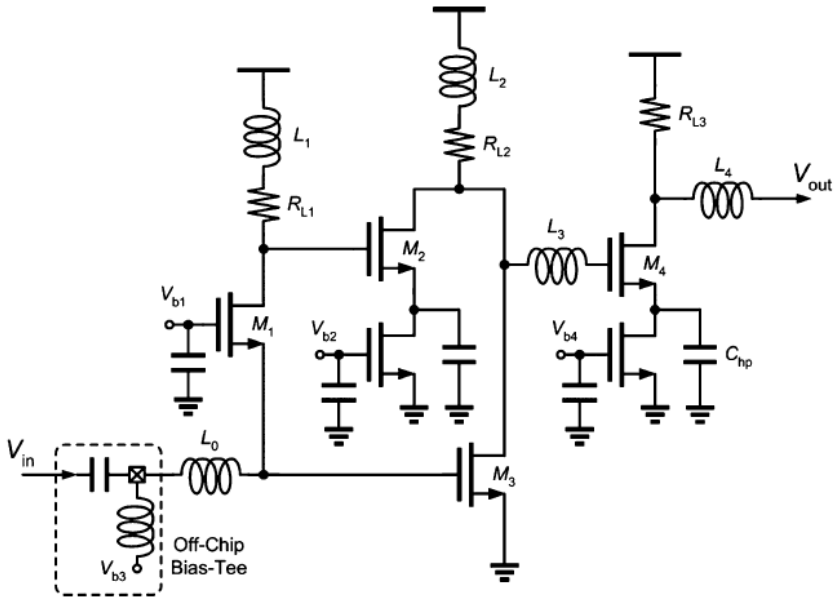

Figure 2.5: Liao (2005)

The input stage incorporates a common-gate topology to facilitate ease of matching. The inductor L_o and parasitic capacitance of M1 and M3 form an LC ladder structure. The noise of M1 is cancelled by M2 and M3 and the noise current due to M1 flows in opposite directions when combined at the drain of M2 and M3. Inductors L_1, L_2, and L_3 roles were extending the bandwidth of the circuit. Transistor M4 which connected to C_{hp} filters out low frequency below 3 GHz by forming high-pass g_m.

The overall performance of this circuit dependent on the two stages. The size and bias of R_{L1}, L_o and L_1 determined the effect of noise cancelling and the noise figure of this LNA,

b)

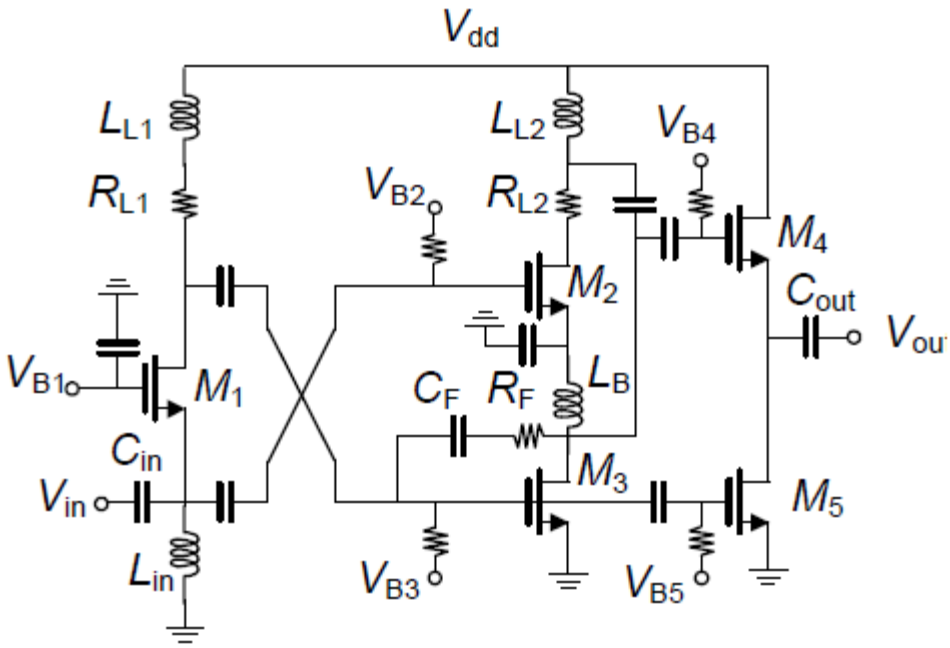

Figure 2.6: Mirkavili (2009)

L_{in} is used to eliminate the degrading effect of the gate-source capacitances of transistor M_1 and M_2. The deviation of input impedance of common-gate amplifier from the conventional $1/g_m$ due to low output resistance of the transistor provides useful isolating conditions of the input matching with noise cancellation.

Noise cancelling technique was used in this design. The noise of the input transistor after gone through transistor M_2 and M_3 was cancelled at the output while, the input signal is amplified.

ii. Common-G cascode with Common-Source

a)

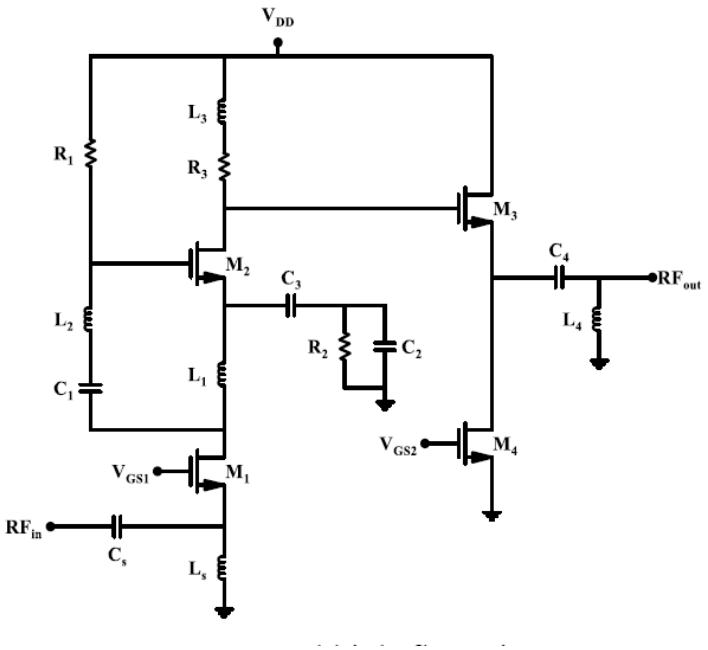

Figure 2.7: Pourjahafarian and Mafinezhad (2015)

The LNA consist of common-gate stage M_1 and common-source M_2. The input common-gate stage provides an input matching and common-source stage amplifies gain. Current-reused technique and cascaded topology used reduces power consumption. Output buffer cascaded with second stage combines gain of lower frequency and higher frequencies to extend ultra-wide bandwidth. A current source, M_4, provides bias current for M_3 and R_1 provides dc bias for M_2.

R_2 in the circuit provides the output impedance of M_1 increased thus, first stage gain is decreased and noise is lowered. The noise figure of the proposed LNA is affected by the input CG stage. C_3 prevents current flow to R_2 therefore, power consumption was not increased. The importance of L_3 was that it provides flat gain by resonating at high frequencies.

b)

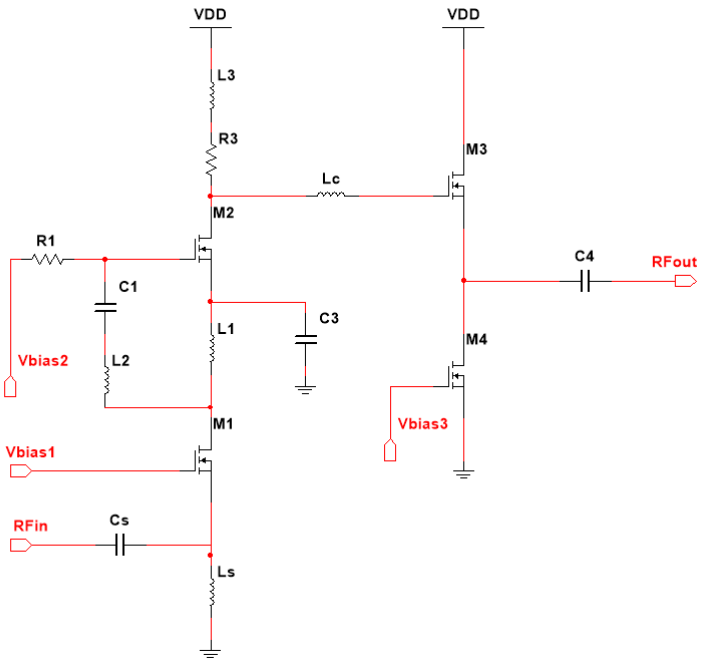

Figure 2.8: Zulhilmi (2016)

The LNA design from Zulhilmi adopted from Pourjahafarian and Mafinezhad (2015) design. The design consists of common-gate stage M_1 and common-source M_2. The input common-gate stage provides an input matching and common-source stage amplifies gain. Current-reused technique and cascaded topology used reduces power consumption. Output buffer cascaded with second stage combines gain of lower frequency and higher frequencies to extend ultra-wide bandwidth. A current source, M_4, provides bias current for M_3 and R_1 provides dc bias for M_2.

R_2 and C_2 were removed as it presence were not affecting the result of the throughout the process. New biased voltage source provided to M_2 as it will have its own independent power source.

2.2.2 Ideal passive component

Ideal passive component is a component that is available in the Cadence software library which its model information was set to ideal. Every simulation that were done in ideal cannot be accepted in the industry as components are never ideal and need to be done in RF simulation.

2.2.3 RF passive component

RF passive component is a component that was provided by Silterra's model library which contains the parasitic information of the components that currently being used in the industry. Thus, this will be brings us to a new understanding of the effects of RF components compared to the ideal component to the design.