Design of 0.13-um CMOS Low Noise Amplifier with Enhanced Input Matching Performance and Flat Gain for Cognitive Radio Application

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TABLE OF CONTENT

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CR	Cognitive Radio
CS	Common Source
dB	Decibel
DC	Direct Current
GHz	Giga Hertz
IIP3	Third Order Intercept Point
IP1dB	Input 1-dB Compression Point
LNA	Low Noise Amplifier
MHz	Mega Hertz
NF	Noise Figure
NMOS	N-Channel MOSFET
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
SP	Scattering Parameters
UHF	Ultra High Frequency
UWB	Ultra wideband
WPAN	Wireless Personnel Area Network

LIST OF SYMBOLS

Ω	Ohm
$\bar{I}^2_n$	Thermal Noise
γ	Noise Factor
A_v	Voltage Gain
C_{gd}	Gate to Drain Intrinsic Capacitance
C_{gs}	Gate to Source Intrinsic Capacitance
K_f	Stability Factor
g_m	Transconductance
S_{11}	Input Reflection Coefficient
S_{12}	Reverse Isolation
S_{21}	Power Gain
S_{22}	Output Reflection Coefficient
Z_{IN}	Input Impedance
Z_L	Load Impedance
Z_0	Output Impedance
Z_S	Source Impedance

Reka bentuk 0.13-um CMOS Penguat Hingar Rendah dengan Prestasi Padanan Masukan yang Dipertingkatkan dan Gandaan Rata untuk Aplikasi Radio Kognitif

ABSTRAK

Teknologi UltraWideband (UWB) adalah teknologi yang sangat berkesan dengan kadar penghantaran data yang besar pada jalur frekuensi 3.1-10.6GHz dengan penggunaan kuasa minimum. Penguat hingar rendah (LNA) biasanya merupakan peringkat pertama penerima yang prestasinya sangat mempengaruhi prestasi penerima keseluruhan. Dalam sistem Radio Kognitif (CR) UWB, LNA mesti memenuhi keperluan angka hingar (NF) yang rendah, gandaan kuasa tinggi, dan kerugian pulangan yang tinggi, serta penggunaan kuasa yang rendah merentasi jalur lebar yang sangat luas. Tesis ini membentangkan reka bentuk UWB LNA dengan topologi suap balik keberintangan dan litar induktif merosot. Tumpuan adalah diberikan kepada padanan masukan, S_{11} dan mengoptimumkan LNA untuk prestasi yang lebih baik merentasi jalur lebar untuk topologi tersebut. Kesan komponen RF pasif pada LNA juga difokuskan dan dibincangkan dalam tesis ini. LNA direka dalam teknologi proses CMOS 0.13-µm Silterra dan simulasi pra-bentangan dilaksanakan dengan menggunakan Cadence SpectreRF. Pengoptimuman LNA dijalankan menggunakan analisis parametrik Cadence. Pengoptimuman dibuat pada komponen yang dihipotesiskan untuk menyumbang paling banyak kepada prestasi S_{11} dan juga kepada prestasi LNA keseluruhan. Langkah akhir projek ini adalah mengoptimumkan LNA dengan komponen RF pasif untuk prestasi terbaik dalam topologi ini. Reka bentuk ini mencapai gandaan kuasa paling tinggi 17.67 dB, NF terendah <3.36dB, S_{12} <-49 dB, S_{22} <-10 dan K_f> 1 dalam jalur lebar operasi 300 MHz-10GHz.. S_{11} reka bentuk ini mencapai nilai di bawah <-10 dB bagi julat frekuensi 4.2 GHz -10 GHz. Reka bentuk ini dapat mencapai nilai IIP3 -10.86 dB manakala nilai IP1dB ialah -17.93 dB pada 2 GHz dalam simulasi pra-bentangan. Penggunaan kuasa adalah 9.6 mW dengan 1.2V bekalan voltan. Perlakuan ini menunjukkan bahawa reka bentuk itu mampu mencapai semua objektif yang ditetapkan untuk projek ini.

Design of 0.13-um CMOS Low Noise Amplifier with Enhanced Input Matching Performance and Flat Gain for Cognitive Radio Application

ABSTRACT

Ultrawideband (UWB) technology is very effective technology with huge data transmission rates over 3.1-10.6GHz frequency band with minimum utilization of power. Low noise amplifier (LNA) is typically the first stage of a receiver whose performance greatly affects the overall receiver performance. In UWB Cognitive Radio (CR) system, the LNA must satisfy stringent requirements of low noise, high gain, and high linearity, as well as low power consumption over a very wide bandwidth. This thesis presents the design of UWB LNA with resistive feedback and inductive degeneration for the frequency of 300MHZ-10GHz. Focus given on improving the input matching, S_{11} and optimizing LNA for better performance across the wideband for the respective topology. The effects of passive RF components on LNA were also investigated and discussed in this work. The LNA was designed in Silterra's 0.13-µm CMOS process technology and the pre-layout simulation were executed using Cadence SpectreRF. The LNA optimization are conducted using Cadence's parametric analysis. The optimizations were made on the components that are hypothesized to contribute most to the S_{11} performance and to the overall LNA performance as well. Final steps of this project were on optimizing the LNA with passive RF components for best performance in this topology. This design can achieve gain as high as 17.67 dB, lowest NF of 3.36dB, $S12$<-49 dB, S_{22} <-10 and Kf > 1 within the desired bandwidth. The S_{11} of this design achieved value below <-10 dB for 4.2 MHz-10 GHz frequency. This design is able to achieve IIP3 of -10.86 dB while the value of IP1dB is -17.93 dB at 2 GHz in pre-layout simulation. The power consumption of the LNA is 9.6 mW with 1.2V voltage supply. These performances indicate that the design is able to achieve all the objectives set for this project.

Chapter 1

Introduction

1.1 Introduction

Cognitive Radios are smart communication systems that were introduced to overcome the problem of saturated frequency spectrum in wireless communication. CR is the solution to the inefficient frequency management in traditional communication systems. The transmitter and receiver can intelligently detect which communication channels are available in wireless spectrum and instantly move into vacant channels while avoiding occupied ones. This will optimize the use of available radio-frequency (RF) spectrum while minimizing interference to other users. Meanwhile, Ultra-wideband (UWB) is a transmission technique that uses pulses with a very short time duration across a very large frequency portion of the spectrum [1]. It is a new wireless technology capable of transmitting data over a wide spectrum of frequency bands from 3.1-10.6GHz with very low power and high data rates and even at very low cost [2]. Specifically, it is imagined to replace every single cable network at home or in an office with a remote association that highlights several megabits of information for every second [1][2]. As the requirement of UWB are high, the interest in designing appropriate UWB devices has gradually increased over the years. Among the UWB Low Noise Amplifier (LNA) architecture proposed so far in CMOS technology, distributed amplifiers can realize the gain-band width product (GBW) very close to device ft, but it occupies very large chip area and consumes very high power [2]. Particularly, the beneficiary part has come in the vital point of consideration and lately, numerous of UWB front-end have been designed.

1.2 Research background and Motivation

It is realized that the performance of the RF receiver is altogether affected by the LNA. Filling in as the principal dynamic amplification block in the accepting way, LNA amplifies the received signal from the transmitter through atmospheric medium. The signal received by an antenna is weak due to the interference of other signal and the distance between transmitter and receiver. This makes LNA an important device in the front end of telecommunication system

as it amplifies the received signal while adding little noise to it. LNA is placed at the front-end of a radio receiver circuit whose noise performance decides the noise of entire receiver. The noise of all subsequent stages reduces by the gain of LNA, while noise of LNA itself is injected into the received signal. A good LNA can be produced by applying a suitable matching network located on the input and output to prevent the signal from reflecting back and fourth between the LNA and antenna [2].

Cognitive radios are smart Radio Frequency (RF) communication system that senses the RF spectrum which allocates a less crowded spectrum to the user abstaining the interference of other spectrum users. Cognitive radios pose challenges at all levels of abstraction. The receive signal path of a cognitive radio must deal with issues like broadband characteristics, flat noise figure (NF) and gain, and adequate input matching and high linearity [1]. Moreover, UWB LNA suffers many interferers from co-existing systems like WLAN and Bluetooth. This condition requires the LNA linearity must be considered as important as its noise performance.

Design of a UWB front end LNA involves many challenges and performance trade-offs. As the LNA acts as the critical block in the receiver, the challenges such as good wideband input matching, sufficient gain to suppress noise from the subsequent stages, low NF, stability and high linearity and most importantly low power consumption [3].

1.3 Problem statement

Several challenges are often encountered in designing of LNA such as the wide-band input matching to minimize the return loss, flat and high gain to suppress the noise, low noise figure (NF) to enhance receiver sensitivity, low power consumption and small die area to reduce the cost. However, it is impossible to design LNA without the trade-offs between its performance metrics [2].

In this project, cascode resistive shunt feedback with inductive degeneration LNA topology has been initially designed to improve the gain, noise figure (NF) and stability. Futhermore, this topology makes better gain over the broadband frequencies such as in UWB range. However, this proposed topology burns a lot of power and optimization is needed to reduce the overall power consumption [3].

Previous works on the design of the LNA indicates relatively low performance in term of its S-parameters where the return loss (S_{11}) parameter did not achieve less -10dB for the wide bandwidth of 300MHz to 10GHz. This has affected the entire performance and other parameters of the LNA as well. Thus, this work would highlight the design challenges and performance of LNA design and the effects of using the real components (RF) in the LNA design for greater wideband of a resistive shunt feedback with inductive degeneration topology. Other than that, the design of LNA is expected to meet certain specifications such as sufficient gain and low power consumption as well in accordance with the design specification.

1.4 Objectives

i) To obtain the input return loss, S_{11} of a resistive shunt feedback with inductive degeneration LNA topology less than -10 dB.

ii) To optimize the gain, noise figure, linearity and power consumptions of the LNA to fulfil the design specification.

iii) To implement the passive RF components in the resistive shunt feedback with inductive degeneration LNA topology.

1.5 Project scope

In this project, the focus is to design a resistive shunt feedback with inductive degeneration UWB LNA that operates from 300 MHz to 10 GHz with flat gain and enhanced performance metrics. The LNA is designed to meet the specifications set and will be optimized to produce the best performance for this LNA topology. Next, the LNA design will be simulated using the passive RF components and their effects are studied while simultaneously upholding the design specification. The schematic design is to be conducted using Silterra's 0.13 um CMOS Process Technology and simulated using Cadence Spectre RF. The execution of proposed LNA topology will be compared with work of others. This work will not cover the post-layout. Simulation as the main concern is until pre-layout simulation because of cost and time imperatives.

1.6 Thesis Outline

There are 5 chapters in this thesis.

Chapter 1 introduces project's background and overview, the problem statements, the objectives, brief explanation on the scope of this research and presents the organization of the thesis.

Next in Chapter 2, it describes the background related to the design and analysis of LNA. The design topologies, techniques by others and covers about the limitation in previous researches in this research area. The target specification is then set based on the related literature review carried on.

In Chapter 3, the procedures involved in designing the LNA are explained in detail. Generally, this chapter presents the overall process sequence related to the design of the LNA. The design methodology process and circuit analysis are presented and the optimization strategy used to get best performance are discussed in this chapter.

In Chapter 4, the simulation result for the schematic design are presented and analysed. The acquired data from the result will be followed by explanation and discussion with the help of figures and tables. The performance of this work is then compared with the previous work by others and discussed.

Finally, Chapter 5 demonstrates the conclusion of the finding of this study and future works that can be done.

Chapter 2

LNA Fundamentals and literature review

2.1 Introduction

This chapter gives a review of the fundamental theoretical concept on LNA performance metrics including the S-parameter, the power consumption, linearity and the noise figure. Next, the discussion continues with the relevant literature review on LNA topologies followed by the proposed circuit. Later in this chapter, the concept of RF circuit design before designing the LNA are discussed as well.

2.2 Overview of LNA

In the signal receiving path, the wanted RF signal is weak and always surrounded by noise and interferers. These weak signals captured by the receiver are amplified by an electronic amplifier, LNA. LNA has always been a critical circuit component in any modern wideband receiver. In an UWB system, the LNA must satisfy stringent requirements of low noise, high gain, and high return loss, as well as low power consumption and higher linearity over a very wide bandwidth [4]. Moreover, the UWB LNA suffers many interferers from co-existing systems like WLAN and Bluetooth where it requires an excellent LNA linearity across the wideband.

However, the design of the receiver involves many issues and trade-offs as LNA is the first active element in the receiving chain. Thus, before exploring the design details of a low-power LNA, it is helpful to have the knowledge of the LNA design first.

2.3 LNA Performance Metrics

The performance metrics that determine the efficiency of an LNA are stated in Table 2.1 and described in detail in section 2.1.3.

Table 2 1: LNA performance metrics

Performance metric	Description
Gain	The gain ranges between 10-25 dB.
Return loss	Return loss below than <-10 dB is accepted.
NF	Represents the degradation in signal/noise ratio as the signal passes through a device.
Linearity	Higher linearity promises less signal distortion.
Power consumption	Low power consumption to prevent energy loss and wastage and also a strict requirement for mobile applications.

2.3.1 Scattering parameter

In radio frequency range, scattering parameters (S-Parameters) is normally employed to help to relate between the incident voltage to the port and the reflected wave from the port. S-parameters differ from other parameters as it does not employ open or short circuit to characterize a linear electrical network but with match loads [5]. S-parameters are often used in RF operating networks where the signal power and energy considerations are easily quantified than voltages and currents. S-parameters are measured in terms of power ratio and vary with the measurement frequencies [3][5].

By definition S-parameter of 2-port network can be expressed as follows [5],

$$b_1 = S_{11}a_1 + S_2a_2 \tag{2.1}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.2}$$

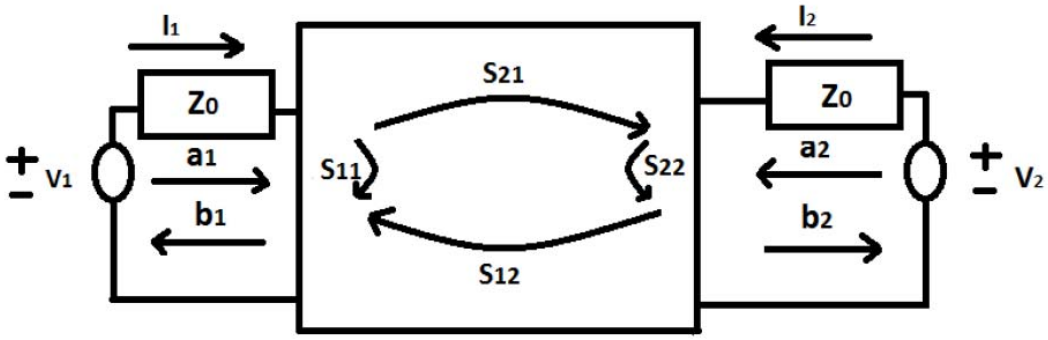

Figure 2. 1: S-parameter of two port network [5]

From the figure above, the independent variables, a_1 and a_2 are normalized incident voltages expressed as [5]:

$$a_1 = \frac{voltage\ wave\ incident\ on\ port1}{2\sqrt{Z_0}} = \frac{v_{i1}}{\sqrt{Z_0}} \tag{2.3}$$

$$a_2 = \frac{voltage\ wave\ incident\ on\ port2}{2\sqrt{Z_0}} = \frac{v_{i2}}{\sqrt{Z_0}} \tag{2.4}$$

Meanwhile, the dependent variables b_1 and b_2 are normalized reflected waves expressed as:

$$b_1 = \frac{reflected\ voltage\ wave\ from\ port1}{2\sqrt{Z_0}} = \frac{v_{r1}}{\sqrt{Z_0}} \tag{2.5}$$

$$b_2 = \frac{reflected\ voltage\ wave\ from\ port1}{2\sqrt{Z_0}} = \frac{v_{r2}}{\sqrt{Z_0}} \tag{2.6}$$

From the equations above, S-parameters are a method of describing the behaviour of incident and reflected waves at the ports of a network. In a two-port network, S_{11} is the input reflection coefficient and S_{22} is the output reflection coefficient, S_{21} is the forward transfer parameter, and S_{12} describes the reverse transfer [6].

I) Input reflection coefficient with matched output port

$$S_{11} = \frac{b_1}{a_1} \text{ at } (a_{2=0}) \quad (2.7)$$

II) Reverse transmission coefficient with matched input port

$$S_{12} = \frac{b_1}{a_2} \text{ at } (a_{1=0}) \quad (2.8)$$

III) Forward transmission coefficient with matched output port

$$S_{21} = \frac{b_2}{a_1} \text{ at } (a_{2=0}) \quad (2.9)$$

IV) Output reflection coefficient with matched input port

$$S_{22} = \frac{b_2}{a_2} \text{ at } (a_1 = 0) \quad (2.10)$$

S_{11} is the input return loss which is defined as the ratio of the reflected voltage wave to the incident voltage at the input port with load impedance matched to Z_0[6]. S_{21} is known as forward transducer power gain as it is the ratio of the reflected voltage wave at the output port to the incident voltage applied at the input port, provided the output port termination in $Z0$[6]. The S-parameters often expressed into the Equation 2.11,

$$S_i(dB) = 20\ log_{10} S_i \quad (2.11)$$

The S_{21} is often designed to be more 10 dB with S_{11} and S_{22} being below than -10dB for a better LNA performance. Meanwhile, S_{12} is expected to be less than -40 dB for better circuit stability.

2.3.2 Noise

Noise limits the minimum signal level that a circuit can process with acceptable quality. This causes the analogue designers to deal with the problem of noise because it trades with power dissipation, speed and linearity.

Circuit noise is associated with the electrical components that build the subcomponents, such as resistor and transistor. The noise phenomena considered are caused by small current and

voltage fluctuation that are generated within the device themselves. There a two types of circuit noises [5].

a. Device electronic Noise: noise created within the circuit namely thermal noise, flicker noise.

i. Thermal noise - noise caused by the random thermal movement of carriers in the channels. Since MOSFET operation is controlled by voltage, it noise varies with resistance value in the triode region. Equation 2.12 shows the model that is valid in the triode region of MOSFET operation [5][6],

$$i_d^2 = 4kT\gamma g_{do}\Delta f \tag{2.12}$$

Where k is Boltzmann's constant, T is temperature, γ varies between 1 and 2/3 in triode region, g_{do} is the channel conductance and f is frequency.

ii. Flicker noise – noise that are prominent in MOSFET devices as it is caused by the charge trapping phenomenon. Some impurities and defects randomly trap and release charges which in turn causes noise spectrum in the transistors. However, for high frequency applications flicker noise is often not considered a concern.

b. Environmental Noise- it is caused by random interruption in circuit through power supply and ground lines. However, it is often negligible in MOSFET as the device noise interrupts its performance.

The noise performance is translated into noise factor, F. The F is defined as [5]:

$$F = \frac{SNR_{IN}}{SNR_{OUT}} \tag{2.13}$$

where SNR_{IN} and SNR_{OUT} are the signal-to-noise ratios measured at the input and output. itis often translated into decibels and commonly referred to as noise figure, NF [5].

$$NF(dB) = 10log_{10}F \tag{2.14}$$

2.3.3 Linearity

Linearity is a key requirement in the design of an LNA because the LNA must be able to maintain the linear operation in the presence of a large interfering signal. The linearity of a system determines the maximum allowable signal level to its input [7]. All real-life systems exhibit some degree of nonlinearity which causes some Signal distortion is a direct consequence of the nonlinear behaviour of the devices in the circuits. The most common measures of non-linearity are the 1-dB compression point (P1dB) and the third-order intercept point (IIP3) [7].

2.3.3 1-dB compression Point

When the input signal is increased, a point is reached where the power of the signal is not amplified by the same amount as the smaller signal at the output. At this point where the input signal is amplified by an amount 1 dB less than the small signal gain, thus it is called 1 dB compression point. Operation should occur below this point in the linear region.

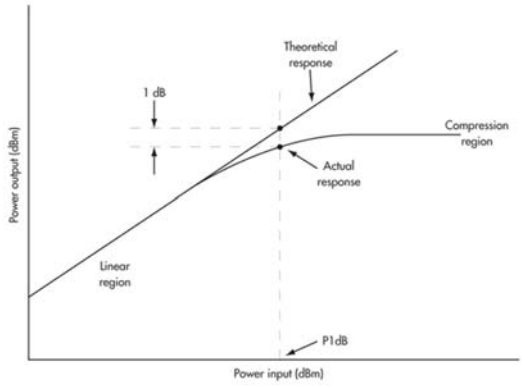

Figure 2.2: 1-dB compression point [7]

2.3.5 Third-Order Intercept Point

When two signals with different frequencies are applied to a non-linear system, the output exhibits some components that are not harmonics of the input frequencies. Called

intermodulation (IM), this phenomenon arises from “mixing” (multiplication) of the two signals. This intermodulation is modelled in the figure below.

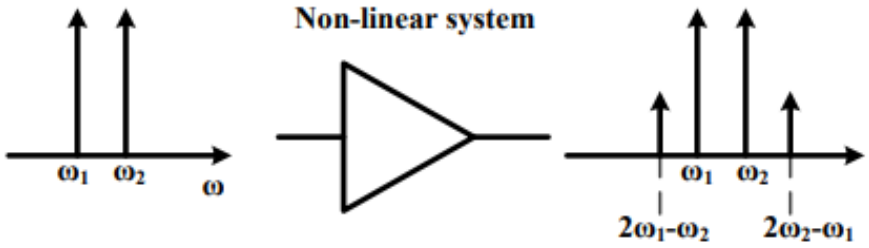

Figure 2.3: Intermodulation in a nonlinear system [5]

Figure 2.3 shows the IIP3 at which the third-order distortion signal amplitudes equal to the power of the first order output. This a theoretical point at which the third-order distortion signal amplitudes equal the input signals. This point is never reached as the transistor saturate before this could occur. The LNAs are designed to have a high value IIP3 indicating a good linearity.

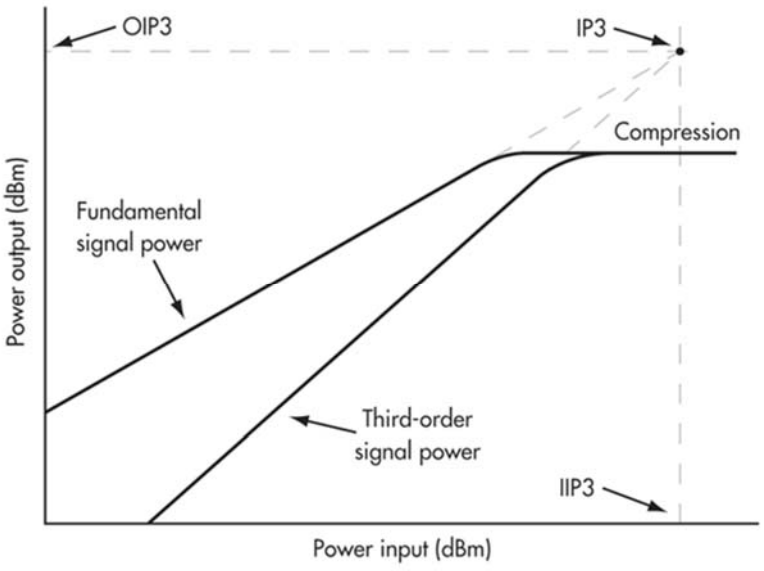

Figure 2. 4:Third order Intercept [7]

2.3.6 Stability

The stability analysis is another important step in the LNA design. The stability,K_f of an amplifier is a very important consideration in a microwave circuit design. Stability or resistance to oscillation in a microwave circuit can be determined by the S-parameters. Oscillations are possible in a two-port network if either or both the input and the output port have negative resistance. There are two types of amplifier stability, unconditionally stable and conditionally stable. To get unconditionally stable system, K_f should be more than 1. The method of calculating K_f is explained futher in Chapter 3.

2.3.7 Power consumption

Power consumption is one the primary concerns in designing a wideband LNA. As LNA is low-powered device, it only burns a few milliwatts(mW) of power depending on the type of operation. However, the power consumption is often in trade off with gain and noise performance in an LNA as it all could not be satisfied at once [8][9]. To obtain optimized performance with minimum trade-offs, design techniques such physical construction of the circuit board, circuit topology selection and transistor design are being incorporated.

2.3 Literature review

Many LNA designs and researches are compared and four of them are selected with the respect to the desired performance metrics of LNA. The work that had been selected are Cao Jia et al [10], Mehran Nazari [11], Pokharel et al [12] and Amsyar [13] are summarized below.

2.3.1 30-dB 1–16-GHz low noise IF amplifier in 90-nm CMOS [10]

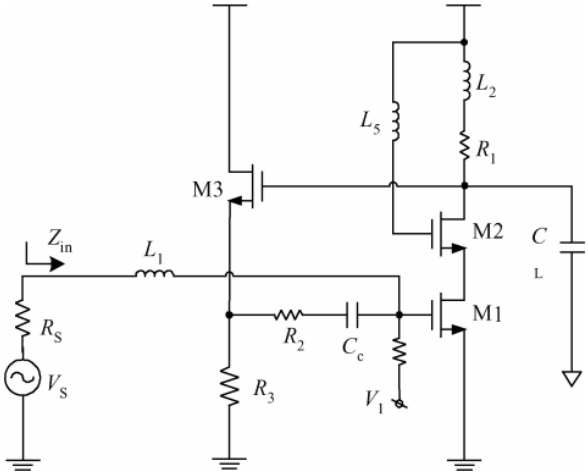

Figure 2.5: Resistive feedback with input series inductor L1 and series peaking inductor L5 [10]

A high-gain wideband low-noise IF amplifier aimed for the ALMA front end system using 90-nm LP CMOS technology. Active shunt feedback technique is employed along with input inductor and a gate-inductive gain-peaking inductor to extend the matching bandwidth and optimize the noise figure across 1–16 GHz.

The LNA achieves an excellent flat gain of 30.5 dB over the bandwidth of 1–16 GHz and a minimum noise figure of 3.76 dB. However, the S_{11} reaches <-10 dB for the desired bandwidth but S_{22} only achieves <-10 dB from 2-8 GHz only. Meanwhile, the output-to-input isolation indicated by S12 is below 48 dB in the desired band of 4–12GHz. The design consumes huge power of 42 mW with 1.2V voltage supply.

2.3.2 Wideband Low Noise Amplifier using Modified Cascode Structure for 45GHz Band Applications [11]

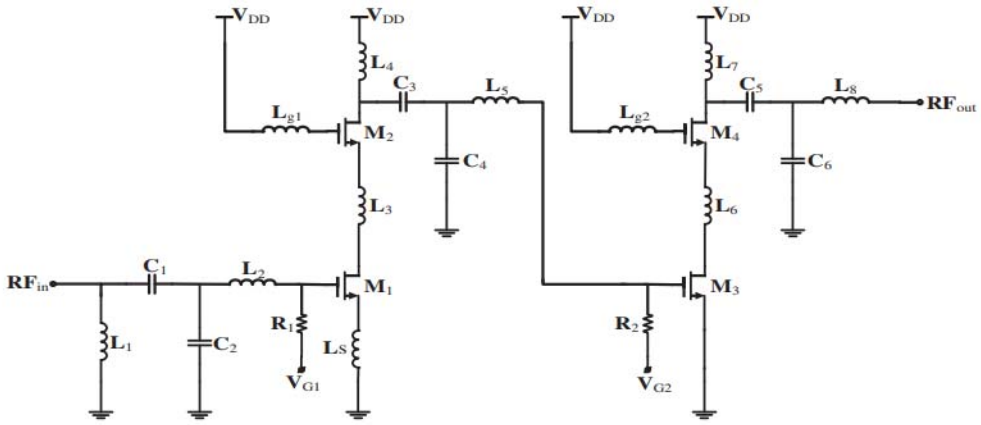

Figure 2.6: Modified cascode structure topology [11]

The LNA is simulated by using 0.18 um CMOS technology for high frequency application at 45 GHz with modified cascode structure topology. The LNA circuit contains two modified cascode stage to achieve desirable gain. The modified cascode structure leads to gain improvement and consequently decreases the circuit's noise and improves system's NF. Meanwhile, the band pass networks are used in LNA's input and output to achieve wideband matching.

The LNA achieved 8 dB gain across the wide bandwidth and low NF of 4.8 dB in 45 GHz frequency. Moreover, the insertion loss, S_{11} and S_{22} achieve value <-10 dB across the wideband. The LNA consumes 11.2 mW of power by using 1.8 V supply voltage.

2.3.3 Flat Gain and Low Noise Figure LNA for 3.1-10.2GHz Band UWB Applications [12]

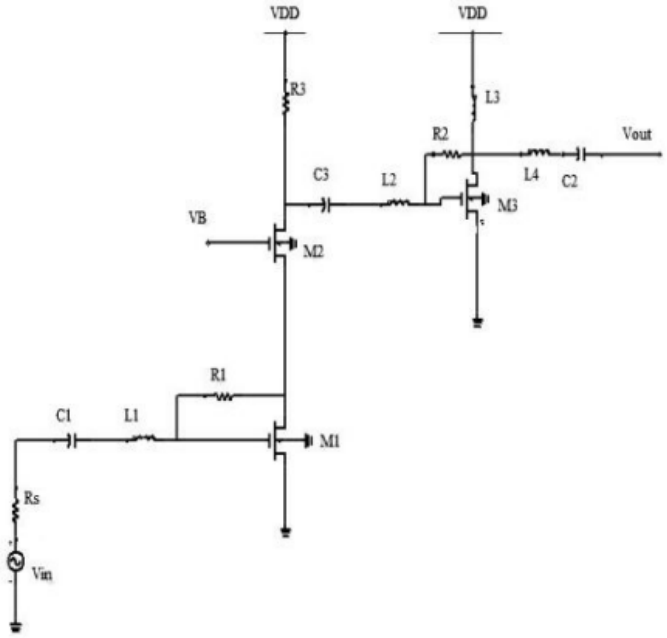

Figure 2.7: Resistive shunt feedback topology [12]

The LNA in Figure 2.9 is simulated using 0.18um CMOS technology for 3.1-10.2GHz Band UWB applications. The circuit employs resistive shunt feedback technique and an inter-stage inductor as an inductive peaking to realize the flat gain throughout the UWB band. The cascode amplifier with resistive shunt feedback is used to supply the feedback current to the input to achieve input matching and low NF.

This UWB LNA achieves a 20 dB flat gain, NF less than 3.5dB and input return loss is less than -7 dB. The reverse isolation of the designed LNA which is lesser than -45dB. It consumes high power consumption of 24 mW with 1.8V voltage supply.

2.3.4 0.13-um CMOS LNA with Flat Gain for Cognitive Radio Application [13]

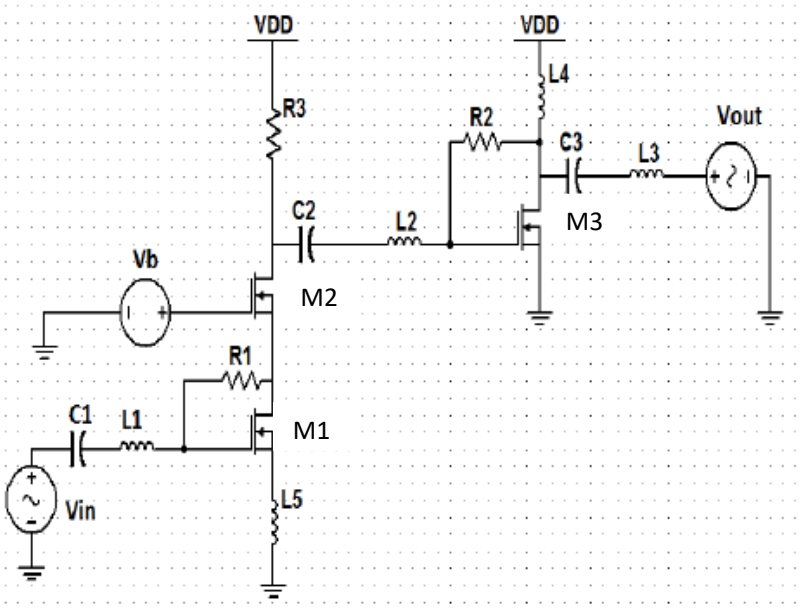

Figure 2.8: Resistive shunt feedback with inductive degeneration [13]

The Figure 2.10 shows the optimized LNA circuit of Amysar [13]. The original LNA circuit from [12] is optimized for better performances and in even wider bandwidth. The UWB bandwidth stretches from 300 MHz -10GHz and performances of the LNA across this bandwidth is simulated using 0.13-um CMOS technology. An additional inductor, L_5 is added into the circuit to the improve S_{11} and NF.

This reoptimized LNA achieved high flat gain with minimum and maximum value 18.56dB and 21.31 dB, respectively. The NF is lower than 5 dB throughout the desired bandwidth, the reverse isolation is below -49.43 dB and the power consumption is 30.11 mW with 1.2V voltage supply.

Table 2 2: Comparison on LNA performance from previous works

Performance metrics	[10]	[11]	[12]	[13]
Topology	Active shunt feedback	Cascoded structure	Resistive shunt feedback	Resistive-feedback LNA with inductive source degeneration
Bandwidth (GHz)	1-16	32-52	3.1-10	0.46-10
S_{11} (dB)	<-10	<-10	<-7	<-10 (8-10 GHz)
S_{21} (dB)	30	8	20	19
S_{22} (dB)	<-7	<-10	-	<-7.5
S_{12} (dB)	<-48	<-40	-45	<-50
Power (mW)	42	11.2	24	34.8
NF (dB)	3.5	4.8	3.5	4.41
IIP3 (dBm)	-22	-	-9	7.97
CMOS Technology(μm)	0.9	0.13	0.18	0.13

From the literature review made, it is seen that each topology is proven to provide different performance metrics. Thus, it is important to choose the topology that provides the desired performance required by this work. Based on the Table 2.2, it can be seen that [10], [12] and [13] design provide higher gain value than in [11] as these designs employ the resistive feedback LNA.

The resistive feedback and an inductive peaking technique help to achieve the flatness of the gain throughout the UWB band [12]. Negative feedback also improves the stability (K) factor to provide unconditional stability of the amplifier and reduce the gain sensitivity [10]. However, the power consumption [10] design is the highest amongst the four. Nevertheless, this also contributes to the highest gain.

Meanwhile for the design in [12], the wideband is very broad as it stretches from 300MHz to 10GHz. However, this design is found to be having a relatively high gain, low NF but less optimum input and output matching. Moreover, it is known that the cascading resistive shunt feedback is mainly designed for reducing power consumption [12]. Cascading resistive shunt feedback amplifier is used for this LNA design operates in low power and less input supply voltage [12] [13].

The inductive degeneration impedance matching method is the most preferred architecture as it does not add noise to the LNA and simultaneously achieves both input and noise matching [13]. The inductors are utilised to extend the bandwidth [12] and reduce the NF of the LNA. Besides, the decreasing size of CMOS technology will result in better NF for the LNA. This can be seen in design [10] with 0.9μm and it achieves the least NF compared to other works, [11][12][13]. However, the better noise performance can also be contributed by the higher power consumption as in [10].

All in all, although all the designs cover the wideband application, the performance metrics of each design varies. Amongst the compared work, design [13] is found to be the better topology to be employed in this project considering its ability to provide wide bandwidth operation at high flat gain with moderate power consumption. However, trade-offs and optimization are needed on the circuit to fulfil the design specification of this project.

Chapter 3

Methodology

3.1 Introduction

In a RF front-end of receiver, LNA is one of the key segments which decides the execution of affectability, linearity and power utilization. The challenge in designing UWB LNA is to design a LNA with high gain, low NF and high linearity across the wideband.

This work prioritizes the enhancement of input and output matching of the CMOS LNA with the wideband range of 300MHz to 10GHz. Meanwhile, the trade-offs and the drawbacks are needed to be considered to produce the LNA with the best performances metrics in wideband applications [11]. Furthermore, the effects of RF components on the LNA design is studied and optimized again for the performance enhancement. Finally, the design of LNA is expected to meet certain specifications such as high flat gain and low power consumption as well.

The LNA is designed in Cadence Virtuoso to obtain the simulation data for design verification and further analysis. However, this design does not follow the custom IC design flow (full custom design flow) as this work only stops at pre-layout simulation stage due to time and financial constraints. The steps involved in this work is as shown in the following flowchart Figure 3.1:

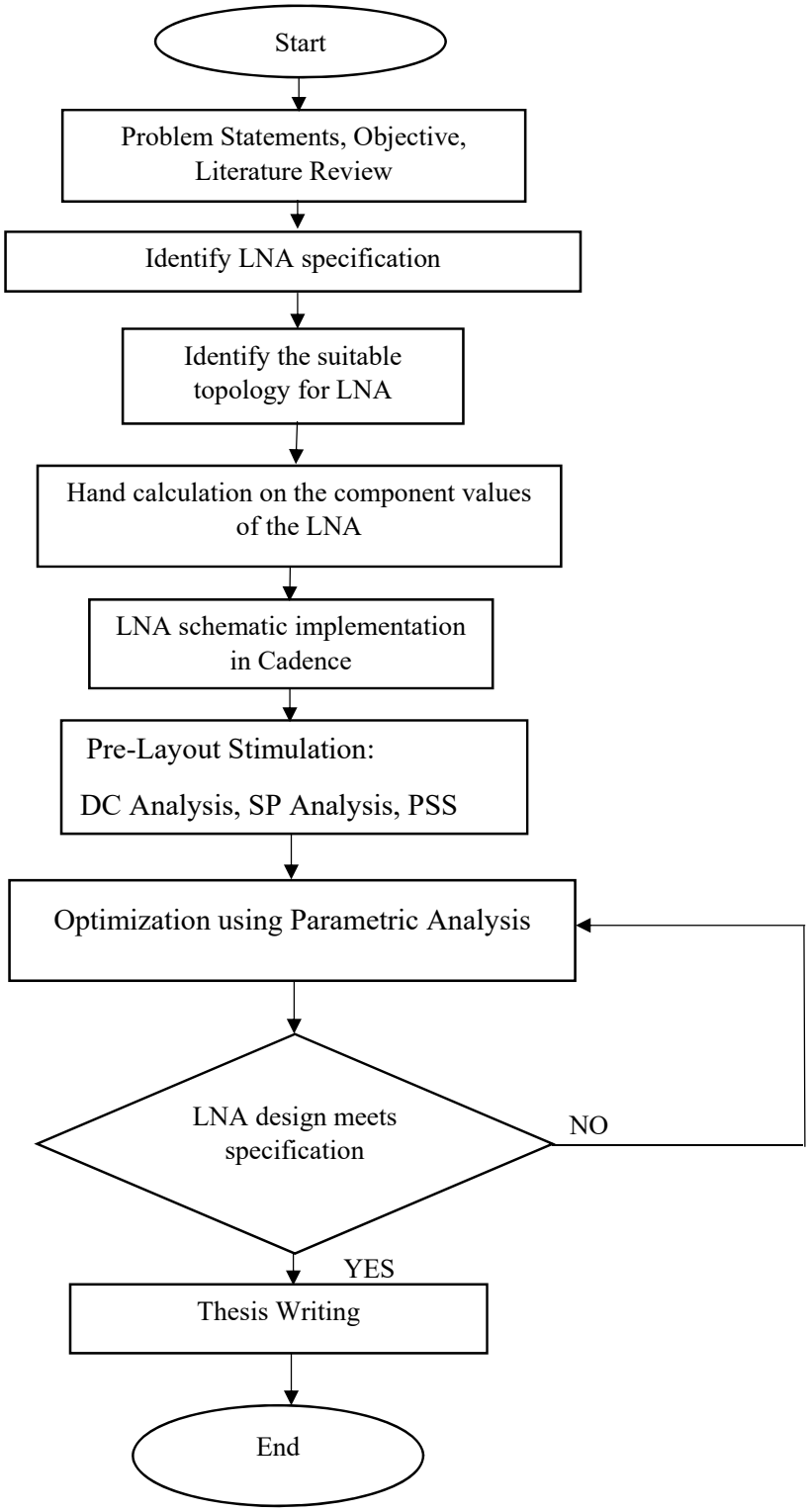

Figure 3.1: Project Implementation Flow

3.2 Design Specifications

The design flow for any circuit always starts with a set of target specifications that describes the expected output of the designed block in the end. As for LNA design, usual specifications are normally concern about the gain, matching parameters, noise performance and linearity,

The UWB LNA designed is for CR reception range (300MHz-10GHz) using 0.13µm CMOS technology. The low cost, power consumption and area make the CMOS technology the best choice to set up this LNA compared to other models. Following table 3.1 shows the specifications outline the requirements for the designed LNA. These design specifications were derived from the literature review conducted in Chapter 2 which LNA performance metricswere summed up in Table 2.2.

Table 3: 1: Design specifications for LNA

Parameters	Specification
Operating frequency range (GHz)	0.3-10
Voltage gain(dB)	>15
Noise figure (dB)	<5
Matching parameters (dB)	<-10
IP1dB (dBm)	>-20
IIP3dB (dBm)	>-10
Power consumption	<20mW

3.3 Calculation of components

3.3.1 Width of M1, M2, M3

The width of the transistors is vital to the ensure that the transistor could operate in saturation region. For a NMOS transistor to achieve the saturation region, the following condition should be obeyed [5],

$$V_{DS} \geq V_{GS} - V_{TH} \tag{3.1}$$

The width of M1 of LNA [13] is calculated by using a few assumptions. The input impedance of the circuit is given by the equation,

$$\frac{V_{in}}{I_{in}} = Z_{in} = 50\Omega \tag{3.2}$$

The equation shows Z_{in} represents input impedance which need be matched to the 50Ω source. From the literature review carried out in section 2.2, it is found that drain current, I_D used is 2 mA. Thus, the I_D is set as a constant here and the value of transconductance is obtained using the Equation 3.4 with considering the assumption below [14],

$$V_{ov} = V_{gs} - V_{th} = 0.2V \tag{3.3}$$

$$g_m = \frac{2I_D}{V_{ov}} \tag{3.4}$$

The width of the M1 can be determined using the Equation 3.5,

$$W = \frac{2I_D L}{\mu_n C_{OX}''(V_{gs} - V_{th})^2} \tag{3.5}$$

where $W =$ width of M1/m, $L = 0.13\mu\text{m}$ for CMOS technology, $\mu_n = 0.022\ m^2/(V \cdot s)$ and $C_{0X}'' = 0.015145\ F/cm^2$

Meanwhile, the width of M2 is made about half of M1. This to limit the capacitive load while still only minorly affecting the NF which leads to better linearity performance [5]. The

gate terminal of M2 is connected to power supply and the width of M3 is made almost equal to M3 to maintain the gain across the wideband.

However, after iterations, the values of M2 and M3 are slightly altered for a better performance. Meanwhile, the length, L of all transistors are equal to 0.13 µm.

3.3.2 Input matching network

Matching is a critical task in LNA design. The goal of input matching is to provide 50Ω proper termination for standard communication application. In this design, the impedance matching topology used is inductive source as this offers the best noise match. An ideal inductor, $L_5$was placed in the gate of the transistor to aid input matching and to improve NF.

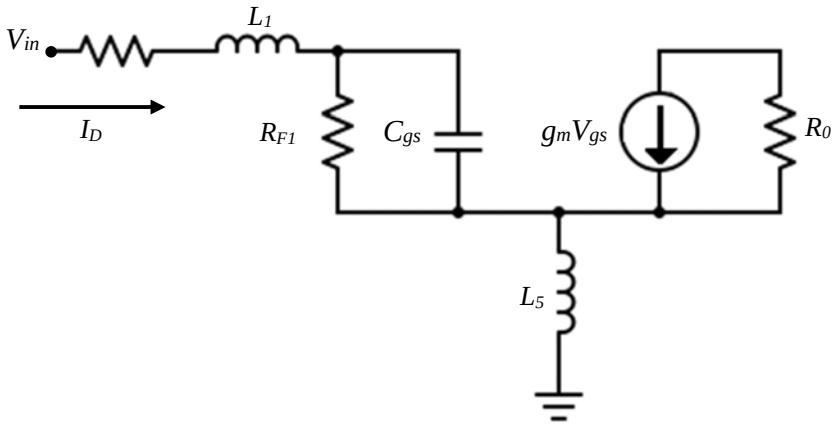

Figure 3: 2: Small signal equivalent circuit at the input of MOSFET

From the small signal model in Figure 3.2, the input impedance can be expressed as [5],

$$\frac{V_{in}}{I_{in}} = Z_{in} = j\omega(L_1 + L_5) + j\omega\left(\frac{1}{C_{gs}} + L_5 g_m V_{gs}\right) \quad (3.6)$$

$$Z_{in}(j\omega) = j\omega(L_1 + L_5) + \frac{1}{j\omega C_{gs}} + g_m \frac{L_5}{C_{gs}} \quad (3.7)$$

Thus, the real part of the Equation 3.7 as follows [5] [7],

$$Re[Z_{in}] = g_m \frac{L_5}{C_{gs}} = 50\Omega \quad (3.8)$$

$$Im[Z_{in}] = j\omega(L_1 + L_5) + \frac{1}{j\omega C_{gs}} = 0 \quad (3.9)$$

From the Equation 3.8, it can be observed that inductor, L_5 controls the real part of the input impedance of the circuit.

The ideal inductor does not bring with it the thermal noise of an ordinary resistor because a pure reactance is noiseless [15]. Hence, a method that creates a real part of input impedance without additional noise is found. This property is taken advantage to give specified input impedance without degrading the noise performance of the amplifier. Besides, the feedback resistor, R_{f1} also controls the input impedance of the circuit.

3.3.3 Output matching

The output matching of LNA has to be designed to get a flat gain and good linearity over the broadband. In this design, the output matching is realized through components inductors, L_3, L_4 and conductor, C_3. Moreover, the linearity can be optimized by tuning the output matching network.

3.3.4 Gain, S_{21}

As the type of topologies discussed in chapter 2, resistive shunt feedback with inductive degeneration LNA is found to the be best suited for the wideband UWB application. For the CMOS LNA, the feedback system is widely used as the input impedance of MOSFETs is large and mostly capacitive [15]. Hence, by coupling with passive components in the form of source