DESIGN AND SIMULATION OF LOW POWER COMPARATOR USING LOW POWER DESIGN TECHNIQUES FOR ANALOG CIRCUITS

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By

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LIST OF ABBREVIATIONS

ABBREVIATION	DESCRIPTION
ADC	Analog to Digital Converter
BTBT	Band-to-band Tunnelling
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DTTS	Dual Threshold Transistor Stacking
GND	Ground
ITRS	International Technology Roadmap for Semiconductor
IC	Integrated Circuit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTCMOS	Multi-threshold Voltage
MTSCStack	Multi Threshold Super Cut-off Stack
NMOS	N Channel MOSFET
PMOS	P Channel MOSFET
SCCMOS	Super Cut-off CMOS

LIST OF SYMBOLS

SYMBOL	DESCRIPTION
V_{GS}	Gate-to-source voltage
V_{TH}	Threshold voltage
V_{DS}	Drain-source voltage
V_{BS}	Bulk source voltage
V_{DD}	Drain supply
V_{IN}	Input voltage
V_{REF}	Reference voltage
V_{OUT}	Output voltage
V_{BP}	PMOS bulk biasing
V_{BN}	NMOS bulk biasing
P_{total}	Total power
$P_{dynamic}$	Dynamic power
$P_{leakage}$	Leakage power
$P_{short\text{-}circuit}$	Short circuit power
P_{static}	Static power
I_{leak}	Leakage current
I_{sub}	Sub-threshold leakage current

C_L	Load capacitance
P_{SC}	Dynamic short-circuit power
I_{PEAK}	Short-circuit current

REKA BENTUK DAN SIMULASI PEMBANDING KUASA RENDAH MENGGUNAKAN TEKNIK-TEKNIK KUASA RENDAH BAGI LITAR ANALOG

ABSTRAK

Pembanding adalah salah satu blok utama yang memainkan peranan penting dalam keseluruhan prestasi penukar analog ke digital (ADC) dalam semua peranti teknologi moden. Peranti berkelajuan tinggi dengan voltan dan kuasa yang rendah dianggap penting untuk aplikasi perindustrian. Reka bentuk pembanding kuasa yang rendah dengan kelajuan tinggi diperlukan untuk memenuhi keperluan dan kebanyakannya dalam peranti elektronik yang diperlukan untuk ADC kelajuan tinggi. Bagaimanapun, peranti berkelajuan tinggi yang membawa kepada teknologi proses CMOS yang semakin meningkat akan menggunakan lebih banyak kuasa. Teknik pengurangan kuasa diterokai dalam reka bentuk litar bersepadu elektronik. Teknik pengurangan kuasa seperti Multi Threshold Super Cut-off Stack (MTSCStack), Dual Threshold Transistor Stacking (DTTS), bulk-driven current mirror, NMOS bulk-driven differential pair dan PMOS bulk-driven differential pair telah dikaji. Tujuan kajian ini adalah untuk mengkaji gabungan teknik ini untuk menghasilkan pembanding yang boleh beroperasi dengan kuasa yang rendah tanpa menjejaskan prestasi sedia ada menggunakan 0.13µm CMOS proses. Pembanding dicadang (pembanding konvensional bersama MTSCStack & DTTS & PMOS bulk-driven differential pair) menunjukkan keputusan 11.1 mV bagi mengimbangi, 19.8 mV bagi resolusi, 40.5

gandaan voltan, 21.86 ns bagi perambatan lengah, 4.06 µW bagi kuasa statik, 18.91µW bagi kuasa dinamik dan 22.97 µW bagi keseluruhan kuasa.

DESIGN AND SIMULATION OF LOW POWER COMPARATOR USING LOW POWER DESIGN TECHNIQUES FOR ANALOG CIRCUITS

ABSTRACT

Comparator is one of the main blocks that plays an important role in overall performance of analog to digital converters (ADC) in all modern technology devices. High speed devices with low voltage and low power are considered essential for industrial application. Design a low power comparator with high speed is required to accomplish the requirements mostly in electronic devices that necessity for high speed ADCs. However, high speed device that lead the scaling down of CMOS process technology will consumed more power. The power reduction techniques are explored in electronic integrated circuit (IC) design. Power reduction techniques such as Multi Threshold Super Cut-off Stack (MTSCStack), Dual Threshold Transistor Stacking (DTTS), bulk-driven current mirror, NMOS bulk-driven differential pair and PMOS bulk-driven differential pair were studied. The aim of this study is to investigate the combination of these techniques to produce a comparator that can operate in low power without compromising existing performance using 0.13µm CMOS process. Proposed comparator (conventional comparator with MTSCStack & DTTS & PMOS bulk-driven differential pair) shows result of 11.1 mV for offset, 19.8 mV for resolution, 40.5 for voltage gain, 21.86 ns for propagation delay, 4.06 µW for static power, 18.91 µW for dynamic power and 22.97 µW for total power.

CHAPTER 1

INTRODUCTION

This chapter introduces the background of this study as well as the problem statement. This chapter also presents the objectives and the scope of this study. Besides, this chapter also presents the overview of the thesis.

1.1 Research Background

Semiconductor industries are facing a lot of problems in designing the chips consists of transistors with less than 10nm technology. Ever increasing demand for portable-operated system has lead to aggressive scaling. While technology scaling facilitates faster and high performance devices, at the same time it causes excessive power dissipation. Leakage power dissipation is now a dominating component of total power consumption in such portable devices. So there is a tremendous need to limit the power dissipation in high density chips which has initiated many innovative techniques to develop in the design of low power circuits and systems without increasing the size of the devices.

Employing ADC offers an industry best combination of low power and high performance and they are necessary for low power applications. ADC is one of the main components in any signal- processing system. They are used to process, transport or store any analog signal into digital form. ADC is mainly consists of comparator.

According to past work, the comparator is responsible for 70% of the ADC speed [1]. ADC are currently adopted in many application fields to improve digital system, which achieve superior performances with respect to analog solutions.

According to the International Technology Roadmap for Semiconductor (ITRS), the contribution of leakage to the overall power consumption is consistently increase as the size of the device getting smaller. As CMOS technology keeps scaling down, the leakage current has increased exponentially. The predominant way to generate low power is to start with the fundamental principles that are defined in the existing technologies that it gives low power is to start with less leakage current. In order to reduce the dynamic and static power consumption, some of the techniques have to be applied to the integrated circuit.

1.2 Problem Statement

Power consumption is now become a major concerned on technical problem facing the semiconductor industry. In previous research, power reduction technique is mostly applied in digital circuit. This is due to the complex design of analog circuit. Comparator is one of the analog integrated circuit that plays the important role in the most rapid growing building block which is ADC. In ADC, comparator is the electronic device that mainly used and responsible for the delay produced and power consumed by an ADC. A low power and high speed comparator is required to satisfy the future demand. Since the demand keep increasing, many alternative in redesigning the comparator with various type of techniques has been done.

The outcomes of this research is to get the best comparator with low offset, high voltage gain, low resolution while maintaining low propagation delay and high frequency for faster comparator speed. Therefore, we have to find the techniques that can reduce the power dissipation of the analog circuit without affecting the performance of ADC.

1.3 Objective of Research

Below are the objectives of this research :

I. To study and analyze the available power reduction technique.

II. To design a low power comparator using selected low power reduction techniques.

III. To compare the performance of conventional comparator with proposed comparator.

1.4 Scope of Research

This study is focuses on the design of power reduction technique and applies to the analog circuit which is conventional comparator. A low power proposed comparator is design using MTSCStack, DTTS , bulk-driven differential pair technique. Based on previous research on low power design techniques, conventional comparator with different type of bulk-driven technique where chosen to be compared. The simulation is carried out using Virtuoso Schematic Editor from Cadence. The technology used in this design is in 0.13 μm CMOS process technology.

1.5 Thesis Overview

This thesis consists of five chapters as describes below :

Chapter 1 provides the background and problem statement of this research. The objectives and the scope of this research also have been discussed in this chapter.

Chapter 2 will discuss on the literature review on the researches that are related to this work. It describes the literature review of power consumption. This chapter also discussed the advantage and drawbacks of each power reduction technique. In additions, theories and equations that are related to the design of low power comparator are included.

Chapter 3 focuses on the methodology of this work. This chapter also present the schematic of the conventional comparator and the proposed comparator as well as the detailed explanation on the circuit operation.

Chapter 4 present the result, analysis and discussion of this work. This chapter also includes the comparison of results between conventional comparator and proposed comparator. Cadence software is used to run the pre-layout simulation of the comparator.

Chapter 5 contains the conclusion of this work. At the end of this project, the best technique is identify based on the performance of the comparator. Further improvement and recommendation is discussed in order to improve the overall performance of the comparator.

CHAPTER 2

LITERATURE REVIEW

This chapter reviews the literature on power consumption of integrated circuit in which categorized into static power and dynamic power. Each of the components in static power and dynamic power also discussed. Then this chapter reviews various low power consumption techniques to be implement in the comparator circuit. Last but not least this chapter reviews the types and characteristics of comparator.

2.1 Power Consumption

Power consumption is the basic constraints and primary limitation in any type of integrated circuit to the further advancement of semiconductor technologies. The cost of the system is directly related to power. In electronic devices, power dissipation happen when power is converted into heat and then radiated away from the device. A better cooling mechanism are required if the integrated circuit is consuming more power to keep the circuit in normal conditions. The device may get damaged on continuous use due to this generated heat. An analysis of power dissipation related problems faced by semiconductor industry starts with identifying the source of power consumption. There are four primary sources of power consumption in CMOS integrated circuit. The total power consumption of CMOS circuit is

$$P_{total} = P_{dynamic} + P_{leakage} + P_{short\text{-}circuit} + P_{static} \quad (2.1)$$

2.1.1 Static Power

Static power refers to the power consumed when a CMOS circuit is driven by low voltage swing input signal. IC will dissipate some static power even though there are no explicit circuits using static current. This power dissipation is result of leakage current through nominally off transistors and it is known as off-state leakage. Static power is essentially determined by the formula

$$P_{static} = I_{leak} . V_{dd} \quad (2.2)$$

Where,

V_{dd} = supply voltage

I_{leak} = leakage current

Overall static power consumption may be reduced by reducing any of the parameters. Meanwhile the leakage current can be minimized by lowering the operating point and lowering the leakage transistor.

2.1.1.1 Leakage Current

Leakage current which is the source of static power consumption is a combination of sub-threshold and gate-oxide leakage.

$$I_{leak} = I_{sub} + I_{ox} \quad (2.3)$$

Where ,

I_{sub} = sub-threshold leakage

I_{ox} = gate-oxide leakage

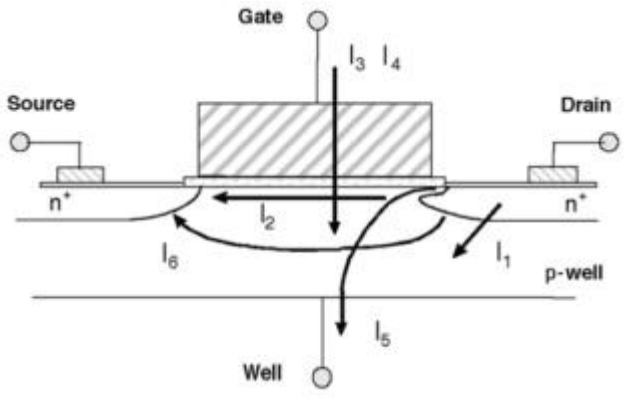

Figure 2.1 : Leakage current in CMOS device.

Figure 2.1 shown several sources in a CMOS device that caused the leakage current [2]. The leakage currents are dominated by reverse-bias diode leakage at the transistor drains and sub-threshold leakage through the channel of an "off" device known as I_1 and I_2 respectively. I_3 is the oxide tunneling current. The reduction of the gate oxide thickness caused the I_3 to appear. Hence holes or electrons can tunnel the gate oxide [2].

2.1.1.2 Reverse-biased PN-junction Leakage

The reverse-biased PN-junction leakage is known as the band-to-band tunnelling (BTBT). This leakage occurs between diffused region and the substrate. As a result, parasitic diode is formed. Since the diode is reverse-biased, leakage current exist when the transistor is in idle state and only its leakage current contributes to static power. The reverse-biased PN-junction leakage current is expressed as below.

$$I_D = I_S(e^{\frac{qV}{KT}} - 1) \tag{2.4}$$

Where ,

I_s = reverse saturation current

V = diode voltage

K = Boltzmann's contant (1.38×10^{-23} J/K)

q = electronic charge (1.602×10^{-19} C)

T = temperature

2.1.1.3 Sub-threshold Leakage

A MOSFET operates in the weak inversion known as sub-threshold region when V_{GS} is below than threshold voltage, V_{TH}. In this state the transistor considered as an "OFF" and no current should flow from source to drain. However, it exist a current defined as the sub-threshold current[2]. The sub-threshold region is important in analog circuit in order to operate at low power. So, only small voltage is required for biasing. The sub-threshold leakage current is represented by the following equation 2.5 [3].

$$I_{SUB} = K(\frac{W}{L})e^{(\frac{V_{GS}-V_{TH}}{nVT})}(1-e^{\frac{-V_{DS}}{VT}}) \quad (2.5)$$

Where,

K = Boltzmann's contant (1.38×10^{-23} J/K)

$\frac{W}{L}$ = width / length

n = technology parameter

V_{GS} = gate-source voltage

V_{TH} = threshold voltage

V_{DS} = drain-source voltage

From equation 2.5, two possible ways for reducing I_{SUB} are turning off the supply voltage and stepping up the V_{TH}.

2.1.2 Dynamic Power

The dominant source of power consumption in a typical CMOS circuit is the dynamic power. Dynamic power happens when a device is actively switching from one state to another. The dynamic power is divided into dynamic capacitive power and dynamic short-circuit power. Capacitance is leads to dynamic power dissipation during the charging and discharging of the parasitic load capacitances. While short circuit power is caused by direct current from V_{dd} to ground due to conducting path between NMOS and PMOS transistor.

2.1.2.1 Dynamic Capacitive Power

The dynamic capacitive power is the most consumed power during the device states of changing its logic. Charging and discharging of capacitance is required to change the transistor state from OFF bit to ON bit or vice versa. The dynamic power can be calculated as the following formula.

$$P_{dynamic} = C_L V_{dd}^{\ 2} f \tag{2.6}$$

Where,

C_L = load capacitance

V_{dd} = supply voltage

f = operating clock frequency

There are three ways to reduce dynamic capacitive power. Lowering the supply voltage is one of them because supply voltage affects the most dynamic power. Reduce the capacitance and and operating clock frequency are the other ways.

2.1.2.2 Dynamic Short-circuit Power

The dynamic short-circuit power is the instantaneous short-circuit power flows from the power supply to ground when both PMOS and NMOS are simultaneously active during switching time. During this time, PMOS and NMOS transistor conduct current at the same time, The dynamic short-circuit power is given by

$$P_{SC} = t_{sc} V_{dd} I_{peak} f \tag{2.7}$$

Where ,

t_{sc} = slope of the input signal

V_{dd} = supply voltage

I_{peak} = short-circuit current

f = frequency

2.2 Power Reduction Techniques

In recent years, many highly effective techniques for reducing the leakage power consumption have been proposed. This is due to shrinking of devices that has grown exponentially with the power consumption. Research on the power reduction techniques have proven to be effective in increasing the performance of a circuit. There are a few commonly used power minimization technique such as Body-biasing, Super Cut-Off CMOS (SCCMOS), Multi-Threshold CMOS (MTCMOS), Stack transistor and Sleepy keeper technique. Hence, a few selected power reduction techniques are analyzed to be tested in the proposed comparator.

2.2.1 Multi-Threshold CMOS Technique (MTCMOS)

MTCMOS is a very popular technique for standby mode in leakage power reduction. In this technique, high threshold device is inserted in series into low V_{TH} circuitry [4]. Figure 2.2 shows MTCMOS circuit in which increases the performance of the circuit when threshold voltage devices is lower while decreases the standby current of the circuit when threshold voltage sleep transistors is high. In standard design, the power terminal is not connected directly to the supply but to virtual Vdd and virtual Gnd. MTCMOS is such an effective technique for reducing leakage currents in combinational logic [5].

The MTCMOS technology has two main features. Firstly is “active” and other is “standby”. During the active mode sleep signal is OFF while sleepbar is ON and the circuit operates normally. During the standby mode, sleep signal is ON while sleepbar

is OFF. Thus both the sleep control transistors are off due to the cut-off from the power supply [6]. Since sleep transistors are high threshold voltage transistors, the leakage current is reduced.

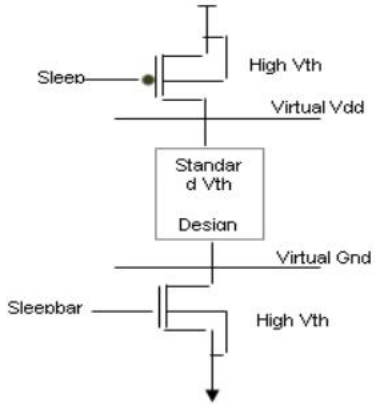

Figure 2.2 : MTCMOS structure [4]

2.2.2 Stack Transistor Technique

The stack transistor technique is a technique used in active mode for leakage power reduction. The leakage current decrease due to two or more series transistor are turned off, which known as Stack effect [4]. Equation 2.5 gives the relation of the sub-threshold current to the four terminal voltage. The dependence of sub-threshold current is determined by the transistor stacking effect. Besides, when the source voltage of the transistor increase,the sub-threshold leakage current reduces exponentially. By increasing the number of transistor connected in stack structure, more leakage power saving can be obtained. The technique resulted in V_{GS} becomes more negative because of the positive potential at the intermediate ode of the stacked transistor. However, the addition of transistors induces the diminishing of the performance and increment of dynamic power consumption.

2.2.3 Sleepy Stack Transistor Technique

The sleepy stack technique is the combination structure of forced stack technique and sleep transistor technique. By using sleepy stack, the exact logic state is retained unlike sleep transistor and forced stack technique. High threshold voltage transistor can utilize without delay penalties[4]. The structure of sleepy stack transistor technique is the solution for static power consumption problem.In this approach, the first step of implementation is forced stacking by replacing the transistor with two or more series transistor. Then, followed by inserting the sleep transistor parallel to one of the stack transistors. For circuit implementation, the width of the transistor is divided into half compared to the transistor size and connected to form a stack[5].

The working of sleepy stack circuit during active mode and during standby mode of operation shown in Figure 2.3. During the active mode, the two parallel transistors are ON ,thereby reducing the effective resistance of the path. This result the propagation delay is reduced during the active mode. During the standby mode, sleep transistors are OFF and the leakage power is reduced due to the transistor stacking effect.

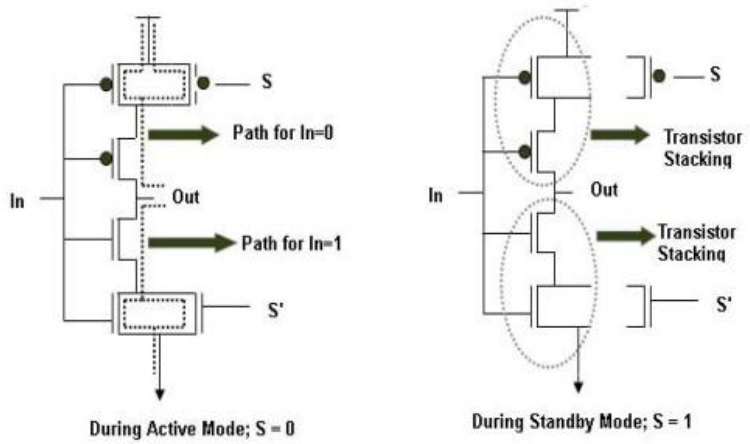

Figure 2.3 : Sleepy Stack Structure

2.2.4 Super Cut-Off CMOS (SCCMOS)

Figure 2.4 shows the structure of SCCMOS technique[4]. As stated in equation 2.5, the sub-threshold leakage current is dependent on V_{GS} . Therefore, by using slight negative voltage gate according to Figure 2.4, the sub-threshold current can be reduced. This technique almost similar with MTCMOS technique. The key difference between these two technique is the sleep transistor have the same low threshold voltage as compared to high threshold voltage. The additional delay produced by high threshold voltage sleep transistor can be reduced due to the uses of low threshold voltage sleep transistor during active mode. The sleep transistors are over-driven or under-driven in standby mode, which induce the standby leakage mechanism.

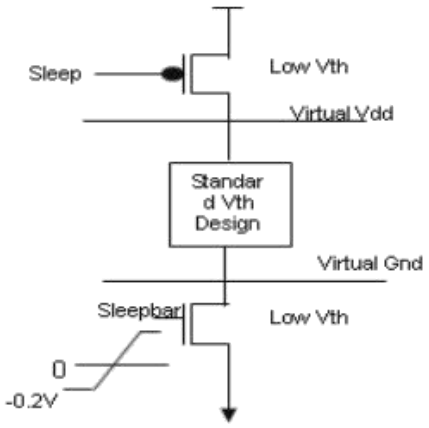

Fig. 2. SSCMOS

Figure 2.4 : SCCMOS structure

2.2.5 Dual Threshold Transistor Stacking Technique (DTTS)

Dual Threshold Transistor Stacking (DTTS) is the combination of Multi Threshold CMOS (MTCMOS) and Stack Transistor technique. Means the sleep transistors of high threshold voltage are redesign with stack effect. The combination takes an

advantages of power reduction during both active and standby mode. It effectively reduces the leakage current by assigning higher threshold voltage to the transistors in non-critical paths , while the performance is maintained due to the use of low threshold transistors in the critical path. [5] . Figure 2.5 shows the structure of DTTS technique.

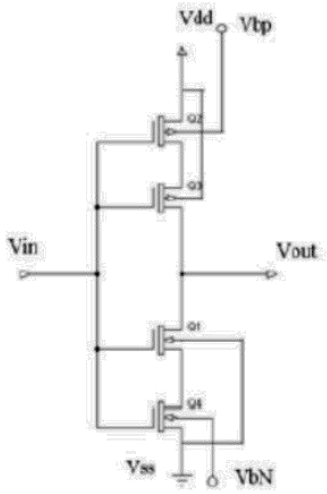

Figure 2.5 DTTS structure

2.2.6 Multiple Threshold Super Cut-off Stack (MTSCStack)

Multi Threshold Super Cut-off Stack (MTSCStack) is the combination of three power reduction techniques which are Multi-Threshold CMOS (MTCMOS), Super Cut-off CMOS (SCCMOS) and forced stack transistor technique. In MTSCStack technique, power consumption is reduced in active mode and in the same time retains the exact logic state in sleep mode [7]. Operation of MTSCStack technique is similar to the MTCMOS technique where the sleep transistors are turned on during active mode and turned off during sleep mode. The low threshold voltage transistor work with high speed in active mode when sleep transistor are turned on and able to reduce leakage power. Meanwhile in standby mode, there is no connection between low threshold

voltage transistor and source as well as ground when sleep transistor are turned off. In this case, high threshold voltage will reduce the leakage power. The only source of VDD to the pull up network is when NMOS transistors in parallel to the PMOS sleep transistors and the only source of GND to the pull down network is when PMOS transistors in parallel to the NMOS sleep transistors. Figure 2.6 shows the structure of MTSCStack technique.

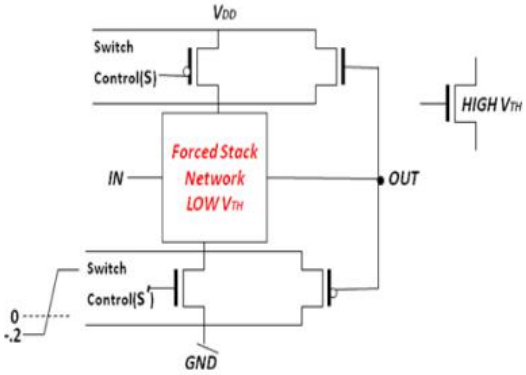

Figure 2.6 : MTSCStack structure

2.2.7 Bulk-driven Technique

Threshold voltage is a critical parameter for low voltage operation of any CMOS devices. However threshold voltage does not scale down at the same rate as of power supply. This poses a great challenge to CMOS mixed-signal design. To perform any sort of signal processing, the MOSFET is required to be turned on. Therefore, the supply voltage must be satisfied equation 2.8. for strong inversion operation. While when the MOSFET is a gate-driven the supply voltage satisfied equation 2.9.

$$V_{dd} + |V_{ss}| \geq V_{GS} = V_{DS} + |V_T| \tag{2.8}$$

$$V_{DD} + |V_{SS}| \geq V_{GS} = V_{DS} + |V_T| + V_{SIGNAL} \tag{2.9}$$

Equation 2.9 consist of overhead associated with threshold voltage from the signal path. To overcome this problem, the bulk-driven technique is proposed. Bulk driven MOSFET (BDM) is a very effective technique in removing the bottleneck caused by threshold voltage and it works like JFET as a depletion device.

2.2.7.1 Bulk-driven Current Mirror

In the bulk-driven technique, the signal is applied at bulk-drain instead of gate-drain connection. This technique is employed to overcome the threshold voltage limitation [8]. Since the signal is applied to the bulk-driven, requirement of V_{TH} is removed from the signal path. Under this circumstance, a lower voltage drop is required across input and output terminals of the drive. With the fixed voltage at the gate terminal ensures the dependency of the MOSFET current on the bulk-driven voltage based on the equation 2.10 below:

$$I_D(sat) = \frac{\beta}{2}(V_{GS} - V_{TH0} - \gamma\sqrt{|2\Phi_F| - V_{BS}} + \gamma\sqrt{|2\Phi_F|}^2) \quad (2.10)$$

$$V_{DS} > V_{GS} - V_{TH}$$

Where ,

$\beta = \mu C_{ox} W/L$

μ = mobility of the carriers

Cox = gate oxide capacitance per unit area

W/L = aspect ratio of MOSFET

Φ_F = absolute fermi potential

V_{T0} = zero bias threshold voltage

γ = body-effect coefficient

Figure 2.7 shows the design structure of the bulk-driven PMOS current mirror with the bulks of M1 and M2 are tied together rather than the gates and Figure 2.8 shows the design structure of the bulk-driven NMOS current mirror . By using equation 2.10 above, the current across the MOSFET can be determined. Precaution must be taken that the value of V_{BS} is such that bulk-source junction either reverse biased or slightly forward biased with V_{BS} less than V_{TH} to ensure the negligible bulk current in the circuit. Constant bulk source is applied to get the operation current mirror of the bulk-driven circuit, M1 and M2 MOSFETs. In order to enhance the current range, transistor pair must be in saturation region [8]. It can be done by connecting their gates to an appropriate value.

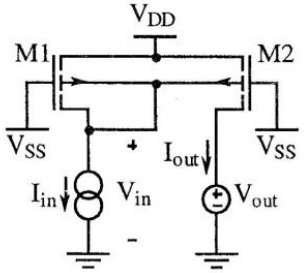

Figure 2.7 : Bulk-driven PMOS Current Mirror

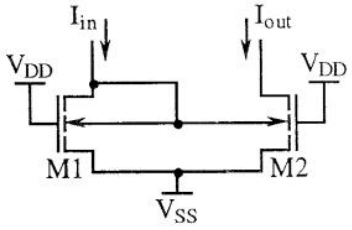

Figure 2.8 : Bulk-driven NMOS Current Mirror

2.2.7.2 Bulk-driven Differential Pair

The last technique to be proposed is Bulk-driven differential pair. When applying this technique in the circuit design, satisfactory performance especially in the low-voltage and low-power applications can be achieved [10]. In the bulk-driven approach, the input signals (Vi+ , Vi-) are applied to the bulk terminals of transistors MB1 and MB2, whereas the gate terminals of these devices are biased with a suitable level V_G in order form the channel [11] .The channel current is modulated by the input signal applied to the bulk terminals. The drain current of an MOS transistor depends on the value of the threshold voltage, which for a p-channel device can be expressed as equation 2.11

$$V_{TH} = V_{THO} + \gamma\left[\sqrt{\left|2\Phi_F + V_{SB}\right|} - \sqrt{\left|2\Phi_F\right|}\right] \tag{2.11}$$

Where,

λ = body-effect coefficient

Φ_F = Fermi potential

V_{SB} = source -bulk potential difference

V_{THO} = threshold voltage in the absence of V_{SB}

For a standard n-well CMOS process, only PMOS devices can be used as bulk-driven transistor. Figure 2.9 shows the bulk-driven PMOS differential pair [11] and figure 2.10 shows the bulk-driven NMOS differential pair [12]. Since the bulk-driven has good control of threshold voltage, it allows a low voltage operation.

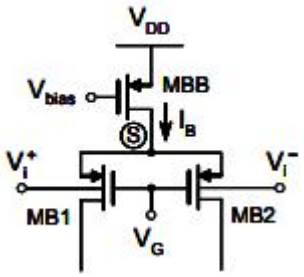

Figure 2.9 : Bulk-driven PMOS Differential Pair

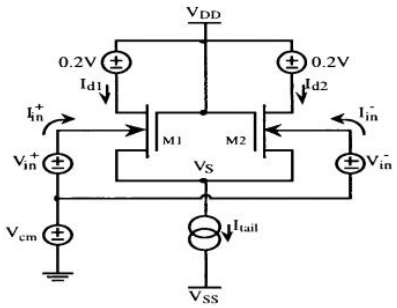

Figure 2.10 : Bulk-driven NMOS Differential Pair

2.3 Comparator

The comparator or known as 1-bit analog-to-digital converter is a circuit that compared an analog signal with another analog signal or with a reference signal. Based on the comparison, comparator will produces binary signal as the output [13]. In flash ADC, in the form of thermometer code, the $2^n - 1$ comparator contribute the input for the encoder. Comparator plays an important role as it is the key blocks for high speed operation. When the analog input voltage is greater than the reference voltage, output '1' is produced. While when the analog input voltage is less than the reference voltage, the comparator will produce output '0'. Figure 2.11 shows the symbol of the comparator [14]. Widely, comparator can be divided into three type. Firstly, open-loop comparator and the other is open-loop with regenerative feedback comparator. The

third type is the combination of the open-loop and open-loop with regenerative feedback which is high comparator [14]. Figure 2.12 shows the voltage transfer function of non-inverting and inverting comparator [15] .

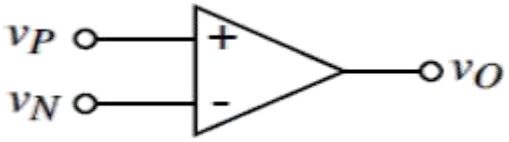

Figure 2.11 : Symbol of comparator

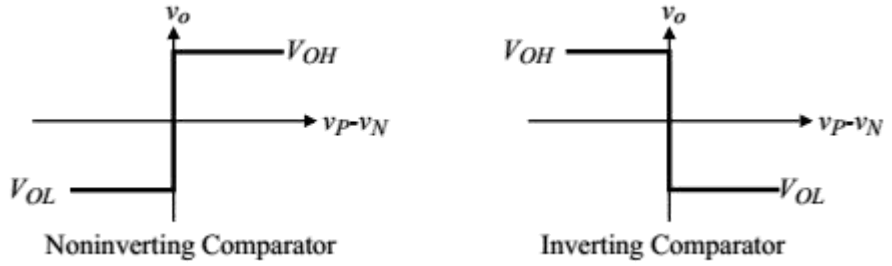

Figure 2.12 Voltage transfer function

2.3.1 Open-loop Comparator

Operational amplifiers are commonly implemented as a comparator. Comparator requires a proper differential input and sufficient gain to be able to produce desired resolution. Figure 2.13 shows the two stage open-loop comparator circuit. Since it is open-loop, the circuit does no need frequency compensation to drive the comparator time response. The circuit consumes minimum number of transistor hence minimize the area of the circuit [13]. However, the open loop comparator is too slow in many applications due to limited gain-bandwidth product.

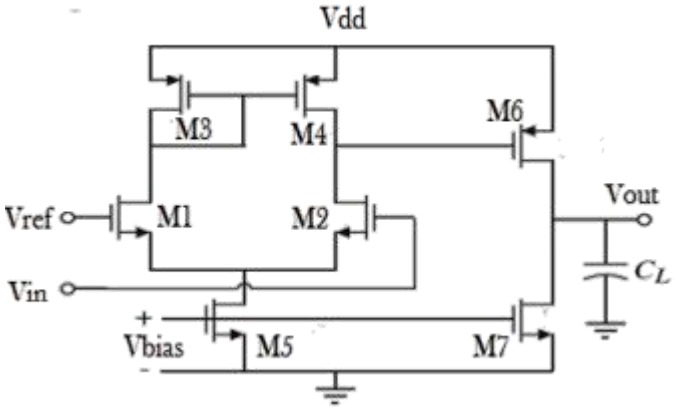

Figure 2.13 : Two stage open-loop comparator

2.3.2 Offset Voltage in Comparator

The resolution of comparator is produced from the difference between input voltage V_{IH} and V_{IL} . The output of the comparator is change when the input voltage is zero in ideal comparator. Practically, the output change is in non-zero input voltage because of the manufacturing process such as transistor mismatch [15]. The offset voltage, V_{os} is shown in transfer curve Figure 2.14. The offset voltage can be determined using the difference between the intersection point the transfer curve with the $V_P - V_N$ and V_O intersection with the $V_P - V_N$. The offset value, sometimes can be predicted where the offset voltage value is half of the value of the comparator resolution. However, problems occur when it is unpredicted.

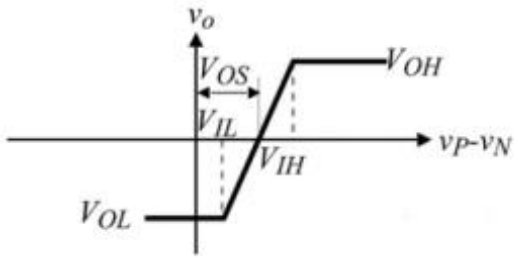

Figure 2.14 : Offset voltage of the comparator

2.3.3 Propagation Delay in Comparator

Another important parameter in comparator is the propagation delay. Propagation delay is to measure of time response of the comparator between output transition and input citation. The speed of conversion of ADC is depends on the length of the propagation delay thus making the parameter very important in ADCs. Figure 2.15 shows the propagation delay time of a non-inverting comparator. The propagation delay inversely proportional to the input. The higher the input, the lower the propagation delay. However, the increment of the input will not affect the delay if there is an upper limit. The operation of comparator in this mode is called slew rate. During the slew rate mode, the propagation delay can be reduced by increasing the sinking or sourcing capability of the comparator.

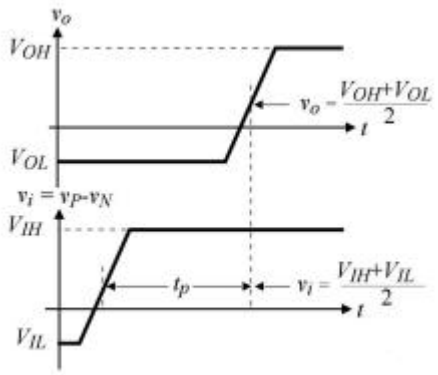

Figure 2.15 : Propagation delay of the comparator

2.4 Summary

In this chapter, static power and dynamic power in integrated circuit have been reviewed. Furthermore, the available power reduction techniques such as Dual Threshold Transistor Stacking (DTTS), Multiple Threshold Super Cut-off Stack (MTSCStack) and Bulk-driven have been analyzed to be implemented in the design of low power and high speed comparator. The operators of the comparator and architecture are also studied for better understanding the operation.