DESIGN AND ANALYSIS OF A CMOS IMAGE SENSOR

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2018

ACKNOWLEDGEMENT

First and foremost I would like to express my gratefulness to the All mighty Allah S.W.T for giving me strength and health during completing this final year project.

I would like to express my sincerest and gratitude to my supervisor, Dr. Anwar Hasni, whose support, guidance and encouragement from the first day of proposing the project title to the very end of this report that helped me to develop my understanding towards the project, his willingness to motivate me contributed a lot in completing this project.

Finally, an honorable regards and blessing to my beloved family and friends for supporting me in any aspect during the completion of this project.

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LIST OF ABBREVIATIONS

ABBREVIATIONS	DESCRIPTION
CMOS	Complementary Metal-Oxide-Semiconductor
CCD	Charge Coupled Devices
CIS	CMOS image sensor
DC	Direct Current
GND	Ground
MOSFET	Metal Oxide Semiconductor Fiel Effect Transistor
NMOS	N Channel MOSFET
PMOS	P Channel MOSFET
APS	Active Pixel Sensor
PPS	Passive Pixel Structure
LASI	LAyout System for Individuals
ADE	Analog Design Environment
CDS	Correlated Double Sampling
FF	Fill Factor
PD	Photodiode

REKA BENTUK DAN ANALISIS SENSOR IMEJ CMOS

ABSTRAK

Projek ini membentangkan satu cip yang direka untuk tujuan menilai kaedah reka bentuk dalam melaksanakan CMOS Image Sensor Technology (CIS) untuk aplikasi visi berasaskan Active Pixel Sensor (APS). Untuk tujuan ini, cara-cara yang mungkin untuk melaksanakan sensor array pixel dan litar bacaan berkaitan dengan teknologi CMOS standard menggunakan proses 0.18μm CMOS yang tersedia secara komersil dengan kedua-dua p-baik dan pelaksanaan n-baik diterokai. Ini adalah untuk memastikan bahawa sensor imej kami digunakan untuk banyak aplikasi. Untuk mencapai matlamat ini, teknologi CIS penyelidikan ini perlu meningkatkan ciri-cirinya seperti kepekaan, arus gelap dan bunyi bising yang sangat bergantung pada susun atur. Cip ini termasuk satu set arsitektur piksel di mana parameter yang berbeza telah diubah suai, susunan penyebaran aktif dan voltan ambang transistor pengikut yang asal. Pengimejan CMOS hanya mempunyai 1 piksel, tetapi itu boleh diperbaiki dengan menukar logik imbasan kerana saiz array piksel ini adalah metrik yang memberikan petunjuk sensor imej prestasi di mana ia dinyatakan sebagai megapixel. Terdapat banyak cara untuk melaksanakan pengesanan piksel CMOS menggunakan mod akumulasi. Pelaksanaan penginderaan piksel aktif yang paling mudah ialah 3T-APS dilaksanakan dalam projek ini. Angin voltan yang diperoleh dari 1 piksel 3T-APS ini ialah 2.66V.

DESIGN AND ANALYSIS OF CMOS IMAGE SENSOR

ABSTRACT

This project presents a chip designed for the purpose of evaluating the design method in implementing a CMOS Image Sensor Technology (CIS) for Active Pixel Sensor (APS) based vision applications. For this purpose, the possible ways of implementing pixel array sensors and readout related circuit with standard CMOS technology using commercially available 0.18 μm CMOS processes with both p-well and n-well implementations were explored. This is to ensure that our image sensors applicable for many applications. Towards this aim, this research CIS technology have to improve its characteristics such as sensitivity, dark current and noise that are strongly layout dependent. This chip includes a set of pixel architectures where different parameters have been modified, layout of active diffusion and threshold voltage of the source follower transistor. This CMOS imager only has 1 pixel, but that can be improved by changing the scan logic because the size of this pixel array is a metric that gives an indication of the performance image sensor where it is expressed as a megapixel. There are many ways to implement CMOS pixel sensing using accumulation mode. The simplest active pixel sensing implementation is 3T-APS is implemented in this project. The voltage swing obtained from 1 pixel of this 3T-APS is 2.66V.

CHAPTER 1

INTRODUCTION

1.1 Background

Complementary metal-oxide semiconductor (CMOS) is a mainstream technology that offers many advantages for digital, analog and mixed-signal application. CMOS has been experiencing a rapid growth that is driven by some huge markets, including CPUs, solid-state memories, ASIC, general-purpose logic integrated circuits and now image sensors[1,2].

The evolution of image sensors started with the invention of Charge Coupled Devices (CCDs) in 1969 at the Bell Labs by Drs. Willard Boyle and George Smith[3] and then Complementary Metal-Oxide Semiconductor (CMOS) was introduced around1970s. However, the use of CMOS technology in the development of image sensors has only begun to be known in early 90s when it is finally suggested. From time to time the performance of CMOS image sensor improved significantly and is more acceptable in most applications.

The first generation of CMOS image sensor was passive pixel CMOS arrays, before CMOS APS (Active Pixel Sensors) was introduced. CMOS APS have shown better performance and flexibility in imaging application compared to the previous technology of the image sensors. However, there must be the improvement on this CMOS APS in order to strongly compete with the others technologies that researchers need to work on. Therefore, there have been several reports on improving the fill–factor (FF) with low power consumption, low voltage operation, low noise, high speed imaging and high dynamic range[4].

1.2 Problem Statement

Before the existence of CMOS image sensors (CIS), Charge-coupled devices (CCDs) have traditionally been the dominant image-sensor technology. In the last decade, design of image sensors implemented in complementary metal-oxide semiconductor (CMOS), Active Pixel Sensor (APS) of CMOS, has emerged as a potential replacement to CCDs. This trend is driven by the[5] increasing demand on larger pixel numbers, better quality, low power, low cost and the ability to integrate different functions in CMOS sensors, unlike CMOS image sensors, CCD cannot be monolithically integrated with analog read out and digital control electronics[6].

The early-stage CMOS image sensors did not compare favorably with that of CCD image sensor due some factors like CMOS's high dark current in the photodiode and high readout noise. Thus, in order to reach compatible result with CCDs, many designs and techniques have been proposed by researcher to overcome the disadvantages of the existing CMOS image sensor.

Adding chip or feature level new features designing for more application specific constraints, reducing the noise and increasing the sensitivity are some of the achievement of the proposed designs, APS design with 3 or 4 number of transistors have been the ones that are used most due to their simplicity and low area head. However, the APS design suffer from the analog limitation since the output of each pixel value is represented by analog voltage signal and required column or chip level ADC.

1.3 Objectives

The objectives of this project are:

1. To study the method of designing a CMOS image sensor (CIS) and to analyse the sensor.
2. To design the pixel circuit for the CMOS image sensor and improve the performance of the previous technology.

1.4 Project Scope

In this project, some possible ways of designing low-cost imaging system are investigated by implementing CMOS active pixel sensor (APS). APS are sensors that implement a buffer per pixel. This APS consists of 2-D matrix of pixel, two addressing decoders for pixel selection by row and column, one decoder for reset of whole column, 1-D array of row switches and readout circuits, and analog buffers[7]. The APS have three different designs that are based on nMOS transistor, pMOS transistors, and both nMOS and pMOS transistors. Each pixel employs one photodiode and three transistors.

Basically, there are three major approaches in order to design a CMOS imager; architecture design, layout design and design verification. The LAyout System for Individuals, LASI is used as a PC based integrated circuit design tool. It is versatile enough that it can be used for ICs, MEMS, discrete devices, schematics, PC boards and project documentation drawings[8]. In the LASI system, complex IC designs are made from simpler object cells. A cell might be a logic gate or an op-amp. Each cell is assigned a name and a rank.

For CMOS image sensor design and performance prediction, it is necessary to verify the layout of the circuit matches the schematic of IC. Simulation Program with Integrated Circuit Emphasis(SPICE) is a general-purpose, open source analog electronic circuit simulator and PSpice is a PC version of SPICE .PSpice has analog and digital libraries of standard components (such as NAND, NOR, flip-flops, and other digital gates, op amps, etc) which makes it a useful tool for a wide range of analog and digital applications. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior.

1.5 Thesis Outline

Overall, this thesis report consists of five main chapters that cover the full details from introduction to conclusion of this research project. The first chapter is the introduction of this research project.

Chapter 2 is the literature review of CMOS image sensor. This chapter begins with the background of image sensor and includes the introduction of different types of image sensors which are Charge-coupled devices (CCDs) and Complementary Metal-Oxide Semiconductor (CMOS). Furthermore, different CMOS pixel sensor and techniques that are compatible with the standard CMOS image sensor (CIS) to with their advantages and disadvantages of each technique used are also presented**.**

In Chapter 3, the methodology for development of this research project is explained in detail. It includes the project implementation flow, circuit design architecture and the simulation tools for both pre-layout and post-layout design. The chip includes different standard CMOS process compatible photodiode and pixels are also explained in this chapter. Within this chapter,

the layout design of this chip, which is specific to n-well 0.18µm standard CMOS process is represented.

In chapter 4, the results and discussion for this research project is presented.it discussed about suing reference design as starting platform and simulation for developed modules. Moreover, the performance analysis of this research project also presented in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

The research on designing a CMOS image sensor (CIS) is a very wide scope of study. First, this chapter provides the background of CMOS image sensor (CIS) and a brief discussion of this CIS feature. The next section reviews about related works in CMOS imager which have been done by previous researchers. In section 2.4, the comparison between CMOS imager and CCDs are discussed. Then, the operation principle and fundamental of characteristics of photo-detector are described in section 2.5. The design of CMOS compatible photodiodes also included for this CIS. In section 2.6, different CMOS pixel sensor circuits and techniques that are compatible with standard CMOS process are discussed by explaining both pixel structure, active pixel sensor (APS) and passive pixel structure (PPS). In Section 2.7, different design of Active Pixel Sensor (3T-APS) is presented. Next, peripheral blocks other than pixels are described in Section 2.8. Addressing and readout circuits are also mentioned in this section. Next, the overall configuration of CIS is covered in Section 2.9. Lastly, a summary for this chapter is provided in Section 2.10.

2.2 Background of Imaging Sensor

The history of Complementary Metal-Oxide Semiconductor (CMOS) image sensor (CIS) begins with solid-state imagers used as replacement for image tubes. There are four important for solid-state image sensors: light detection, accumulation of photo-generated signals, switching from accumulation to readout and scanning.

Morrison at Honeywell proposed the scanning function in X-Y addressed silicon-junction photo sensing devices as the “photoscanner” in the early 1960s[9]. Weimer et al. proposed solid-state image sensors with scanning circuit using thin-film transistors[10]. The photoconductive film is used for the photo detector in these devices. The accumulation mode in a photodiode was first proposed by Weckler[10] at Fairchild Semiconductor used the floating source of a metal-oxide semiconductor field effect transistor as a photodiode. Moreover, Weckler also fabricated and demonstrated a 100 x 100-pixel image sensor by using structure[11]**.**

The imaging area consists of an array of pixel, vertical and horizontal access circuitry and readout circuitry. The architecture of a CIS is as shown in Figure 2.1.

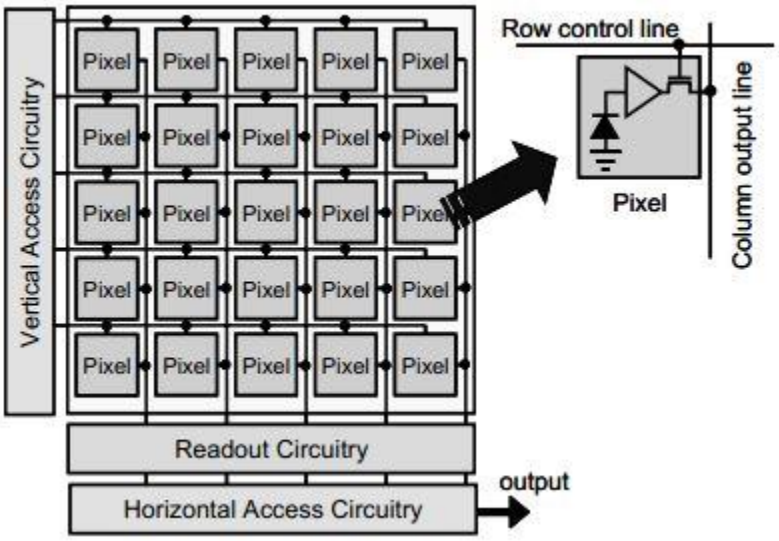


Figure 2.1: Architecture of a CMOS image sensor[6].

The imaging area is a two-dimensional array of pixels; each pixel contains a photo-detector and some transistors. This area is the heart of an image sensor and the imaging quality is largely determined by the performance of this area. Access circuitry is used to access a pixel and

read the signal value in the pixel. Usually a scanner or shift register is used for the purpose, and a decoder is used to access pixels randomly. A readout circuit is a one-dimensional array of switches and a sample and hold (S/H) circuit. Noise cancel circuits, such as correlated double sampling (CDS), are employed in this area[12].

2.3 Related Works

There are numerous studies have attempted to explain about the implementation of a CMOS image sensor (CIS) that can be used to design a CMOS image sensor (CIS).

Beatriz Blanco-Filgueira et al.[13]. In this work, the peripheral contribution to the total pixel photo-response in a 0.18μm CMOS technology was studied using test structures and device simulation. Experimental data was used to fit a semi-analytical model revealing a trade-off between photodiode main area and perimeter in the overall pixel photo-response.

Vargas-Sierra et al.[14] proposed a chip designed for the purpose of evaluating different design alternatives in a 0.18 μm CMOS Image Sensor Technology (CIS) for Active Pixel Sensor (APS) based vision applications. It has been found that round-like pixels have better sensitivity than octagonal-like ones. Besides, source follower transistors with low Vth expand the range of output voltages with no negative effect.

2.4 Comparison between CMOS image sensor and CCDs

In this section, the comparison between CMOS image sensor (CIS) and CCDs will be discussed. The imaging sensor is mainly classified into two types; Charge Coupled Devices

(CCDs) and CMOS image sensor. Both CCD and CMOS image sensors depend on the photoelectric effect to create electrical signal from light and the principle of converting light into charge is almost the same as CCD in CMOS image sensor, just the read out scheme is different.

A CCD sensor converts pixel measurements sequentially using circuitry surrounding the sensor. Only a single amplifier is used for all of the pixels in CCD image sensor as shown in Figure 2.2 The CCD transfer the signal charge to the end of the output signal line and converts it into a voltage signal through this single amplifier[12]. While, CMOS sensors convert pixel measurements simultaneously, using circuitry on the sensor itself and it use separate amplifiers for each pixel as shown in Figure 2.3. The parallel outputs that CMOS imagers could offer, give advantages for high speed imaging means it is possible to acquire the images in very short period of time. The parallel outputs that CMOS imagers could offer, give advantages for high speed imaging means it is possible to acquire the images in very short period of time. Other than that, because of active pixels and ADC are on the same chip that exists in CMOS image sensors, it offer faster images processing for the sensor. This is why CMOS image sensors are preferable in high speed imaging and have received much attention over lately, because their performance is very promising compared to CCD image sensors.

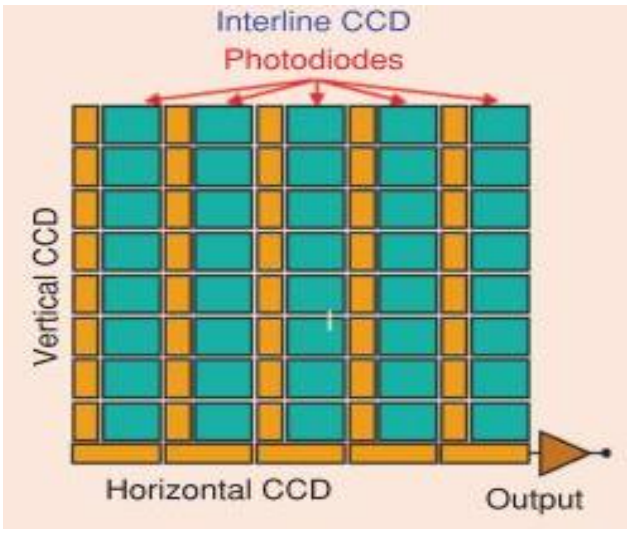


Figure 2.2: Readout architectures of interline transfer CCD[1]

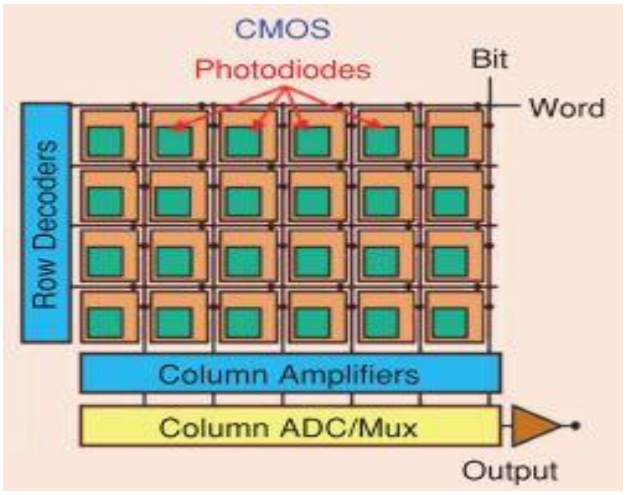


Figure 2.3: Readout architectures of interline transfer CMOS image sensor[1]

2.5 Fundamental of characteristics of photo-detector

The most common type of photo-detector used in CMOS imager technology is P-N junction photodiode (PD), also known as n+/p-well and n-well (NW)/p-type substrate (SUB)

junction is commonly used for photodiode information. However, since 0.18 μm CMOS processes will be implemented for this research project, an NW/PSUB junction is the most suitable PN photodiode structure for processes below 0.35 ~ 0.5 μm. A profile diagram of a pixel cell is shown in Figure 2.4. The "photo area" is simply a large area of source or drain N diffusion.

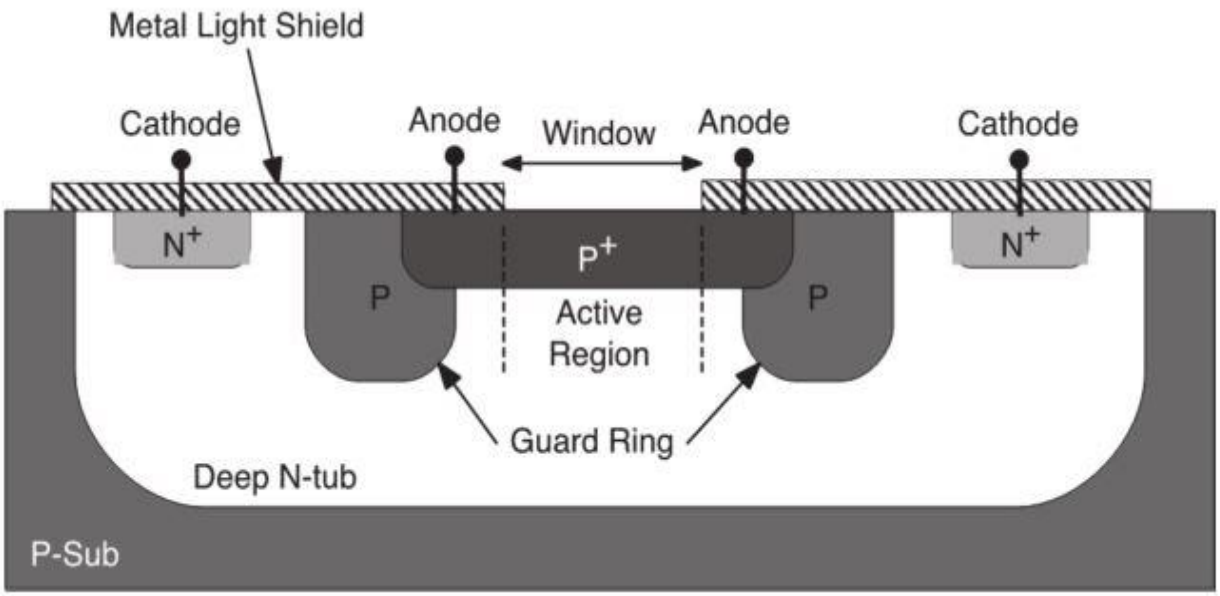


Figure 2.4: Profile diagram of PN photodiode structure

Visible light is absorbed in the silicon below the photo area. This creates free electron-hole pairs which usually will recombine after a few microseconds. Depth of light absorption is also highly dependent on wavelength. Most of the visible spectrum is absorbed in a micron or two of silicon. The depletion region in the P substrate is also a micron or so wide for normal doping levels. Free carriers, holes and electrons, generated in the depletion are rapidly swept out of the depletion by the built-in E field. This is considered "fast" photo current.

Under the P substrate there can be either more P doping or a reverse biased P-N junction. If the pixel cells are small in relation to the absorption depth, we might have to put a reverse biased junction under the region to prevent image leakage from pixel to pixel.

When light strikes the photodiode, the pixel will sensing the incident light and generating the charge signal to be converting the light into measurable voltage. After a certain time of exposure, the signal (voltage) in the pixel is readout and then CDS operation is performed by column electronics after all pixels of the selected row have been reset and read out.

2.6 CMOS pixel sensor circuits and techniques

Basically, there are two types of pixel structures that have been developed since CMOS image sensor was introduced. These two types of pixel structures are passive pixel structure (PPS) and active pixel structure (APS). Historically, PPS came into existence earlier than APS. APS were developed with the purpose to enhance the image quality from previous technology. The biggest difference between APS and PPS is the difference in the number of transistors. PPS consists of only one transistor in a pixel, in contrast to APS with 3 transistors in each pixel or known as 3T-APS. Shortly after 3T-APS, APS that has four transistors in a pixel, the so-called 4T-APS, has been developed to improve the image quality. It has been proven that 4T-APS has improved image quality, but has to undergo a very complex fabrication process compared to conventional 3T-APS.

2.6.1 Passive Pixel Sensor (PPS)

PPS was developed as the first CMOS imager before APS was emerged before this PPS developed was halted due signal-to-noise ratio (SNR) that appears in PPS. The structure of PPS is very simple: a pixel only consists of a photodiode and a transistor in order to connect it to readout structure as shown in Figure 2.5.

Because of its simple structure, a PPS has a large fill factor (FF), the ratio of the PD area to the pixel area[3, 12]. For an image sensor, a large fill factor (FF) is preferable compared to small FF. In spite of the large fill factor, the output signal degrades easily. Other than that, this PPS also suffer from low sensitivity and high noise due to the large column's capacitance (large column FPN) with respect to the pixel's one. Furthermore, this scheme also contain large k_BTC noise, the thermal noise and large smear, which is a ghost signal appearing as vertical stripes without any signal.

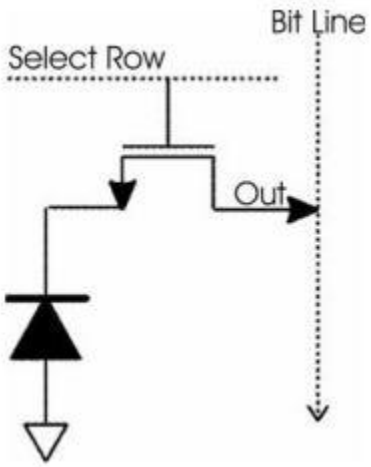


Figure 2.5: A photodiode-type PPS schematic[4].

2.6.2 Active Pixel Sensor, 3T-APS

The APS is named after its active element which amplifies the signal in each pixel[3, 12], as shown in Figure 2.6. By introducing amplification at a pixel, the performance of the pixel will be improved. The conventional APS pixel configuration is called 3T-APS since it consists of 3-transistors and one photodiode (PD) in each pixel.

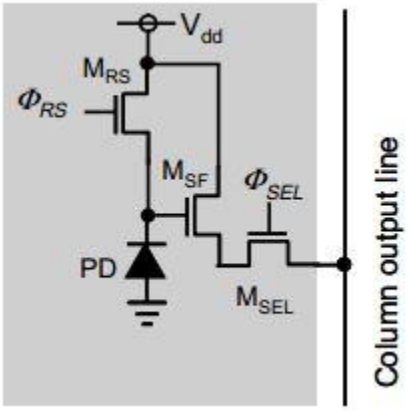


Figure 2.6: Basic pixel circuits of a 3T-APS[12].

The three transistors in each pixel are called as reset transistor M_{RS}, source follower transistor M_{SF} and select transistor M_{SEL}. The M_{RS}transistor acts as a reset transistor, where it reset the junction capacitance of the photodiode (PD). Transistor M_{SF} operates as a source follower that converts the accumulated charges at PD to voltage at its gate. Thus the output voltage follows the PD voltage. While, in PPS the accumulated charges are straightly to the outside of a pixel. Finally, the transistor M_{SEL} acts as an analog selection switch after the signal is transferred to a horizontal output line through this M_{SEL}. Meanwhile, the accumulated charges at PD are not destroyed, which make it possible to read the signal multiple times.

Even though APS was believed can overcome some flaws that existed in PPS especially SNR and power dissipation is minimal compared to CCDs, 3T-APS however has issues that should be addressed. Firstly, this 3T-APS suffer from the difficulty to suppress k_BTC noise caused by the reset transistor. Secondly, this conventional APS faced the problem of having the photo-detection region and photo-conversion region at the same node that is the PD which causes the photodiode design is constrained.

2.6.3 Active pixel sensor, 4T-APS

4T-APS was developed to alleviate the issues with 3T-APS with only one additional transistor which is called transfer gate transistor M_{TG}.this additional transistor, M_{TG} acts to separate the photo-detection and photo-conversion regions by transferring the accumulated photo-generated carriers in photodiode (PD) to floating diffusion (FD) where the carriers are converted to a voltage. Figure 2.7 shows the pixel structure of the 4T-APS. The separation of these two regions allows the noise reduction that cannot be achieved by conventional APS, 3T-APS. This technique is called Correlated Double Sampling (CDS) method, which this technique not only could eliminates the k_BTC noise but allow could reduce the fixed pattern noise (FPN).

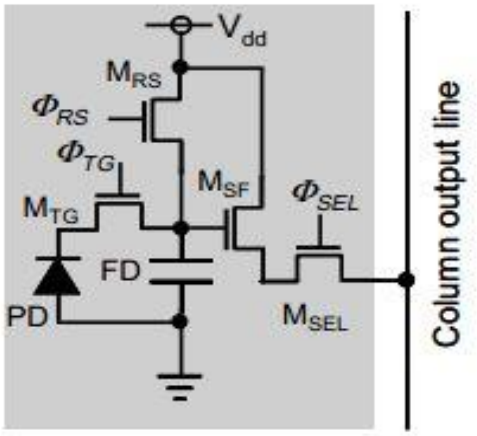


Figure 2.7: Pixel structure of the 4T-APS[12].

By this CDS operation, 4T-APS achieves low noise operation and thus could beat the performances of CCDs. It is noted that in the 4T-APS the accumulated charge must be transferred completely from the PD node to FD node. The incomplete charge transfer may affect the performance of the device and may cause image lag and noise as illustrates in Figure 2.8. This is where Pinned Photodiode (PPD) is required to ensure the complete transfer of the accumulated charge to the FD through the transfer gate.

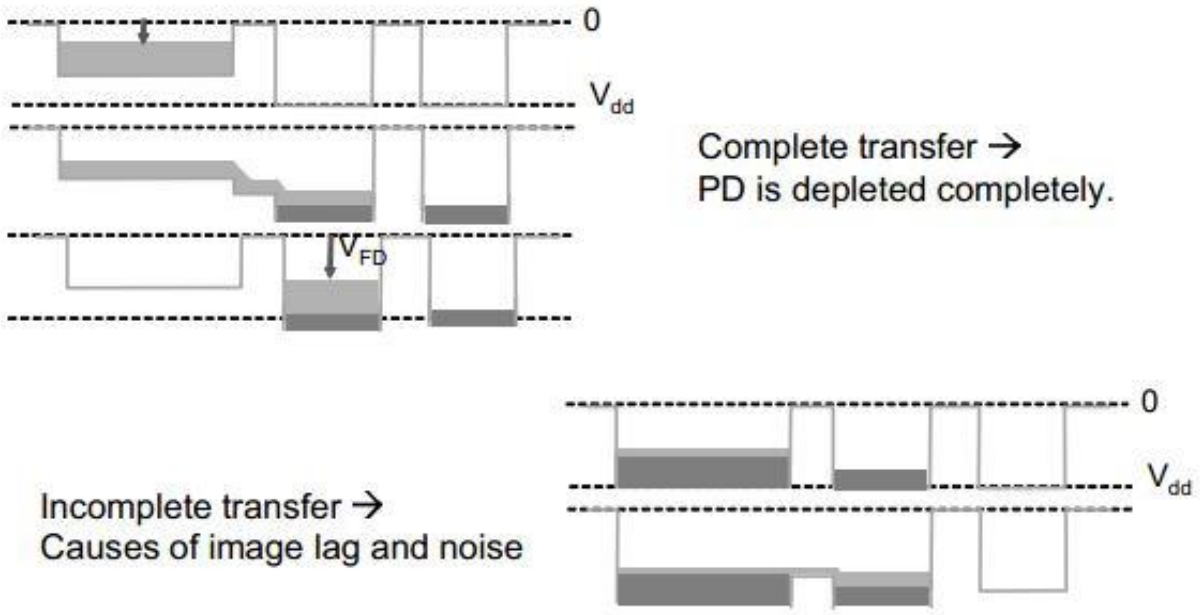


Figure 2.8: Incomplete charge transfer in a 4T-APS[12].

Even though 4T-APS surprassed 3T-APS in its low level noise, still there are several issues with 4T-APS, in addition to image lag that may occur when incomplete transfer of accumulated charge into FD. Those issues are additional transistor reduces the fill factor (FF) compared with 3T-APS and it is difficult to establish fabrication process parameters for the PPD, transfer gate, FD, reset transistor, and other units, for low and low image lag performance. Thus, for this research project, the conventional pixel, 3T-APS is chosen to be implemented for this CMOS image sensor (CIS) project.

2.6.4 Comparison Between Pixel Architecture

In this section, the comparison of three types pixel structure PPS, 3T-APS and 4T-APS are summarized in Table 2.1. Each pixel structure has their own strength and weakness in

different aspect with the others pixel structure. From that we could find the most suitable pixel structure for our devices depends on the purpose of the devices.

Table 2.1: Comparison of three types pixel structure PPS, 3T-APS and 4T-APS[3]

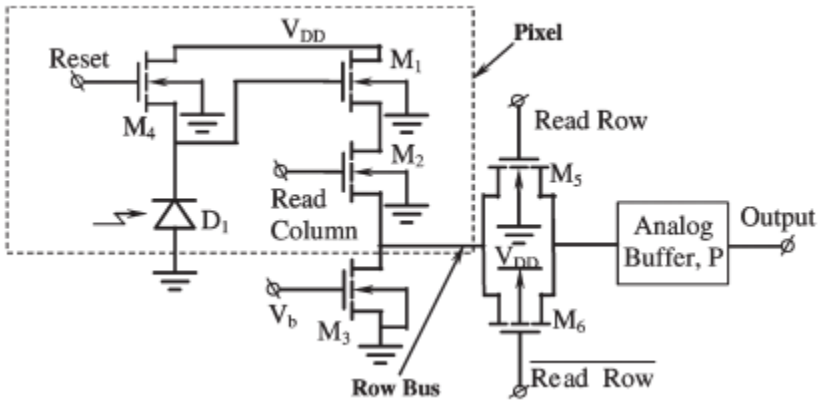
	PPS	3T-APS	4T-APS
Sensitivity	Depends on the performance of a charge amp	Good	Good
Area consumption	Excellent	Good	Fairly good
Noise	Fairly good	Fairly Good	Excellent
Dark current	Good	Good	Excellent
Image lag	Fairly good	Good	Fairly good
Process	Standard	Standard	Special
Note	Very few commercialized	Widely commercialized	Widely commercialized

2.7 Different Design of Active Pixel Sensor (3T-APS)

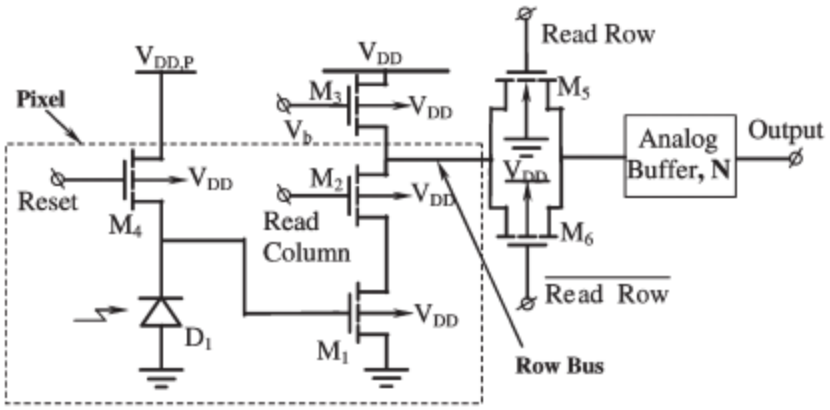
In general, design of CMOS image sensor (CIS) for this research project is based on the concept of active pixel sensor with three number transistors in a pixel with one photodiode, 3T-APS. 3T-APS are sensors that implement a buffer or amplifier per pixel. This APS consists of 2-D matrix of pixel, two addressing decoders for pixel selection by row and column, one decoder for reset of whole column, 1-D array of row switches and readout circuits, and analog buffers

[6]. The APS have three different design that are based on (a) nMOS transistor, (b) pMOS transistors, and (c) both nMOS and pMOS transistor as in Figure 2.9.

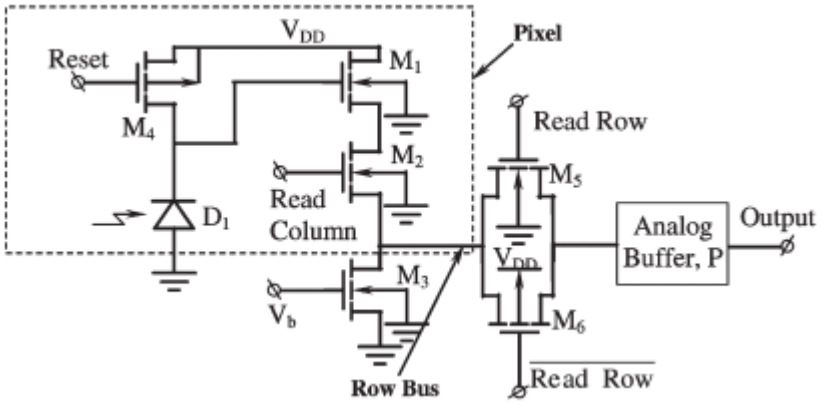
Each pixel employs one photodiode and three transistors. Photodiode is used to converts light into an electrical current and three transistors that operates as source-follower (M1), performs the reset of photodiode (M4) and operates as an analog selection switch (M2). Each transistor must perform their operation synchronously. This is important for image acquisition of very fast moving objects which requires both synchronous integration and low integration times, in order to avoid blur effects. For my design, the 3T-APS that based on nMOS transistors is chosen.



(a)



(b)



(c)

Figure 2.9: Different designs of APS based on (a) nMOS transistors, (b) pMOS transistors, and (c) both nMOS and pMOS transistors[7].

2.8 Sensor Peripherals

2.8.1 Addressing

A decoder or a scanner is used to address each pixel in a CMOS image sensor (CIS). A signal is obtained by scanning the pixel array with both row (vertical) and column (horizontal) scanner. There are two types of scanner that are commonly used to scan these pixels in CMMOS image sensor. These two scanners are shift register and decoder. For this research project, shift register is preferable since it has simple configuration compared to decoder. Other than has simple configuration, this shift register also has low flip noise generation and flexible readout. But decoder has greater scanning flexibility in compared to shift register.

Since in this CMOS imager, we just want to access the horizontal and vertical pixels, a shift register is enough to access both sides of pixel. Only a decoder is required, which is a combination of logic gates when it is involved of arbitrary pixel. A decoder arbitrarily converts N input data to 2^N output data using customized random logic circuits [2]. A typical scanner and decoder are shown in Figure 2.10 below.

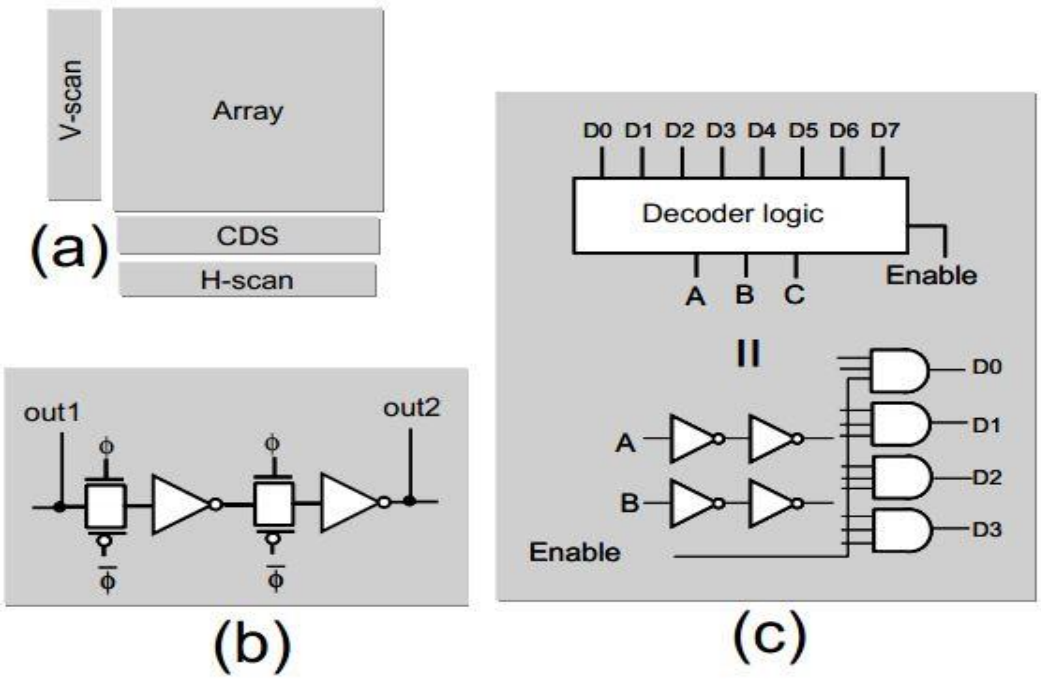


Figure 2.10: Addressing methods for CMOS image sensors: (a) sensor architecture, (b) scanner, (c) decoder[12].

2.9 Overall Architecture of CMOS Image Sensor

The first step is to design the circuits that are compatible for our project. We have to look for and do research on which would use in designing the circuits of CMOS imager. There are several topologies in designing the CMOS image sensor depending on their purposes. However, the main architecture of this CMOS imager can be divided into several main blocks as Figure 2.11 shows. Each block has its own functionalities and contributions for our circuit design as stated Table 1.3 with some additional blocks that do not shown in Figure 2.11.

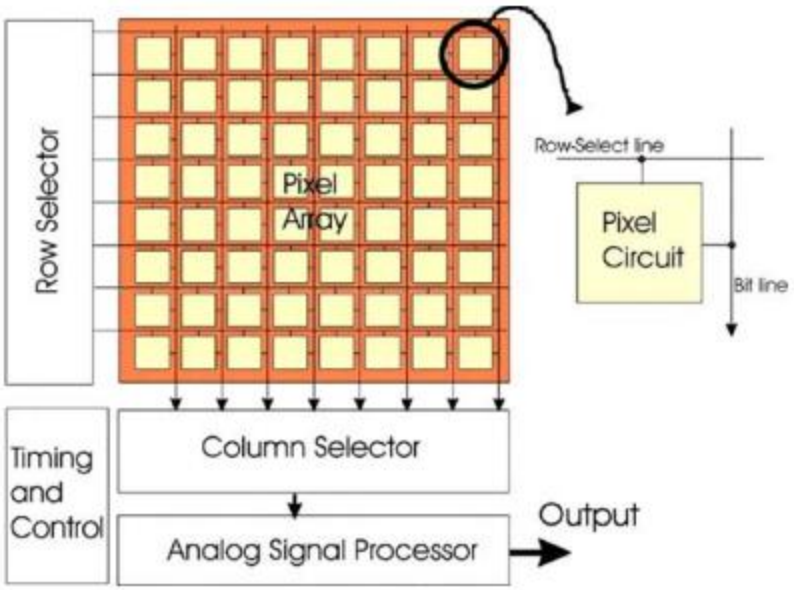


Figure 2.11: CMOS image sensor floor-plan [4]

Table 2.2: The function of on chip blocks of CMOS architecture

Module	Function
Timing and control	The overall control module provides the whole chip with proper time sequence
Pixel Array	Sensing the incident light and generating the charge signal
Column Selector	Shift register with buffers that selects the column of the Pixel Array to read or known as column scanner.
Row Selector	Shift register with buffers that drives the row logic of the Row Reader
ADC	Convert the pixel output analog signal to the digital signal
CPU & Memory	Stores the digital data outing of the processor

2.10 Summary

This chapter introduces the background of imaging sensor. Several research works is also being review in this chapter. The review of theoretical concepts that are related to this project are also provided in this chapter in order understand the project. Furthermore, this chapter also reviews several techniques used to detect the light based on previous works.