CURRENT STEERING DIGITAL ANALOG CONVERTER (DAC)

USING PARTIAL BINARY TREE NETWORK (PBTN)

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CURRENT STEERING DIGITAL ANALOG CONVERTER (DAC) USING PARTIAL BINARY TREE NETWORK (PBTN)

by

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LIST OF ABBREVIATIONS

ADC	Analog Digital Converter
BTN	Binary Tree Network
DAC	Digital Analog Converter
DEM	Dynamic Element Matching
DNL	Differential Non-Linearity
FRDEM	Full Random Dynamic Element Matching
GCN	Generalized Cube Network
INL	Integral Non-Linearity
LSB	Least Significant Bit
MSB	Most Significant Bit
PBTN	Partial Binary Tree Network
SFDR	Spurious Free Dynamic Range
TIA	Transimpedence Amplifier
OP-AMP	Operational Amplifier
CCCS	Current Controlled Current Source

ABSTRAK

Penukar Digital Analog (DAC) merupakan operasi penting dalam kebanyakan sistem digital yang memerlukan penukar data dari bentuk digital kepada bentuk analog. DAC bergantung kepada komponen terpadan untuk menjalankan penukaran data. Walau bagaimanapun, komponen terpadan sepenuhnya adalah hampir mustahil untuk dihasilkan, ralat tidak sepadan akan sentiasa berlaku yang menghasilkan perbezaan antara nilai yang diingini dengan nilai sebenar. Pemadan Elemen Dinamik (DEM) selalu digunakan untuk mengurangkan ralat tidak sepadan komponen. Teknik ini adalah satu teknik satu kod berpadanan bagi setiap masukkan digit blok DAC. Menggunakn teknik ini, purata masa bagi komponen setara disetiap kedudukan komponen adalah sama atau hampir sama bagi mengurangkan kesan komponen tidak sepadan dalam litar elektronik. Pengekodan yang rumit diperlukan bagi pengekod DEM konvesional yang akan menyebabkan transisi tersuis berlaku serentak berlakunya gelinciran di isyarat keluaran. Penyelidikan terdahulu telah berjaya menaikan sempadan penyelidikan PBTN ke 8-Bit .Dalam kajian ini, algoritma DEM adalah dicadangkan, dikenali sebagai rangkaian pokok perduaan separa (PBTN) ,dimana algoritma ini diperkenalkan pada kajian terdahulu.Penyelidikan ini bertujuan untuk menaikan sempadan penyelidikan terdahulu dari 8-bit ke 10-Bit .Selain itu, penggunaan CCCS untuk meninggikan arus yang digunakan pada kajian dahulu digantikan dengan Op-Amp.PBTN digunakan kerana ianya dapat mengurangkan kadar kerumitan sesebuah litar elektronik dan isyarat output yang mempunyai kurang gangguan jika dibandingkan dengan algoritma DEM yang lain.Kajian ini melaporkan keputusan simulasi 8-bit 1-MSB dengan DNL -0.550197255 LSB LSB, INL0.752682 LSB, pengunaan kuasa 16.7 mW manakala bagi simulasi 10-Bit 1-MSB memperolehi DNL -0.535378495 LSB, INL0.955382 LSB, pengunaan kuasa sebanyak 66.31 mw. Penggunaan kuasa dalam penyelidikan ini mencapai nilai jauh lebih rendah daripada penyelidikan sebelum ini.

ABSTRACT

Digital-to-analog converters (DACs) are essential operations in many digital systems which require data converters from digital form to analog form. DAC rely on the matched component to perform data conversion. However, matched components are nearly impossible to fabricate, there will always be mismatch errors which cause discrepancies between the desired value and designed value. Dynamic Element Matching (DEM) is commonly used to reduce component mismatch error. This technique is a randomization technique to select one of the appropriate codes for each of the digital input value before entering the DAC block. Using this technique, the time averages of the equivalent components at each of the component positions are equal or nearly equal to reduce the effects of component mismatches in electronic circuits. A complicated encoding is usually necessary for conventional DEM encoders which will lead to many of switch transitions happens at the same time and it will cause glitches in the output signal. Previous research is able to increase the boundaries of Partial Binary Tree Network (PBTN) to 8-Bits.In this research, DEM algorithm is used, known as Partial Binary Tree Network (PBTN) that been proposed from previous research that aims to push the boundaries of past research from 8-bits to 10-bits. Besides, in this research, the Current Controlled Current Source (CCCS) used to magnify the output current in previous research is replaced with operating amplifier. PBTN is used because it has lower complexity circuit and fewer glitches produce at the output signal. This thesis reports the simulation of 8-bit 1-MSB with DNL of -0.550197255 LSB, INL of 0.752682 LSB, the power consumption of 16.7 mW and for 10-Bit 1-MSB with DNL of -0.535378495 LSB, INL of 0.955382 LSB, the power consumption of 66.31 mW. Power consumption in this research achieved much lower than the previous research.

CHAPTER 1

INTRODUCTION

1.1 Background

In the modern digital system, most of the analog signals such as pressure, temperature, sound or images are converted to digital signals. Digital signal processors were designed to process digital signal effectively. Digital to analog converters (DACs) are used to convert the digital information back to an analog form. Digital signals advantage over analog signals is largely due to the fact that digital signals are more immune to noise and imperfections, problems which greatly hinders the precision of analog signals. Examples of such devices include loudspeakers, video displays, motors, mechanical servos, radio frequency (RF) transmitters, and temperature controls (Mercer, 2014). Figure 1-1 shows that the role of DAC in the digital signal processing system.

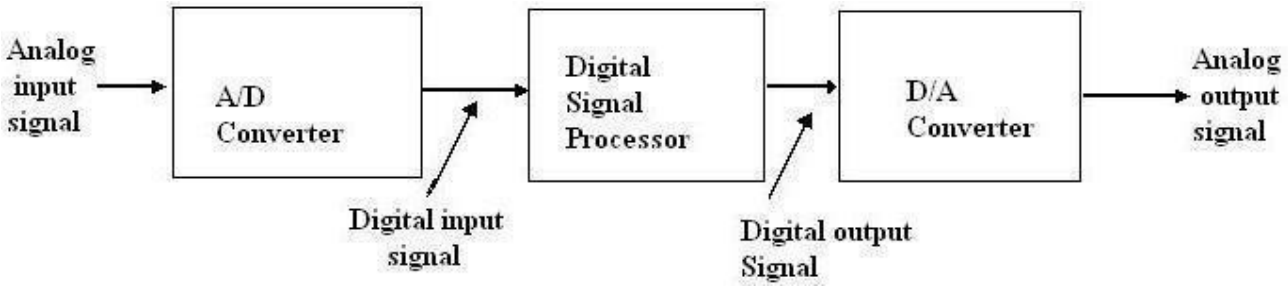

Figure 1-1 Basic block diagram of a digital signal processing system

Uncertainties in photolithographic edge definition result in mismatch value of component such as resistor ratios. Moreover, temperature gradients across the circuit, alignment error, component aging and component noise could cause a component mismatch. Several techniques were applied and introduced to reduce the effects of component mismatch errors. There are special VLSI

layout techniques, laser trimming, digital calibration, self- calibration, error averaging or dynamic element matching. (Gregoire and Un-Ku, 2008). In this research, a Dynamic Element Matching Technique, Partial Binary Tree Network algorithm (PBTN) is used which is introduced from previous research.

A complicated encoding is usually necessary for conventional DEM encoders which will lead to a lot of switch transitions happen at the same time and it will bring glitches to the output signal. In this research, a DEM algorithm is proposed on Current-Steering DACs with Partial Binary Tree Network (PBTN) algorithm to overcome glitches transitions with low complexity.

Uncertainties in photolithographic edge definition, etching error, and process variation result in mismatch value component such as resistor ratios from the ideal value. (Kuboki et al, 1982). Besides, component aging, component noise, temperature gradients across the circuit and alignment error may cause a component mismatch.

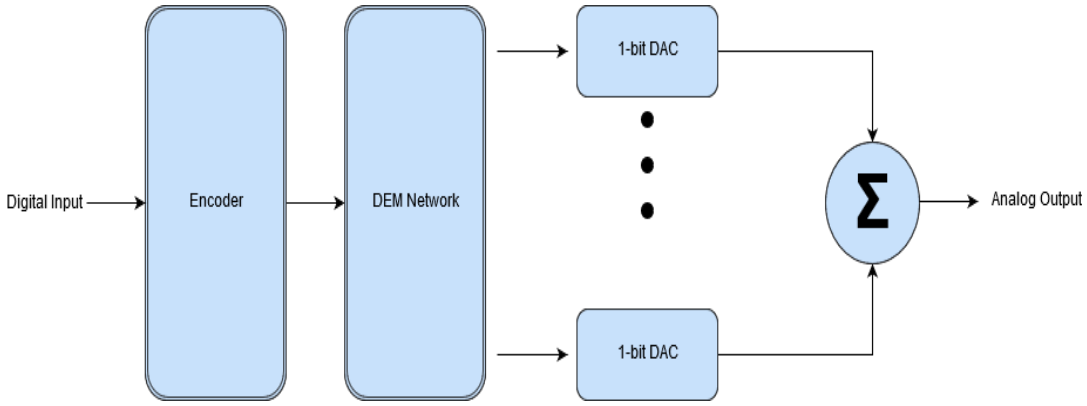

Figure 1-2 Structure of DEM DAC

1.2 Problem Statements

In order for DAC to perform data conversion, the matching of the components involved is an important criteria. A DAC produces a quantized (discrete step) analog output in response to a binary digital input code.(Mercer, 2014). Matched components are very difficult or nearly impossible to realize on silicon since mismatch errors always exist in real implementation. To achieve the desired output, most DAC designs depend on matched components, which is almost impossible to fabricate within a reasonable budget or timeframe. Other proposed DAC designs have utilized special design processes or laser trimming to minimize component mismatches, which unfortunately cannot be thoroughly eliminated and the procedure is expensive.

Dynamic element matching (DEM) is a design technique that is capable of reducing the effects of component mismatches in electronic circuits. This technique allows many possible input codes that introduce an error with randomization technique to select one of the appropriate codes for each of the digital input value before entering DAC block. With this technique, the time averages of the equivalent components at each of the component positions are equal or nearly equal to reduce the effects of component differences in electronic circuits (Bruce, 2000). Since the virtual positions of the components are randomized, harmonic distortions caused by mismatched components can be converted into white noise (Bruce, & Stubberud, 1998). The advantages of DEM is that it improves the dynamic performance such as spurious-free dynamic range (SFDR), as well as its static performance which is defined by differential nonlinearity (DNL) and integral nonlinearity (INL). (Guang Liang et al., 2012).

However, the drawback of implementing DEM is the resulting high hardware complexity for DAC where complicated encoding is needed for conventional DEM encoders which will result

in numerous switch transition and produces a glitch in the output signal. (Teh, 2014). Partial Binary Tree Network (PBTN) is a new DEM algorithm which possesses relatively lower hardware complexity. Fewer transmission gates are needed compared to Binary Tree Network (BTN), hence will have lower hardware complexity and reduced glitches.1-MSB PBTN only performs random switching on the 1-bit most significant bit (MSB).

1.2 Objectives

The main objectives of this research are:

- To design and simulate 8-bit PBTN DEM DAC in terms of power consumption.
- To design and simulate 10-bit PBTN DEM DAC in terms of INL, DNL and power consumption.

1.3 Scope of Research

The scope of this project includes the design, implementation, and evaluation of DAC. In addition, the aim of this project is to solve a problem commonly faced during the design of DACs, which are the mismatch error caused by the difference between the designed and the fabricated component value. To further improve on previous researchers on this algorithm, this research will also look to increase the resolution from 8-bit to 10-bit.

Further improvements can be done to reduce the glitches on the output of the DACs. Power consumption is an important critical design criterion for almost every electronic device and electrical systems. Lowering the power consumption can help to decrease the operating expenses, increases reliability, and allows a compact design.

1.4 Thesis Outline

This thesis begins with the introduction in Chapter 1, where the background, problem statement, objective, and scope are presented.

In Chapter 2, a literature review is presented, where various types of DAC architecture are explored and documented. 8-bit and 10-bit DACs are analyzed and compared in this chapter as well. DEM algorithms are studied, analyzed and compared to determine the advantages and disadvantages of each design.

The methodology is discussed in Chapter 3, where the designs of 1-MSB PBTN DEM DAC are presented.

Results and discussion are discussed in Chapter 4. The simulation results of 8-Bit1-MSB PBTN DEM DAC and 10-Bit 1-MSB PBTN DEM DAC are illustrated, together with performance metrics DNL, INL, and power consumption.

Chapter 5 houses the concluding remarks of this research, and future work to further improve on the proposed method.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In the real-world, signals such as pressure, temperature, sound or images are needed to be converted into digital form since modern digital systems can only process digital signals. Digital-to-analog converters (DAC) act as interfaces in between analog and digital domain. Electrical devices, such as loudspeakers, video displays, motors, mechanical servos, RF transmitters, and temperature controls required DACs to perform some real-world function.

Performance of the DAC is measured by Differential Nonlinearity (DNL), Integral Nonlinearity(INL), glitches impulse and power consumption of the whole circuit as it will affect the overall effectiveness of the system. This research will explore the implementations of DEM, with a newly proposed algorithm known as Partial Binary Tree Network (PBTN).

2.2 DAC Architectures

A DAC produces discrete and quantized analog signal that corresponds to a binary digital input. There is a different type of digital input codes that can be accepted as one of the digital input as shown in table 2.1.(Baker, 2010). Based on the digital input received, this enables switches that combine the number of fractions accordingly to produce the output. If a digital input has N bits, hence there will be 2^N possible levels of output voltage or current. The ideal input-output relationship of a 3 bit DAC is shown in Figure 2-1.

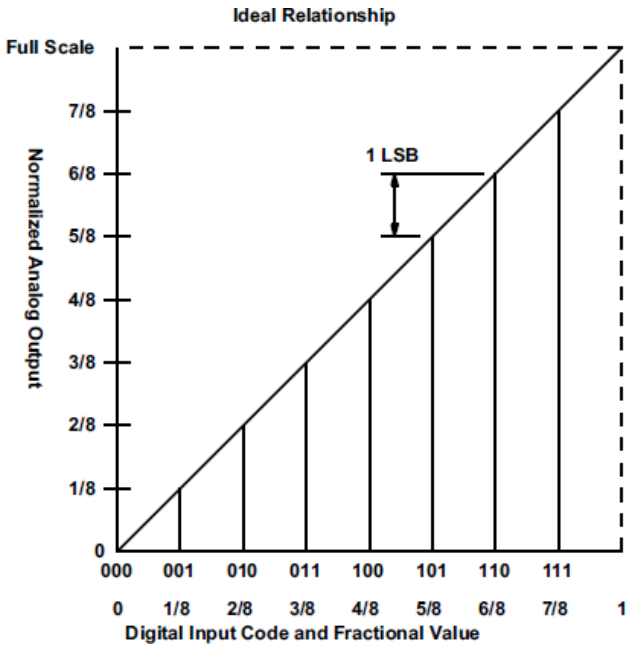

Figure 2-1 The ideal relationship (transfer function) between 3-bit digital input code and the analog fractional value output

Table 2.1: A comparison of different types of digital input codes

Decimal	*Binary*	*Thermometer*	*Gray*	*2'Complement*
0	000	0000000	000	000
1	001	0000001	001	111
2	010	0000011	011	110
3	011	0000111	010	101
4	100	0001111	110	100
5	101	0011111	111	011
6	110	0111111	101	010
7	111	1111111	100	001

2.2.1 String DAC

Binary-weighted architecture in which also known as the Kelvin divider, string DAC is the simplest DAC structure available and require quite complex analysis as shown in figure 2-2.In this architecture, 2^N resistors of equal resistance arranged in a series, where N is the number of input bits. The output is taken from the appropriate tap by closing one of the 2^N switches by decoding 1 of 2^N switches from the N-bit data.(Kester, 2008). Each resistor is connected to one switch, which is either open or closed depending on the input code. The current from each all the closed switches is summed up to attain the output current. (Kester, 2009).

Advantages:

- Simple architecture, inherently monotonic.
- Compatible with purely digital technologies.

Disadvantages:

- High element count and a larger area for higher bit resolution.
- High settling time for higher bit resolution.

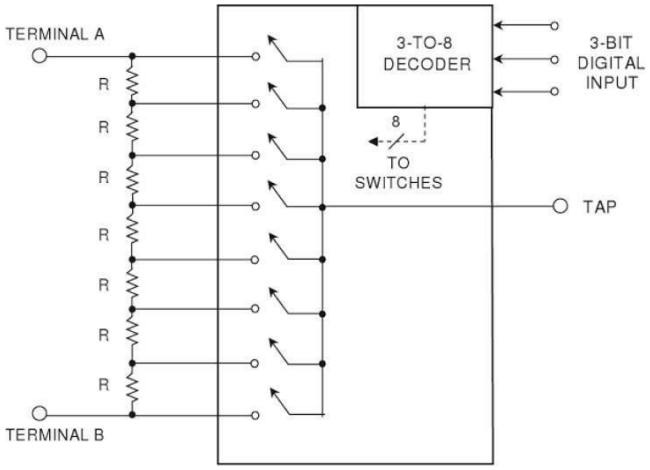

Figure 2-2 String DAC architecture

2.2.2 Oversampling DAC

Oversampling DAC is also known as Delta-Sigma DAC consists of a digital interpolation filter that encodes a high-resolution digital input signal f_c into a lower resolution. The higher sample frequency signal Kf_c is mapped to voltages by inserting extra data point. An analog filter will then smooth the output voltages as shown in figure 2-3.(Kester,2009).

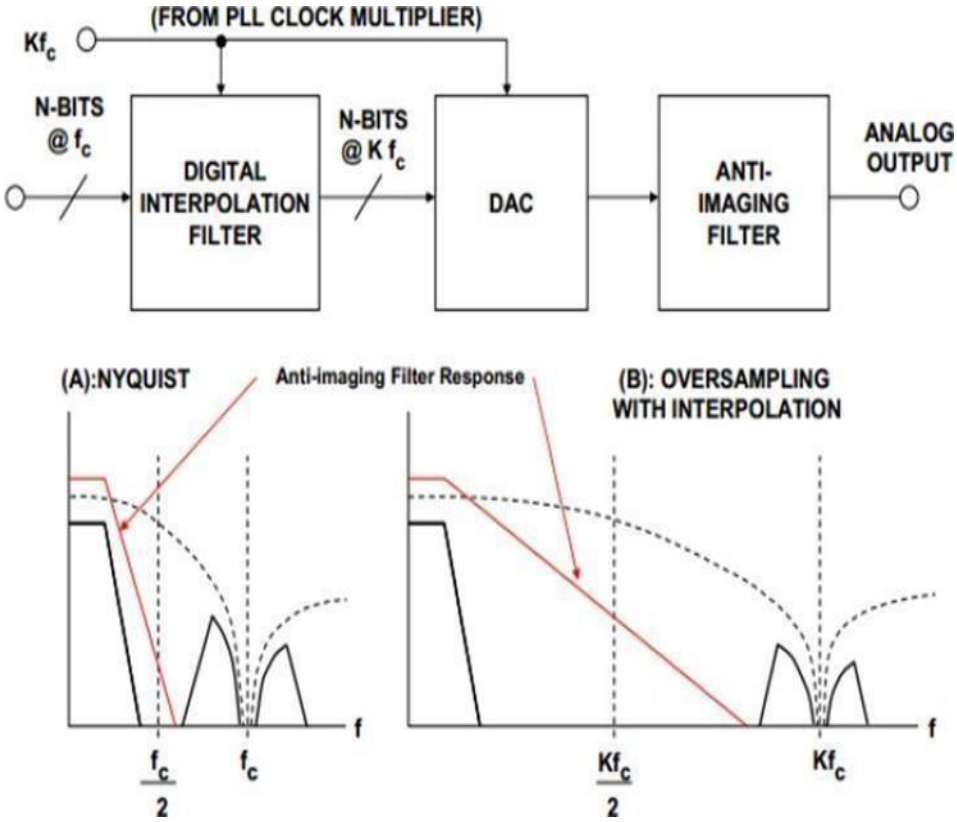

Figure 2-3 Oversampling DAC

2.2.3 Voltage Divider DAC

For this design, it is built by using a 2^N resistor with equal value where N is bit resolution. Each switch from 2^N switches is assigned to an input code. The output is determined by decoding 1 of 2^N switches to tap into a particular location on the resistor string. Figure 2-4 shows the voltage divider DAC.

Advantage:

- Totally monotonic voltage output, and low glitch (as only two switches operate during each code transition).

Disadvantage:

- High number or resistors or current sources required for higher resolutions in which increased the complexity of the circuit.

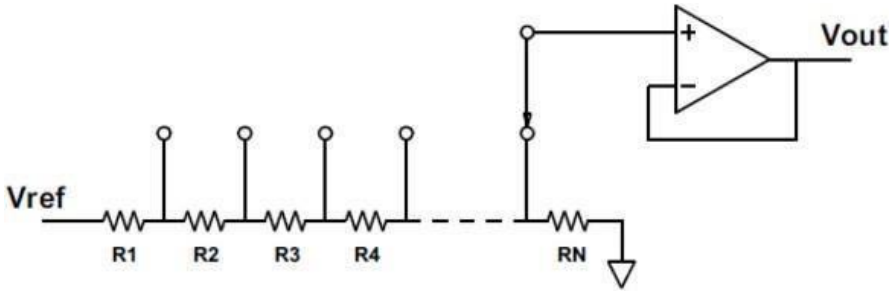

Figure 2-4 Voltage divider DAC

2.2.4 Segmented DAC

In this design, 2 or more DACs architecture is combined to utilize the advantage to construct a high-performance converter. For an example, one of the DAC architecture (binary weighted DAC) handles MSB while DAC architecture (resistor string DAC) handles LSB, and their output will be added together. Figure 2-5 shows a sample of segmented DAC. (Mercer, 2014).

Advantage

- Fast conversion speed with high precision.

Disadvantage

- Require high cost to build.

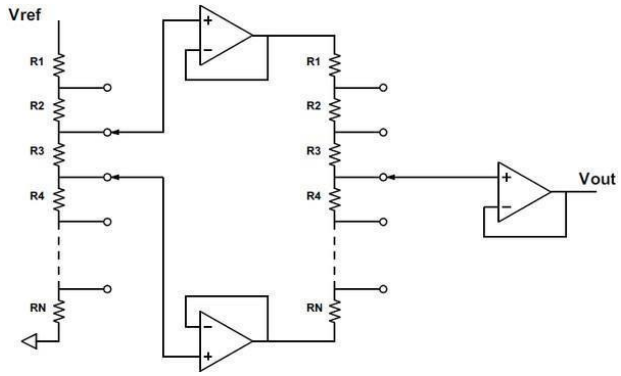

Figure 2-5 Segmented DAC

2.2.5 Current Steering DAC

This DAC architecture is composed of multiple current sources each connected to a switch controlled by the digital code inputs as shown in figure 2-6. The output current from each source was summed together to get the output.

Advantages:

- High performance in terms of INL and DNL.
- Suitable for generating high-frequency signals.

Disadvantage:

- High hardware complexity needed for the decoder in higher resolutions. (Myderrizi and Zeki, 2010).

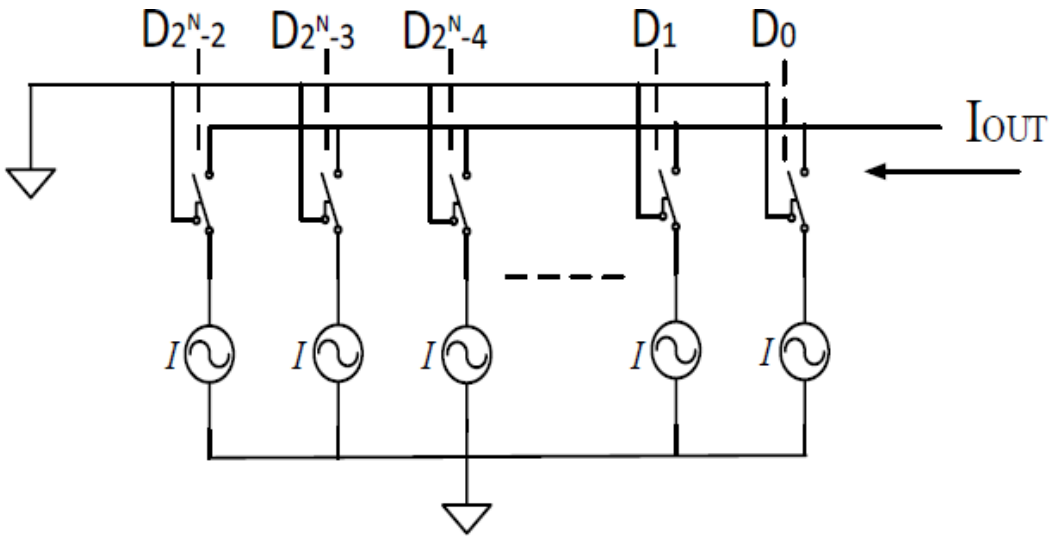

Figure 2-6 Current steering DAC

2.3 Dynamic Element Matching (DEM) DAC Architecture

DEM DACs is a technique used to reduce the effects of component mismatches. The average effect of component mismatch transformed into white noise by randomizing the position of input bit into DAC.(Galton,2010). Errors arising from component mismatches such as pulse shape, timing and amplitude can be eliminated. Figure 2-7 shows the general topology of a B-bit stochastic DEM DAC. The B-bit input data x(n) is passed through a thermometer coder to convert into 2^B – bit thermometer coded signal, t(n). t(n) and 2^B are mapped together and randomized. For example, output t(4) from DEM encoder was not connected to fourth DAC, instead, it was connected to a random unit DAC. By scrambling the usage pattern of the elements, DEM causes the error resulting from the mismatches to be pseudorandom noise that is uncorrelated with the input sequence instead of nonlinear distortion. Thus the dynamic performance such a the spurious-free dynamic range (SFDR) is increased.

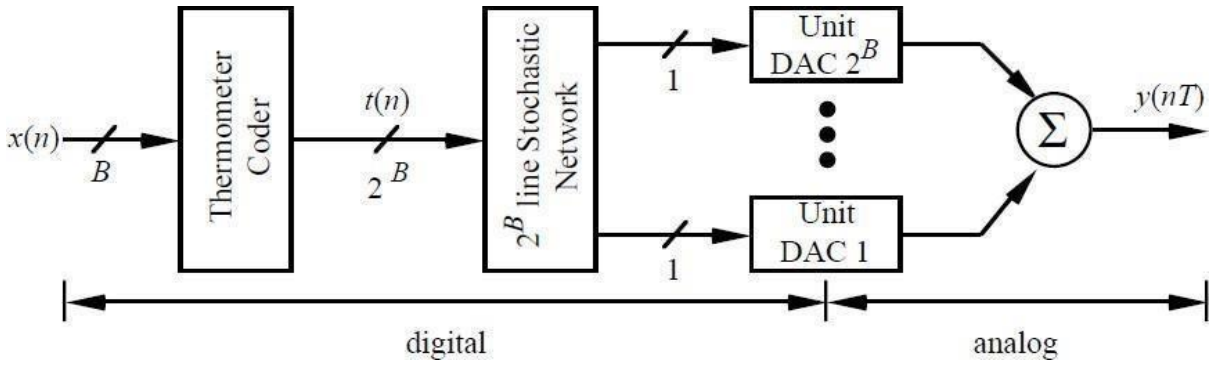

Figure 2-7 General topology of a B-bit stochastic DEM DAC

2.3.1 Full Randomization Dynamic Element Matching Network (FRDEM)

FRDEM networks are made up of switching block of FRDEM as shown in figure 2-8.The control signal $C_{k-1}(n)$ determined the virtual position of all bits. When the control signal is logical zero or (low) the k copies of LSBs sends to the lower output while the k copies of the MSB are sent to the upper output. When the control signal is logical one (high), the network sends *k* LSBs to the higher outputs, while *k* copies of the MSB are sent to the upper output. In other words, the case is reversed. (Bruce, & Stubberud, 1998).

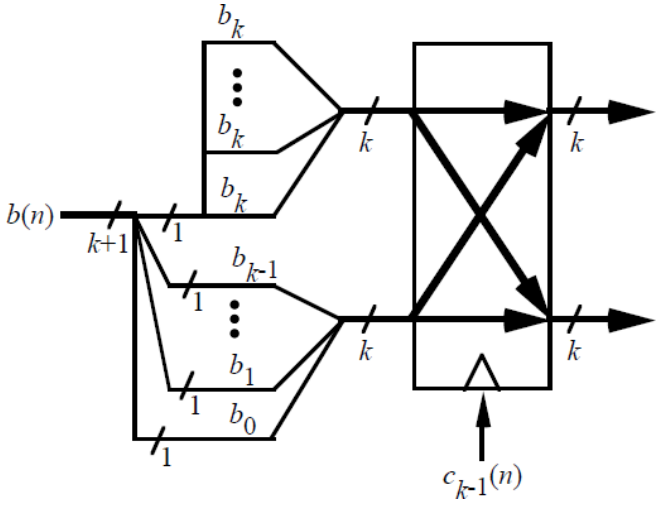

Figure 2-8 FRDEM switching block

2.3.2 Binary Tree Network

Binary tree network (BTN) is one of the implementations of Generalized Cube Network (GCN) on the operations of both the thermometer code and the 2^B line stochastic network.

A 1-bit BTN is shown in Figure 2-9. A k+1 bit BTN can be constructed using the topology as shown in Figure 2-10. (Bruce, & Stubberud,1998).

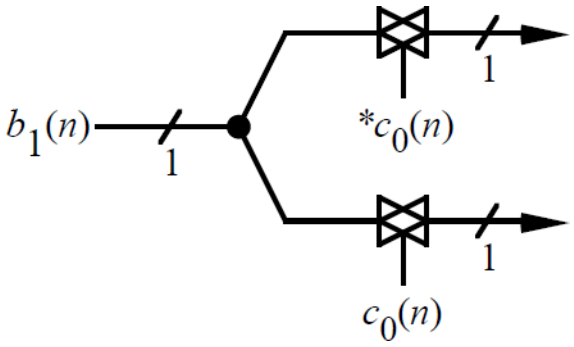

Figure 2-9 1-bit BTN

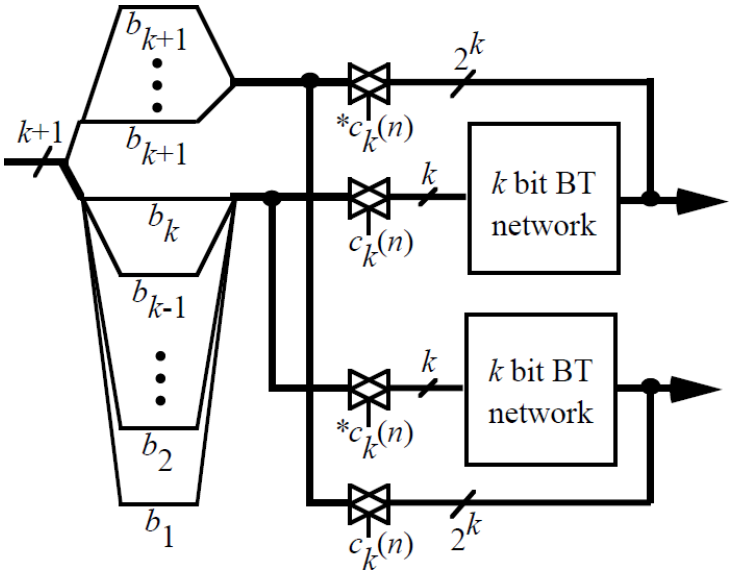

Figure 2-10 k+1 bit BTN

When the control signal $C_k(n)$ is logical zero (Low), the network sends 2^k copies of the input MSB to the upper output and k LSBs to the lower output.

When $C_k(n)$ is logical one (High), the network sends 2^k copies of the input MSB to the lower output and *k* LSBs to the upper output.

2.4 Static Performance

In static performance, there is an error such as offset error, gain error, differential nonlinearity (DNL) and integral nonlinearity(INL).It can be observed at the output of DAC when it is at steady state which is described by its transfer characteristics.(Duke,2013).

2.4.1 Offset Error

Offset error can be defined as a measurement of the shifting of the entire DAC transfer function whether shifted up or down. Figure 2-11 shows the example of offset error.

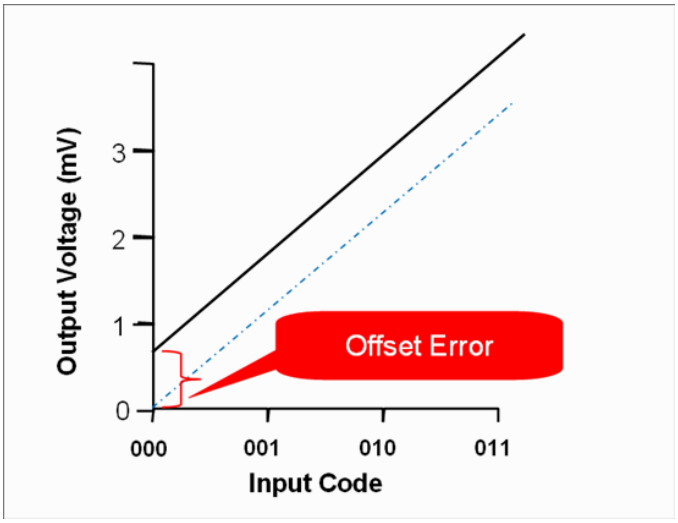

Figure 2-11 DAC offset error

2.4.2 Gain Error

Gain error compares how the real DAC transfer function's slope relates to the ideal slope. In the ideal case, the slope of the transfer function is equal to exactly 1 LSB, but frequently this figure is slightly off. The measurement for gain error is taken from the same two-point line of best fit used in measuring offset error. Figure 2-12 shows the DAC gain error.

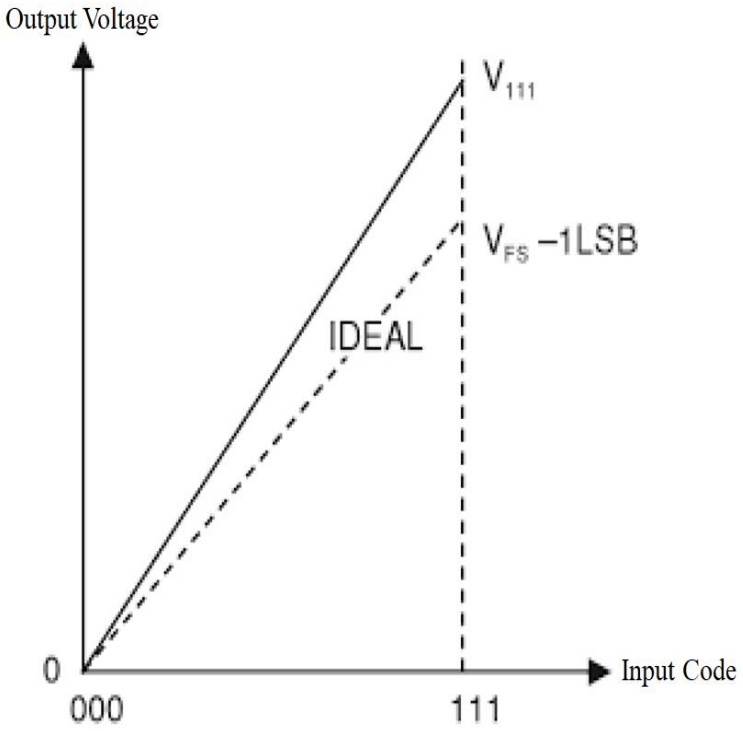

Figure 2-12 DAC gain error

2.4.3 DNL (Differential Non-Linearity) and INL (Integral Non-Linearity)

DNL measure the difference between measured or actual step height and ideal step height size for any two sequential DAC codes as shown in figure 2-13. DNL is often used to infer DAC monotonicity and to determine if the DAC has any missing codes. INL describes the deviation of each step between the ideal output of a DAC and the actual output of a DAC as shown in figure 2-14. In a lot of ways, INL is the most valuable specification to consider for an application that requires extremely high precision. (Duke, 2013)

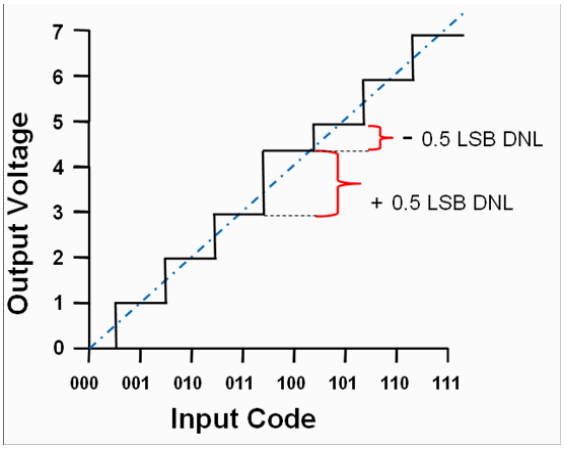

Figure 2-13 Differential nonlinearity (DNL)

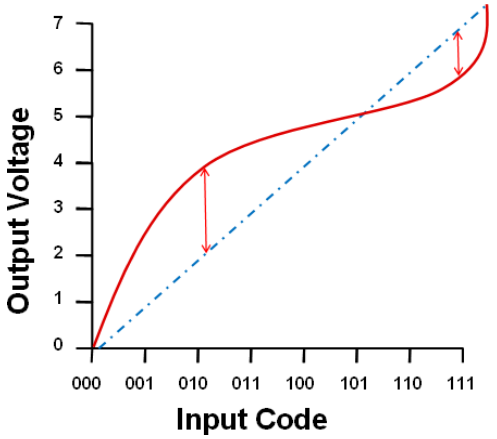

Figure 2-14 Integral nonlinearity (INL)

2.5 Dynamic Performance

Dynamic performance of the current-steering DAC is mainly affected by the mismatch-induced nonlinearity. (Wei Mao,2018). Equipment such as spectrum analyzer and oscilloscope is usually used to measures the DACs dynamic performance.

2.5.1 Settling Time

Settling time can be defined as the time required for a signal to settle within a range or loses its transient. The time taken for the output to exit the error band is one valid method to define settling time as shown in figure 2-15. (Kester,2009). Ideally, the settling time should be minimized to lower the distortions in the output waveform.

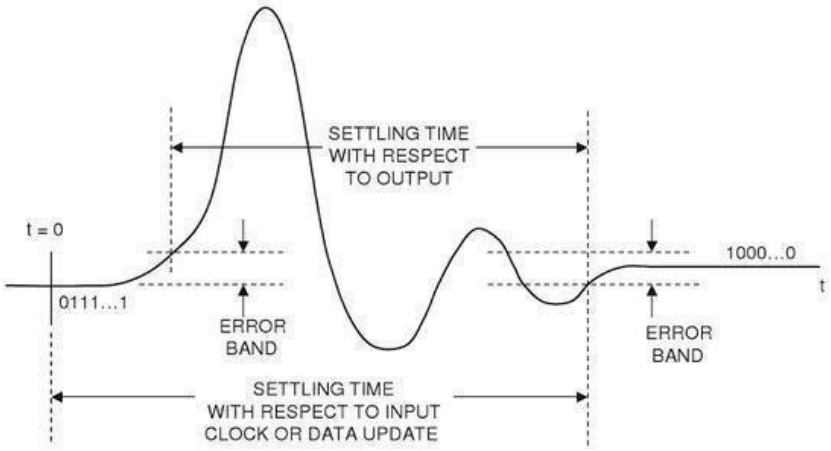

Figure 2-15 DAC settling time

2.5.2 Glitch

When DAC output changes from one code to another, the output of DAC is likely to overshoot, undershoot or both. Thus, a glitch happened as shown in figure 2-16. Glitches happen mostly due to propagation delays in a digital circuit. This problem is caused by the difference in switching time for different bits, and most noticeable when several bits change at once. (Myderrizi & Zeki, 2010).

For example, when an input bit changes instantly from 011111 to 100000, there is a change from 1 to 0 and 0 to 1 while the most significant bit might undergo change faster than all the other bits, this results in the output appears to be 111111 for a very brief amount of time. Such cases are predominant when the MSB has a different value than all the other bits. (Nesboe, 2010).

The glitch can be characterized by measuring the glitch impulse area. The positive and negative are summed up and cancel each other out and is approximated by considering the first four pulses of glitch only.

Techniques for glitch reduction (Ronak Shah,2016):

- Gate freezing.
- Balance path technique.
- Hazard filtering technique.
- Multiple threshold techniques

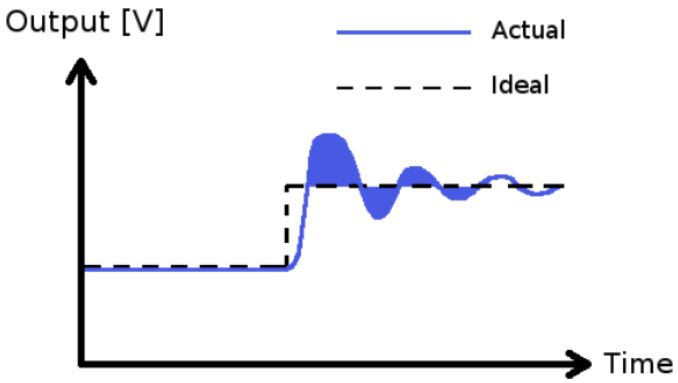

Figure 2-16 Actual output waveform showing glitch pulses, as compared with the ideal output waveform

2.5.3 Spurious Free Dynamic Range (SFDR)

SFDR can be defined as the measurement of the ratio of the fundamental signal to the largest harmonically or non harmonically related spur in the output as shown in figure 2-17.(Kester,2009).SFDR is the measure of the difference in amplitude between the fundamental and largest harmonically or non-harmonically related spur from direct current to the full Nyquist Bandwidth. (Garcia, 1995)

The equation to calculate SFDR is given by:

SFDR = RMS Fundamental Signal – Amplitude of Largest Spur

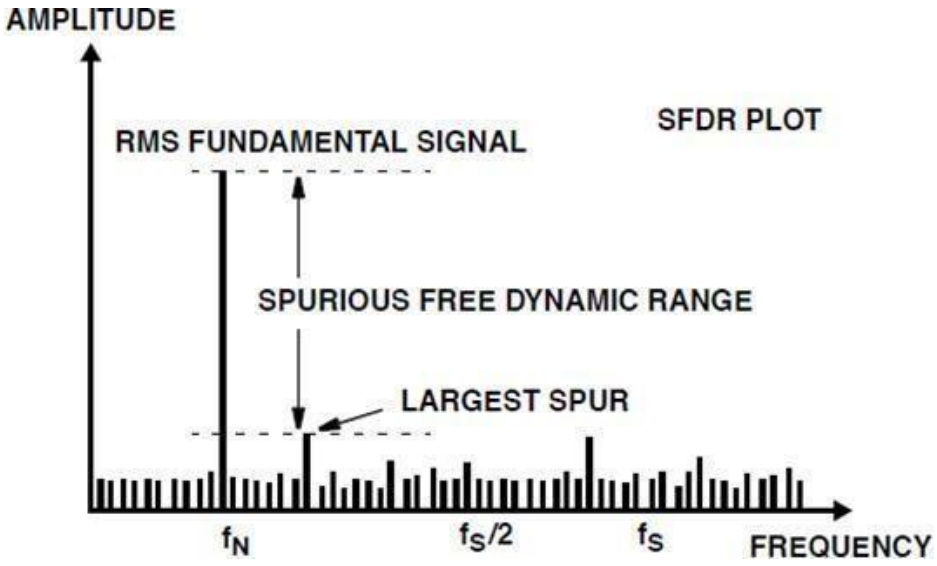

Figure 2-17 DAC spurious-free dynamic range (SFDR)

2.6 Operational Amplifier (Op-Amp)

An Op-Amp is needed as a voltage amplifying device designed to be connected with external feedback components such as resistors and capacitor. The feedback components are connected between its input and output terminals. The operation of the amplifier is determined by the configuration of the feedback components. (Ramakant, 2000). An op-amp consists of two inputs which are known as the inverting inputs with a negative sign (-) while the other input is non-inverting input with a positive sign (+). For the power supply, there is positive and negative supply and the vout is located at the output terminal of the op-amps. Figure 2-18 shows the schematic symbol for the op-amp.

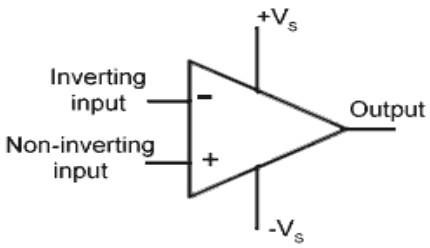

Figure 2-18 Schematic symbol for the op-amp

2.6.1 The inverting Op-Amp

The assumption made when dealing with the inverting op-amp is that the input error voltage is equal to zero so that the feedbacks keeps inverting the input of the op-amp at a virtual ground.(Bruce&Ron, 2009). Figure 2-19 shows the amplifier's inverting configuration. In inverting configuration, there is two resistor involves R_{in} and R_F. The R_F is connected between the output terminal (Vout) and inverting input terminal. The process of "feeding back" the output signal back into the input terminal happened. In addition, the non-inverting input has been grounded and the R_{in} is connected between the inverting input and the input signal source of voltage (Vin). The current flow in the input lead is assumed to be zero, hence current flowing through R_{in} is equals the current flowing through R_F.

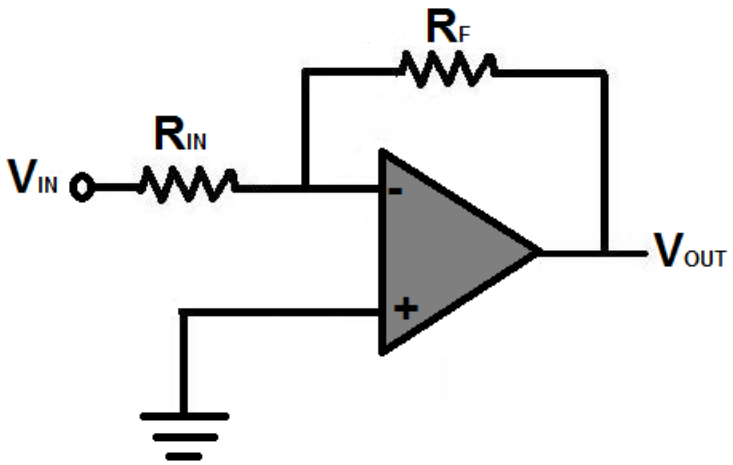

Figure 2-19 The inverting op-amp configuration

2.6.2 Transimpedence Amplifier (TIA)

Transimpendence amplifier (TIA) is also known as current to voltage converter. TIAs provide simple linear signal processing using an operational amplifier and a resistor for dissipating current. (Janet, 2016). Figure 2-20 shows the transimpedence amplifier configuration. The op-amp negative feedback forces a current equal to Iout to flow through the resistor R. Vout will be an analog voltage that is proportional to the binary input of DAC. Using Kirchhoff's Current Law (KCL), the sum of all currents flowing into a node is zero. Assumed that the op-amp is ideal meaning no current flows into the op amp +/- inputs, KCL gives the equation 2.1 and equation 2.2 below.

$$I + \left(\frac{Vout-0}{R}\right) = 0 \qquad (2.1)$$

$$Vout = -RI \qquad (2.2)$$

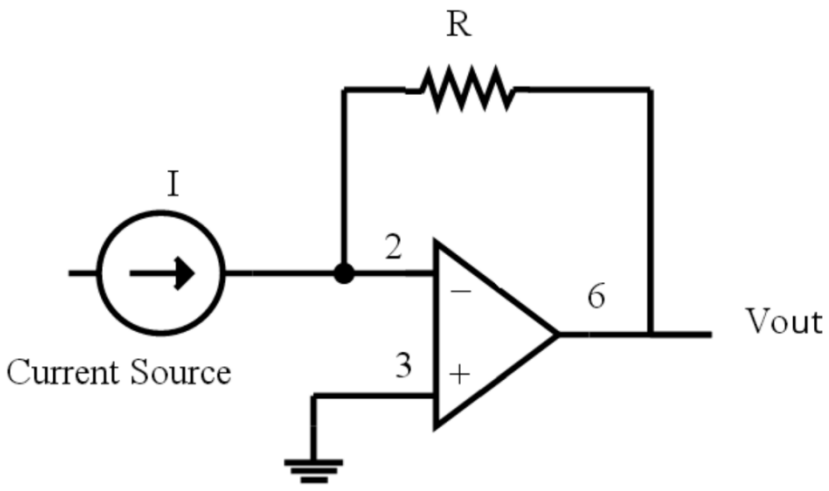

Figure 2-20 The transimpedence amplifier configuration.

2.7 Summary

In this chapter, there are different types architecture of DACs and Op-Amps discussed and introduced with each has different characteristics. Besides, different type architectures of DAC were identified with advantages and disadvantages.

Furthermore, DEM architectures are also discussed and introduced which include the FDREM and BTN. The performance of DACs was also reviewed and presented in which static performance can be measured by using INL, DNL, offset error and gain error while the dynamic performance include settling time, glitch and SFDR.