0.18 um CMOS Power Amplifier

for 2.45 GHz IoT Application

ANG WEI KEAT

UNIVERSITI SAINS MALAYSIA

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by

ANG WEI KEAT

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CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

ACLR	Adjacent Channel Leakage Ratio
ACPR	Adjacent Channel Power Ratio
ADE	Analog Design Environment
AM-AM	Amplitude to amplitude Modulation
AM-PM	Amplitude to phase Modulation
BLE	Bluetooth Low Energy
CCDF	Complimentary Cumulative Density Function
CMOS	Complementary Metal Oxide Semiconductor
DRC	Design Rule Check
ET	Envelope Tracking
EVM	Error Vector Magnitude
GaAs	Gallium arsenide
GaN	Gallium Nitride
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
IMD	Intermodulation Distortion
IMD3	Third Order Intermodulation Distortion
InP	Indium Phosphide
IoT	Internet of Things
IP3	Third Order Intercept Point
IC	Integrated Circuit
ISM	Industry, Scientific and Medical
LPF	Low Pass Filter

LVS	Layout Versus Schematic
nMOS	Negative Metal Oxide Semiconductor
OIP3	Third-order Output Intercept Point
PA	Power Amplifier
PAC	Periodic AC
PAE	Power Added Efficiency
PAR	Peak-to-average Ratio
PDK	Process Design Kits
PSS	Periodic Steady State
P1dB	1dB Compression Point
RF	Radio Frequency
RFID	Radio Frequency Identification
Si	Silicon
SP	S-parameter
VCO	Voltage Controlled Oscillator
VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless Fidelity
WLAN	Wireless Local Area Network

LIST OF SYMBOLS

f	Frequency
I_D	Drain Current
I_{DC}	DC Current
K_f	Stability K-factors
P_{DC}	DC Power
P_{in}	Input Power
P_{NOPC}	Power Output Capability
P_{out}	Output Power
V_{DC}	DC Voltage
V_{DS}	Drain-Source Voltage
V_{GS}	Gate-Source Voltage
w	Channel Width

0.18 um CMOS Penguat Kuasa

bagi 2.4 GHz Aplikasi Objek Rangkaian Internet

ABSTRAK

Sejak kemunculan industri Objek Rangkaian Internet (IoT) kebelakangan ini, permintaan pasaran kepada litar bersepadu dalam sistem komunikasi yang berkapasiti penghantaran data yang lebih tinggi dan penggunaan kuasa yang lebih rendah semakin meningkat. Oleh sebab itu, reka bentuk Penguat Kuasa (PA) Frekuensi Radio (RF) menjadi semakin mencabar dan penting. Dalam tesis ini, 0.18 um PA CMOS untuk 2.45 GHz aplikasi IoT telah dibentangkan. Rekabentuk PA terdiri daripada dua peringkat iaitu peringkat pemandu dan peringkat utama. Kedua-dua peringkat ini direka dalam konfigurasi peringkat tunggal yang terdiri daripada satu transistor di setiap peringkat. Dalam sudut prestasi, PA mampu menyampaikan keuntungan kuasa yang lebih daripada 20 dB dari operasi frequensi 2.4 GHz kepada 2.5 GHz. Kuasa pengeluaran maksimum yang dicapai oleh PA adalah 13.28 dBm. Oleh sebab sasaran PA itu adalah untuk diguna pada pemancar Bluetooth Tenaga Rendah (BLE), PA yang direka bentuk harus mencapai sekurang-kurangnya kuasa pengeluaran 10 dBm untuk menghantar isyarat dalam piawaian BLE. PA mempamerkan titik pemintasan pengeluaran tahap ketiga (OIP3) yang agak stabil pada 18 dBm sebelum kuasa pengeluaran PA mencapai 10 dBm. PA menunjukkan puncak kecekapan kuasa tambahan (PAE) sebanyak 17.82 % pada kuasa pengeluaran ialah 3 dBm. Oleh itu, PA direka mempamerkan pengeluaran yang lurus sehingga kuasa pengeluaran mencapai 10 dBm tanpa mengorbankan kecekapan dengan kadar yang tinggi. Pada operasi frequensi 2.45 GHz, PA mempamerkan nilai kestabilan,k-faktor melebihi 1. Oleh itu, PA mampu beroperasi dalam rantau stabil tanpa syarat. Selain itu, PA menunjukkan prestasi parameter-S yang baik iaitu S_{11} mencapai

sebanyak -10.36 dBm dan S_{22} mencapai -10.38 dBm. Prestasi PA ini dicapai dengan menggunakan kuasa elektrik sebanyak 1.8 V.

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ABSTRACT

Due to the emerging of the Internet of Things (IoT) industry in recent years, the demand for the higher integration of wireless communication system with higher data rate of transmission capacity and lower power consumption has increases tremendously. The design of Radio Frequency (RF) Power Amplifier (PA) is getting more challenging and crucial. In this work, a 0.18 um CMOS PA for 2.45 GHz IoT application is presented. The designed PA consists of two stages, which are the driver stage and output stage. Both driver stage and output stage utilise single stage common source transistor configuration. In the view of performance, the PA is able to deliver more than 20 dB gain in the frequency range of 2.4 GHz to 2.5 GHz. The maximum output power achieved by PA is 13.44 dBm. As the PA designed is targeted for Bluetooth Low Energy (BLE) transmitter, a minimum of 10 dBm output power should be achieved by PA to transmit the signal in BLE standard. The PA exhibits a nearly constant Third-order Output Intercept Point (OIP3) of 18 dBm before PA goes into saturated after 10 dBm output power. The PA shows a peak Power Added Efficiency (PAE) of 17.61 % at 13.24 dBm output power. Therefore, the designed PA exhibits good linearity up to 10 dBm output power without sacrificing much on the efficiency. At the operating frequency of 2.45 GHz, the PA exhibits stability k-factor, K_f value of more than 1 and thus the said PA is considered as unconditionally stable. Besides, the PA shows s-parameters performance of -7.91 dBm for S_{11} and -11.07 dBm for S_{22}. These performances of PA are achieved with input power supply of 1.8 V.

CHAPTER 1

INTRODUCTION

1.1 Background

Wireless communication system is vital in data communication to ensure data or information is transmitted wirelessly from one device to another device without requiring any cables. Hence, with the introduction of Internet of Things (IoT) concept in recent years, there is an increasing demand for the higher integration of wireless communication system with higher data rate of transmission capacity and lower power consumption. For example, in early days of mobile wireless communication, the mobile devices only carry the function of voice communication. However, with the advancement in data communication, the mobile device with only voice communication function doesn't satisfy the consumers' needs, but a mobile device with voice and video communication, multimedia functions and wireless internet access. Furthermore, a research from Cisco states that global mobile data traffic grew 63 percent in 2016 and expected to grow to 49 exabytes per month by 2021, a sevenfold increase over 2016 [1]. Hence, the modern wireless communication industry has devoted great effort to improve the current wireless communication systems including Wi-Fi, Bluetooth, WLAN and radar communication to compromise the higher data rate of exchange.

Bluetooth technology with Bluetooth Low Energy (BLE) standard has the advantages compared to other technologies in providing short range, low power and low cost method wireless communication. Bluetooth gadgets operate in 2.45 GHz ISM (Industry, Scientific and Medical) frequency band and have range of 1 m to 100 m [2]. ISM acts as a rule or standard for radio bands so that these radio bands are reserved internationally for the use of radio frequency (RF) energy for industrial, scientific and

medical purposes other than telecommunications. Bluetooth communication protocol can be classified into 3 classes based on signal transmission distance which are Class 1 (20 dBm output power), Class 2 (4 dBm output power) and Class 3 (0 dBm output power) [3]. The power amplifier which integrated in BLE transmitter must be designed to have at least 4 dBm output power in order to meet the Class 2 requirement [4]. However, the target output power is set to 10 dBm which is larger than required output power because there might be a downgrade of performance in power amplifier after fabrication process.

In order to send the Bluetooth signal out of the device, a Bluetooth transmitter is used. A Bluetooth transmitter consists of Voltage Controlled Oscillator (VCO), Up-converter, Power Amplifier (PA), Low Pass Filter (LPF) and antenna as shown in Figure1.1 [5]. The design of Power Amplifier is one of the most crucial aspects in designing a transmitter. This is because the Power Amplifier must be able to provide sufficient output power to overcome the path loss of the transmitter. Besides, a power amplifier with high efficiency is preferred to warrant a long working time of the portable IoT application device. However, there is a trade-off between the power efficiency and linearity. It is crucial for the power amplifier to possess high efficiency without sacrificing the linearity. A balance between efficiency and linearity has to be carefully considered in power amplifier designing. In this work. the power amplifier is targeted to possess power added efficiency (PAE) of 15 % and Third-order Output Interception Point (OIP3) of 18 dBm.

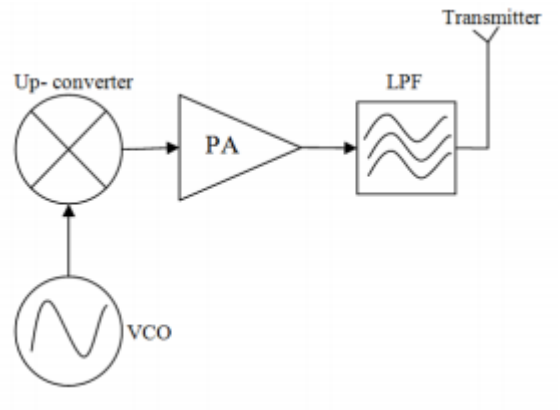

Figure 1.1 Block Diagram of a BLE transmitter [5]

Power amplifier is usually designed and fabricated by using III-V compound semiconductors such as GaAS, GaN, and InP materials. The power amplifier by these materials possesses better characteristics in power output ability and efficiency than that in Si CMOS technology [6]. Based on Table 1.1 which shows the performance comparison of each technology, the power amplifier based on Si CMOS technology possesses the lowest performance compared with other technologies. Furthermore, Si CMOS transistor has the substrate coupling and substrate loss problems which increase the complexity to integrate the whole transceiver into single chip [6][7]. However, Si CMOS power amplifier has the advantages of lowest power consumption, highest integration level, and lowest fabrication cost compared to other technologies.

Table 1-1 Performance Comparison of GaAs pHEMT, GaN HEMT, InP HBT and Si CMOS Technologies [6]

Performance	**GaAs pHEMT**	**GaN HEMT**	**InP HBT**	**Si CMOS**
Frequency range	High	Very high	Very high	High
Output power	High	Very high	Very high	Low
Efficiency	High	Very high	Very high	Low
Breakdown voltage	Low	Very high	Very high	Very high
Application field	Low	High	Low	Very high

1.2 Problem Statement

In this work, the power amplifier is designed by using 0.18 um CMOS technology. Besides CMOS technology, the power amplifier can also be designed and fabricated with III-V compound semiconductors such as Gallium Nitride (GaN) with High Electron Mobility Transistor (HEMT) technology and Gallium Arsenide (GaAS) with Heterojunction Bipolar Transistor (HBT) technology. The power amplifiers with these technologies have better performances in term of output power capability and efficiency of the power amplifier. However, the low power consumption and small size properties of CMOS technology made it more suitable for Internet of Things (IoT) application compared to III-V PAs [7]. It is known that, a radio frequency (RF) transmitter circuit may consist of several components such as Voltage Controlled Oscillator (VCO), Up-converter, Power Amplifier (PA) and Low Pass Filter (LPF). For that reason, the whole transmitter circuit can be implemented into single chip with smaller chip size if the power amplifier and other components are designed with CMOS technology.

There is a research proposed research which have high linearity and high efficiency Class-B power amplifiers design using GaN HEMT technology [8]. The said power amplifier possesses 48 % of saturated Power Added Efficiency (PAE) with 36 dBm of output power at 10 GHz. Another research proposed a low power CMOS power amplifier design for Radio Frequency Identification (RFID) and the Internet of Things (IoT) application [9]. The amplifier possesses 31.2 % PAE at 4.2 GHz operating frequency and 12.6 dB output power gain. By comparing these two, the power amplifier in GaN HEMT technology possesses better performances compared to the power amplifier in CMOS technology. However, Si CMOS power amplifier has the advantages over GaN HEMT technology in lower power consumption, higher integration level, and lower fabrication cost and these advantages make it more suitable technology to be used. Hence, one of the motivations of this project is to design a CMOS power amplifier which possess the performance close to HEMT power amplifier.

Moreover, power amplifier is subjected to trade-off between the power efficiency and linearity. A balance between efficiency and linearity has to be carefully considered in power amplifier designing. It is crucial for the power amplifier to possess high efficiency without sacrificing the linearity. Therefore, second motivation is to design a power amplifier which possesses high efficiency without sacrificing its linearity.

1.3 Objectives

The objectives to be achieved in this project are as follow:

1. To design a Power Amplifier with ability to deliver output power greater than 10 dBm by using 0.18 um CMOS technology.

2. To design a 0.18 um CMOS Power Amplifier with OIP3 and Power Added Efficiency (PAE) higher than 15 dBm and 15 % respectively at operating frequency of 2.45 GHz.

1.4 Scope of Project

The main motivation of the project is to design a low power CMOS Power Amplifier, PA for Internet of Things (IoT) application that follow Bluetooth Low Energy (BLE) standard by using 180 nm CMOS technology. The project scopes involve the schematic design and layout design of the PA. In schematic design, the PA design can be further divided into smaller parts which are PA output stage design, driver stage design, input and output impedance matching network design and biasing circuit design. Besides, the project scopes also involve the pre-layout simulation in order to verify the performance of the PA designed meets the targeted specifications. Furthermore, all of the designing steps are carried out by using the designing software tool of Cadence Virtuoso ADE with 180 nm CMOS technology Process Design Kits (PDK) provided by Silterra.

1.5 Thesis Organization

This thesis consists of five chapters. Chapter 1 provides a brief introduction to the project, this includes the overview of the low power CMOS power amplifier, problem statement, objectives, and scope of the project and organisation of the thesis.

Chapter 2 provides the literature reviews on the fundamental of power amplifier and the review on the power amplifier designs previously done by other researchers.

Chapter 3 presents the methodology of the project. The design specifications and the targeted performance are presented. Besides, the schematic and layout design steps and approaches are presented in this chapter.

Chapter 4 discusses on the results of the research. The results from the pre-layout simulation is presented and discussed.

Chapter 5 concludes the outcome of the research and discusses about the future work which can improve this research.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Wireless communication is a type of data communication in which the data or information is transmitted wirelessly from one device to another device without requiring any cables connections. Bluetooth technology is one of the examples of the wireless communication technology. Bluetooth technology has the advantages compared to other technologies in providing short range, low power and low cost wireless communication.[10]. In order to send the Bluetooth signal out of the device, a Bluetooth transmitter is used. It consists of Voltage Controlled Oscillator (VCO), Up-converter, Power Amplifier (PA), Low Pass Filter (LPF) and antenna [5]. The design of Power Amplifier is one of the most crucial aspects in designing a transmitter. Most of the signal output power is provided by power amplifier. Hence, a well-designed power amplifier plays a crucial role in getting a high performance Bluetooth transmitter.

In this chapter, the fundamentals of power amplifier are discussed. Firstly, the power amplifier design parameters are identified and discussed. Secondly, the power amplifier classes are discussed. After that, the power amplifier designs from other researches are discussed and a summary of comparison between these designs is made.

2.2 Power Amplifier Design Parameters

A power amplifier is defined as an amplifier which is used to amplify the signals delivered to the antenna to the desired level, without compromising signal integrity, so that receiver can recover the information transmitted by the transmitter. Before advancing to design a power amplifier, it is crucial to understand the fundamental of RF power

amplifier. The important design parameters of the RF power amplifier include output power, power gain, efficiency, power added efficiency (PAE), linearity, 1-dB compression point and intermodulation distortion (IMD).

2.2.1 Output Power

Output power is one of the importance performance parameters of power amplifier as output signal must acquire sufficient energy to be transmitted by the antenna. Output power is represented by dBm defined in Eq. (2.1)

$$P_{dBm} = 10log\frac{P_{out}}{10^{-3}} \tag{2.1}$$

where Pout is the real output power with Watt as its unit [6].

2.2.2 Efficiency

The power amplifier's efficiency is a measure of its ability to convert the dc power of the supply into the signal power delivered to the load [11]. Efficiency is defined as the ratio of output power at the drain to the input power supplied to the drain by the dc supply. It is described as in Eq. (2.2) [6].

$$Efficiency = \frac{P_{out}}{P_{DC}} \tag{2.2}$$

2.2.3 Power Added Efficiency (PAE)

In some cases, it is ineffective to use power efficiency to evaluate the power performance of a power amplifier because a power amplifier could get high efficiency with low power

gain. Therefore, power added efficiency (PAE) is used to evaluate the power performance of the power amplifier. It is defined as in Eq. (2.3)

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2.3}$$

where P_{in} is input power [6].

2.2.4 Power Gain

The power gain is defined as the ratio of output power to input power. It is described as in Eq. (2.4) [6].

$$Gain = \frac{P_{out}}{P_{in}} \tag{2.4}$$

2.2.5 Power Output Capability

Power Output Capability is the RF output power with peak drain voltage of 1V and peak drain current of 1A. It is used to describe power amplifier's output ability. This quantity is unitless and defined with as in Eq. (2.5) [6].

$$P_{NOPC} = \frac{P_{out}}{v_{Dmax} i_{Dmax}} \tag{2.5}$$

2.2.6 Linearity

Linearity of power amplifier is a criterion that represents how the quality of a given signal is maintained throughout the power amplifier. Linearity in power amplifier can be achieved by using linear amplifier or introducing the linearity enhancement techniques to switching amplifier.

Linearity of the system can be defined as 1dB compression point ($P_{1\text{-}dB}$), a third-order intercept point (IP_3), amplitude to amplitude modulation (AM-AM), amplitude to phase modulation (AM-PM), or third-order intermodulation distortion (IMD_3). Linearity of the system can be affected by harmonics, High peak-to-average ratio (PAR), complementary cumulative distribution function (CCDF), and the adjacent channel power ratio (ACPR), adjacent channel leakage ratio (ACLR), error vector magnitude (EVM) as shown in Figure 2.1 [12][13].

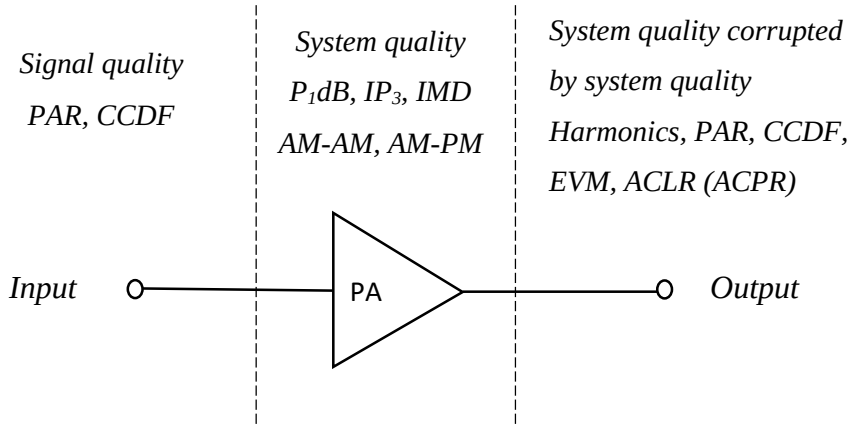

Figure 2.1 Linearity Indicator of PA [12]

2.2.7 1-dB compression point ($P_{1\text{-}dB}$)

Within the linear region, the amplifier has a constant gain over the frequency. However, in reality, the linear region ends at a specific frequency. After this frequency, the increase in input signal no longer contribute to the increase in output signal. The input 1-dB compression point is defined as the power level for which the input signal is amplified 1 dB less than the linear gain as shown in Figure 2.2 [14]. 1 dB compression point can be shown as input or output referred. After the 1 dB compression point, the amplifier is in nonlinear region. Hence, 1 dB compression point is used as a measure of linear range to describe the linearity of amplifier [12].

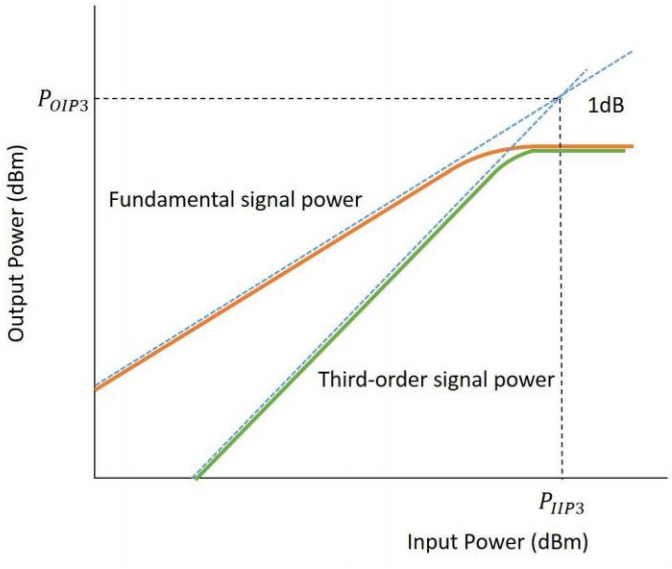

Figure 2.2 1dB compression point [14]

2.2.8 Intermodulation Distortion (IMD)

Intermodulation distortion is a nonlinear distortion composed by the fundamental frequency and harmonics present in the input signal. Figure 2.3 shows the intermodulation in an amplifier. Third order intermodulation products are most critical because they are closest to the fundamental frequency and this causes it difficult to be filtered out. They are produced at frequencies of $2f_1 - f_2$ and $2f_2 - f_1$ as shown in Figure 2.3.

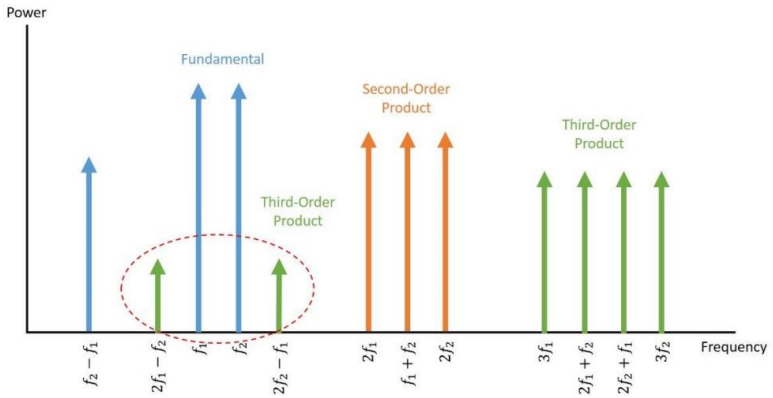

Figure 2.3 Intermodulation in an amplifier [14]

2.3 Classes of Power Amplifier

Power amplifier can be classed as linear and non-linear power amplifier. The difference between linear and non-linear power amplifier is that linear power amplifier generates an output signal that is proportional to their input signal without adding a high amount of harmonic power in the output signal, however non-linear power amplifier generates more harmonic power in their output compared to linear counterparts because they operate near the cut-off region of the transistor. Driving the transistor near the cut-off region has make the non-linear power amplifier to achieve higher efficiency, however come at a cost of a degraded output signal that is no longer proportional to input signal due to harmonics components.

Furthermore, power amplifier can be classed as two basic groups which are biasing type and switching type power amplifier as shown in Figure 2.4. The biasing type power amplifier consists of Class A, B, AB, and C which are classed based on their bias points and in turn their output current conduction angle. On the other hand, switching type power amplifier consists of Class D, E, F, and G which are classed based on their use of digital circuits and pulse width modulation signals to constantly switch the signal between ON and OFF driving the output into the transistors saturation and cut-off regions every time [15].

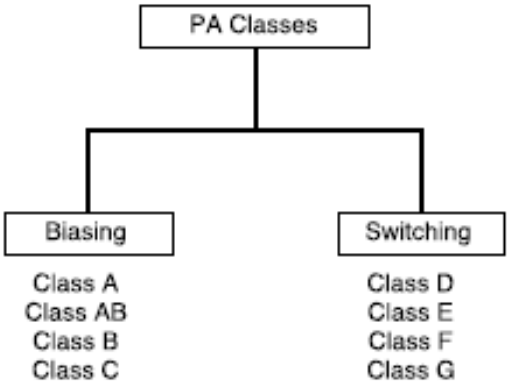

Figure 2.4 Different classes of power amplifier [15].

2.3.1 Class A Amplifier

Class A power amplifier is biased in saturation region. It has the conduction angle of 360 ° in which the transistor will be turned on over the whole output waveform. It possesses high linearity, high gain, and operates close to the maximum operating frequency of the transistor [6][16].

Based on load line and V_{DS} and I_D waveforms shown in Figure 2.5, the class A amplifier is biased in saturation region and this biasing condition gives the drain current of full cycle. Maximum efficiency is obtained when the drain voltage swings from 0 V to 2 V_{DC} as in Figure 2.5. The DC power is defined as in Eq. (2.6) while the output power is defined as in Eq. (2.7) [15].

$$P_{DC} = V_{DC} I_{DC} = \frac{V^2_{DC}}{R_L} \tag{2.6}$$

$$P_{out} = \frac{1}{2}\frac{V^2_{DC}}{R_L} \tag{2.7}$$

By substituting the Eq. (2.6) and Eq. (2.7) into Eq. (2.2), the maximum efficiency obtained is 50 %. The maximum efficiency of class A amplifier is the lowest among other class of amplifier as it conducts the current throughout the whole cycle of waveform [15].

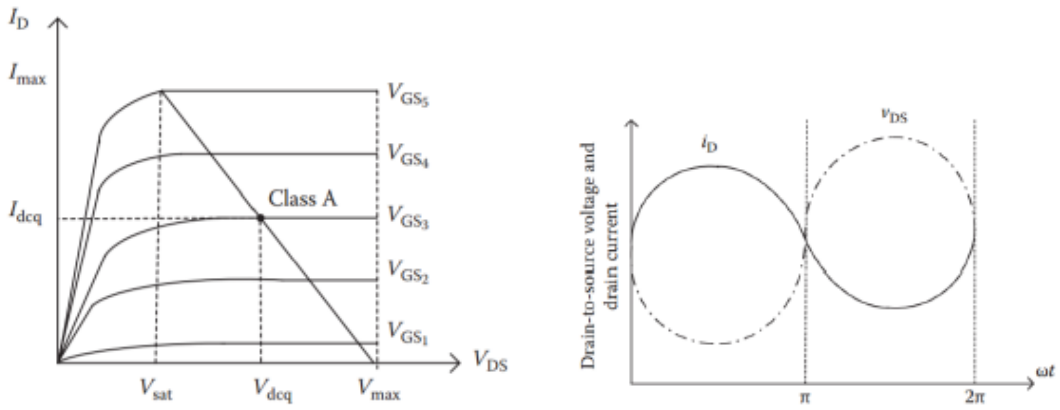

Figure 2.5 a) Load Line and b) V_{DS} and I_D waveforms of class A power amplifier [15]

2.3.2 Class B Amplifier

Class B power amplifier is biased close to cut-off region. The transistor is only turned on for half cycle of the output waveform.

Based on load line and V_{DS} and I_D waveforms shown in Figure 2.6, the class B amplifier is biased closed to cut-off region and a result only outputs a current for half of the cycle. Maximum efficiency is obtained when the amplitude of fundamental output voltage waveform is equal to V_{DC} and the DC power is calculated as in Eq. (2.8) as I_m is the amplitude of fundamental output current waveform. The output power can be calculated as in Eq. (2.9) [15].

$$P_{DC} = V_{DC} I_{DC} = \frac{2}{\pi} I_m V_{DC} \tag{2.8}$$

$$P_{out} = \frac{1}{2} V_m I_m = \frac{1}{2} V_{DC} I_m \tag{2.9}$$

By substituting the Eq. (2.8) and Eq. (2.9) into Eq. (2.2), the maximum efficiency obtained is $\frac{\pi}{4}$ = 78.5% [15]. The maximum efficiency of class B amplifier is higher than that of class A amplifier. However, class B amplifier shows poor performance in linearity

due to the higher order harmonics distortion. Class B power amplifier has the maximum theoretical efficiency of about 78.5% which is higher than Class A power amplifier (50%). However, Class B power amplifier creates a great amount of distortion because it only amplifies half signal wave cycle [13].

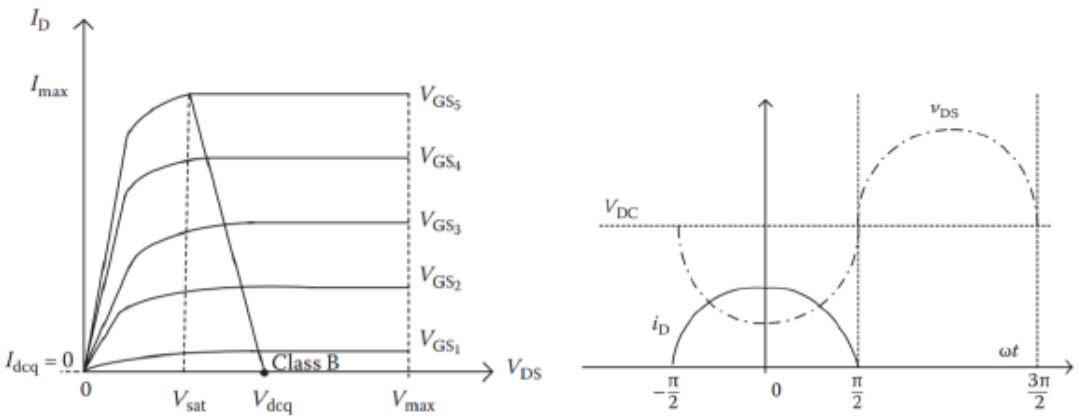

Figure 2.6 a) Load Line and b) V_{DS} and I_D waveforms of class B power amplifier [15]

2.3.3 Class AB Amplifier

Class AB power amplifier is chosen as a good trade-off between class A and class B amplifiers. Class A amplifier has good linearity but poor efficiency. On the other hand, class B amplifier sacrifices the linearity for efficiency.

Based on V_{DS} and I_D waveforms shown in Figure 2.7, class AB amplifier has the conduction angle lying in between 180 °and 360 °and thus its bias point has to be chosen somewhere in between that of the biasing points for class A and class B. In ideal case, the maximum efficiency of class AB amplifiers lies between 50 % and 78.5 %, depending on the bias point chosen [15].

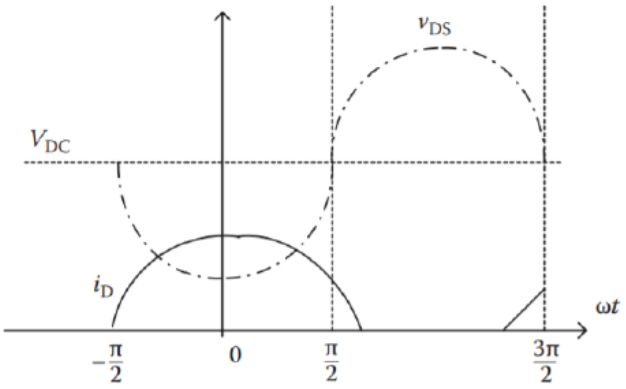

Figure 2.7 V_{DS} and I_D waveforms of class AB power amplifier [15]

2.3.4 Class C Amplifier

Class C power amplifier is biased at the point below the cut-off region and with a conduction angle lower than 180 °. Figure 2.8 shows a typical V_{DS} and I_D waveforms for class C amplifier.

Theoretically, in Class C power amplifier, the transistors work like switches in which the drain to source current is 0 when the transistor is switched ON. In this situation, the DC consumption is equal to 0 and drain efficiency is effectively 100 % [17]. Generally, the switch mode power amplifier has the higher efficiency than that of the current mode power amplifier.

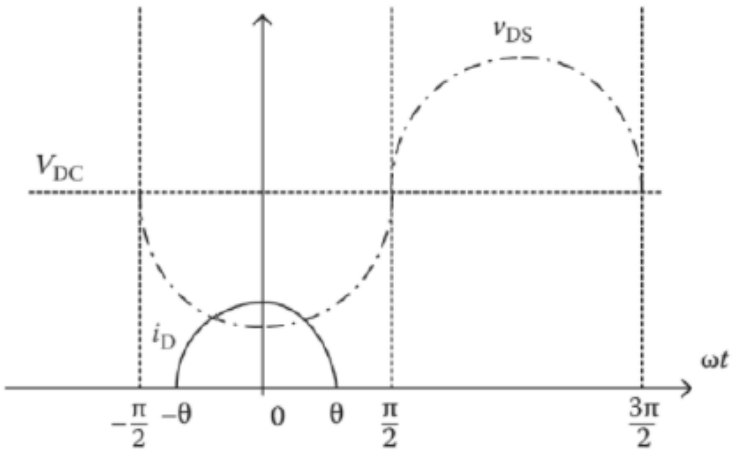

Figure 2.8 V_{DS} and I_D waveforms of class C power amplifier [15]

2.4 Power Amplifier of Previous Researches

2.4.1 Fully Integrated CMOS Power Amplifier with Discrete Gain Control

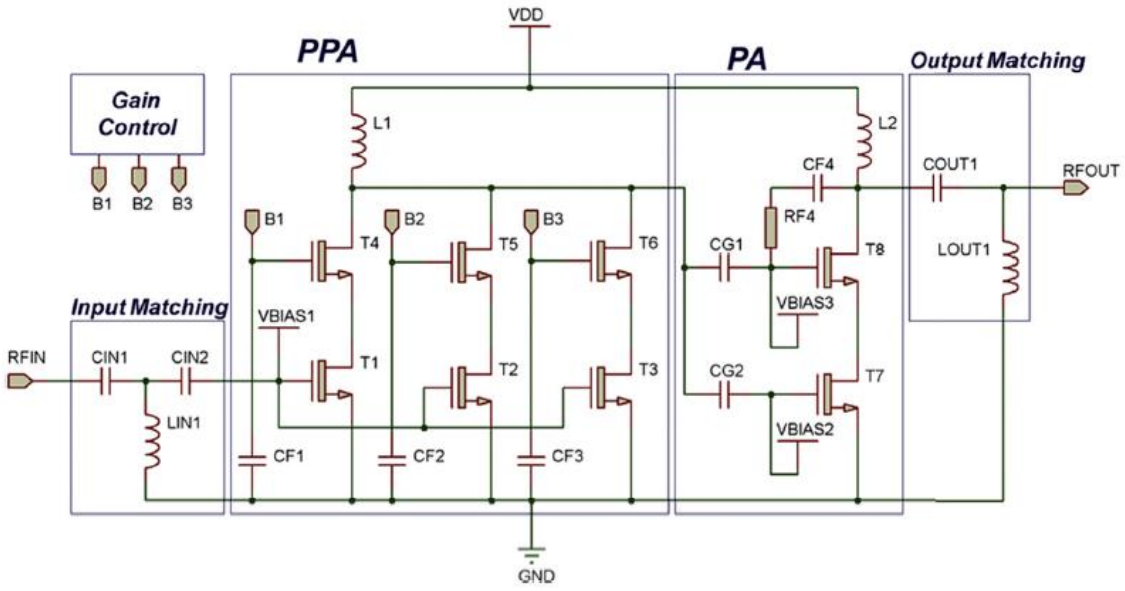

Figure 2.9 Fully Integrated CMOS Power Amplifier with Discrete Gain Control [18]

This research proposed a power amplifier which designed in 130 nm CMOS technology targeting the 2.4 GHz band [18]. Figure 2.9 presents the circuit topology of the power amplifier designed. The power amplifier consists of two stages. The first stage is the Reconfigurable Gain Stage (PPA) while the second stage is the Power Stage (PA).

At the Reconfigurable Gain Stage, 3 parallel cascade amplifiers are implemented to perform the gain variation. Each cascade cell is associated to controlling signal B1, B2, and B3 which serve as the biasing voltages for the transistors T4, T5 and T6. In order to enabling and disabling the cascade cells, VDD for enabling or GND for disabling is applied to the controlling gate of transistor. The transistor sizes of cascade cells are designed to be different and follow the 1:2:4 ratios in order to achieve sequential gain step. The channel width of the transistor T1 and T4 are 40 µm, T2 and T5 are 80 µm, T3 and T6 are 160 µm. The power gain increases as the channel width increases. By controlling the signal B1, B2 and B3, the effective channel width varies from 80 um (Mode 1), 120 um (Mode 2), 160 um (Mode 3), 200 um (Mode 4), 240 um (Mode 5) to 280 um (Mode 6).

The power stage is using the stacked configuration. The stacked configuration is used instead of cascade because in the cascade configuration, the input signal is solely direct into 1 transistor and the transistor breakdown voltage will limit the output swing, but in stacked configuration, the input signal is directed into 2 transistors, transistor T7 and T8 as in Figure 2.9 above.

The proposed power amplifier is able to achieve the gain ranges from 22.4 dB in Mode 1 to 31 dB in Mode 6. The power consumption is ranging from 171 mW in Mode 1 to 196.2 mW in Mode 6 while maintaining the output power larger than 15 dBm.

Moreover, it is observed that good input matching is obtained near 2.4 GHz with -14.6 dB S_{11} for Mode 6 and -22.5 dB for Mode 1.

2.4.2 Class-AB Power Amplifier with Integrated Phase Linearizer

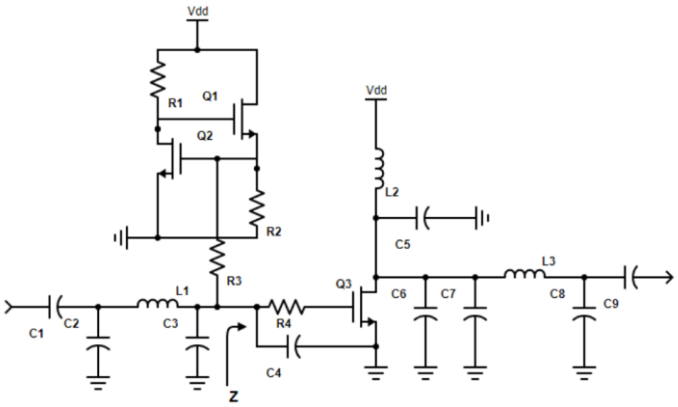

Figure 2.10 Class-AB Power Amplifier with Integrated Phase Linearizer [5]

This research proposed a Class-AB Power Amplifier design with Integrated Phase Linearizer [5]. The power amplifier is biased at Class AB with quiescent current of 14mA. A passive linearizer is integrated at the gate of CMOS transistor to cancel off the effect of Cgs capacitance which causes the nonlinearity effect to the power amplifier as shown in Figure 2.11. By having this linearizer, the linearity of power amplifier under low power condition is improved. Moreover, the design consists of input matching network and output matching network maximize the power transfer to the load. This power amplifier design can achieve an OIP3 of 20 dBm with max PAE of 38.4 % with linear dynamic range of 26 dB with CMOS 180 nm technology. Hence, this power amplifier design serves as a good solution to be integrated in a low power BLE transceiver [5].

2.4.3 Low Voltage Class-E Power Amplifier for Short Range Wireless Communications

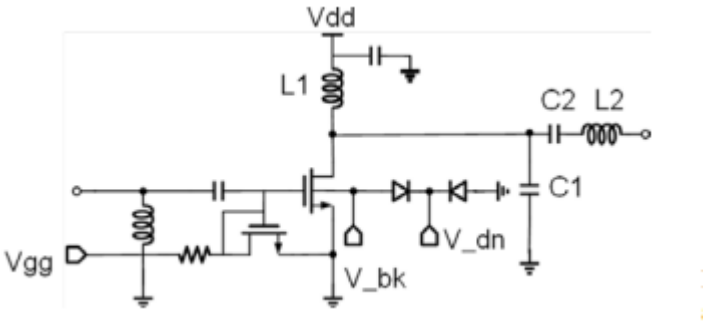

Figure 2.11 Low Voltage Class-E Power Amplifier for Short Range Wireless Communications [19]

This research proposed a low voltage Class-E power amplifier design for short range wireless communications [19]. The power amplifier is biased at class E with back gate effect by using CMOS 180 nm technology for 2.5 GHz band short-range wireless communication systems as shown in Figure 2.12. The class E power amplifier exhibits high efficiency but the dependence of the gain on the input power is highly nonlinear. Hence, the linearity of the power amplifier must be improved so that it could applied into transmitter system which employ the linear modulation. The nonlinearity is caused by the bias condition and load line of the amplifier. Thus, gate-to-source voltage is set to be slightly higher than V_{TH} and is applied to the transistor whereas the inductor L1 is optimized to achieve high efficiency with high gain linearity. The gate bias voltage is applied by a current mirror circuit.

The proposed amplifier can operate at supply voltage from 0.5 V to 1.5 V. The amplifier IC exhibits a P1dB of 6.9 dBm and a saturated output power of 10.7 dBm with a maximum drain efficiency of 36.4 % at a 1.0 V power supply. When the output power

is 10 dBm, a power gain of 7.4 dB and drain efficiency of 31.3 % are obtained. This work explicitly shows that modified class-E amplifier is effective for linear applications [19].

2.4.4 CMOS Power Amplifier Design for Low Power Wireless Sensors Network

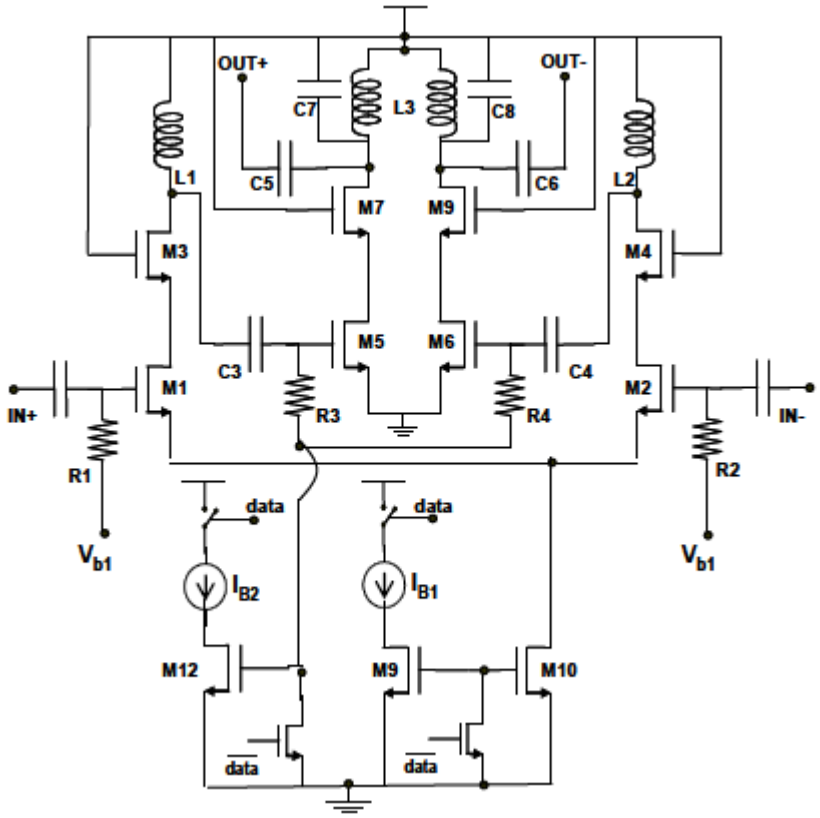

Figure 2.12 CMOS Power Amplifier Design for Low Power Wireless Sensors Network [20]

The reasearch proposed a power amplifier design for low power wireless sensors network. The power amplifier consists of two stages [20]. The first stage is the Differential Driver Stage and the second stage is the Output Stage as shown in Figure 2.10 above. The driver stage and the output stage are in differential topology. By using the differential approach,

the signal swing is effectively doubled as there is a pair of signal terminals. VDD node and common source nodes become ac grounds at fundamental and odd harmonic frequencies and therefore the ground bond-wire effects are reduced.

The driver stage is biased in class A mode. A resistive voltage divider is used to derive the bias voltage from power supply voltage. The output stage is biased slightly above the threshold with conduction angle of 260° in order to reduce the tranconductor's nonlinearity and improves the inter-modulation performance of amplifier.

The simulation shows that the power gain is 11 dB. Each of the output terminal is matched to 50 ohms. It is measured to have output power 6.89 dBm at the frequency of 2.47 GHz. The PA measured a peak PAE of 21 % and a PAE of 18 % at the nominal operating input signal level of -5 dBm. P_1-dB of amplifier is found to be 6.3 dB approximately for an input signal at -5 dBm.

2.5 Summary

The comparison between the different designs of power amplifier is carried out and tabulated into a table as shown in Table 2.1 below. From the table of comparison, it was noticed that power amplifier [19] has highest power added efficiency (PAE) of 36.4 % with average level of lower power gain and it was operated in 2.5 operating frequency. The power amplifier [19] has highest power added efficiency (PAE) because it uses the design of Class-E amplifier which has the high efficiency compared with other amplifier classes.

The power amplifier [5] has the second highest power added efficiency (PAE) of 33.3 % with the gain of 10 dB and it is working in the bandwidth of 2.45 GHz. Moreover, it has high output power which is 15 dBm when compared with other designs. The power

amplifier [5] is operated as Class-AB power amplifier. Class-AB power amplifier will compromise the high linearity in which high linearity is one of the importance criteria to be achieved in designing a power amplifier for RF transmitter.

The power amplifier [18] has the highest gain of 31 dB and output power of 15 dBm compared to other designs. It has the lowest efficiency in which its PAE value is 17.9 %. This power amplifier design consists of 2 stages which are the Reconfigurable Gain Stage (PPA) and Power Stage (PA). Reconfigurable Gain Stage (PPA) structure enable gain variation by varying the bias voltage and this contribute to power amplifier to achieve higher output power and overall gain. However, this power amplifier uses the CMOS 130 nm technology which is different from our project requirement. Its capability in achieving high gain and output power can be worked as the reference in the project.

In summary, the power amplifier design [19] is the most suitable design out of the others according to the application and design specications of the project. The technology used by their design is 180 um CMOS which is the same technology used in this project. Besides that, the power amplifier design proposed by the authors possesses the Power Added Efficiency (PAE) of 36.4 % which is the highest compared that of the other designs. Moreover, the power amplifier proposed possesses ouput power of 10.7 dBm at operating frequency of 2.5 GHz and the gain of 11.8 dB which match with the design specification in this project. In addition, the power amplifier design adopt simple amplifier configuration compared to other designs which implement complicated circuit design to improve the performance.