HIGH RESISTIVITY SILICON: DEEP-LEVEL DOPING COMPENSATION USING ELEMENTAL GOLD

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HIGH RESISTIVITY SILICON: DEEP-LEVEL DOPING COMPENSATION USING ELEMENTAL GOLD

by

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LIST OF ABBREVIATIONS

BESOI	Bond and etch-back silicon-on-insulator
BOX	Buried Oxide
CMOS	Complementary metal-oxide semiconductor
CPW	Coplanar waveguide
CZ-Si	Czochralski-silicon
ELTRAN	Epitaxial layer transfer
FZ-Si	Float-zone silicon
ITRS	International Technology Roadmap for Semiconductor
MMIC	Monolithic microwave integrated circuit
PSC	Parasitic surface conduction
SIMOX	Separation by implantation of oxygen
SOA	Silicon-on-anything
SOI	Silicon-on-insulator
SOS	Silicon-on-sapphire

SILIKON DENGAN KERINTANGAN TINGGI: PAMPASAN DENGAN PENGEDOPAN TAHAP MENDALAM MELALUI PENGGUNAAN UNSUR EMAS

ABSTRAK

Perkembangan pesat dalam peranti beroperasi pada kelajuan tinggi telah meningkatkan keperluan terhadap substrat dengan kerintangan yang tinggi. Kaedah tradisional untuk menghasilkan substrat tersebut dengan semikonduktor gabungan III dan V mengalami masalah kerumitan dan kos penghasilan yang tinggi. Penyelesaian alternatif seperti silikon-di-atas-penebat mempunyai isu kerosakan haba. Oleh itu, keperluan telah timbul untuk menghasilkan substrat dengan kerintangan yang tinggi melalui penggunaan silikon sebagai penyelesaian yang lebih murah dan kurang rumit. Kaedah pampasan dengan pengedopan tahap mendalam melalui unsur-unsur peralihan 3d telah dicadangkan untuk meningkatkan kerintangan untuk substrat silikon Czochralski jenis-p. Tujuan untuk tugasan ini adalah untuk menyelidiki potensi unsur-unsur peralihan sebagai dopant tahap mendalam bagi substrat silikon Czochralski jenis-n. Peningkatan dalam kerintangan untuk substrat silikon jenis-n yang dibekalkan oleh unsur-unsur peralihan yang dikaji, iaitu emas (Au), perak (Ag), kobalt (Co), paladium (Pd), vanadium (V), mangan (Mn) dan platinum (Pt) telah ditemui dan dianalisasi. Analisis atas plot-plot kerintangan silikon Czochralski dengan kepekatan fosforus latar belakang sebanyak 10^{14} cm^{-3} yang dipampas dengan unsur-unsur peralihan yang dikaji telah menunjukkan bahawa Au dan Ag ialah unsur-unsur yang paling baik untuk digunakan sebagai dopant tahap mendalam untuk substrat silikon jenis-n. Peningkatan dalam kerintangan teori yang tertinggi

diperuntukkan oleh Au and Ag ialah hampir empat peringkat magnitud, iaitu daripada 50 Ω-cm kepada $5x10^5$ Ω-cm dengan kepekatan Au atau Ag sebanyak 10^{15} cm^{-3}. Penggunaan Co dan Pd adalah tidak wajar oleh sebab keperluan untuk kemeresapan yang tinggi. V, Mn dan Pt telah disingkirkan kerana unsur-unsur tersebut tidak memberikan pampasan untuk substrat silikon jenis-n. Perbezaan ketara antara keputusan daripada pengiraan teori dan ukuran dibuat atas wafer silikon Czochralski jenis-n yang dipampas dengan Au, iaitu 500 kΩ-cm dan 80 kΩ-cm adalah oleh sebab kewujudan lapisan permukaan Au yang tidak aktif atas wafer silikon dan perbezaan sedikit dalam kedudukan andaian aras tahap mendalam Au dalam jurang jalur silikon yang digunakan dalam pengiraan.

HIGH RESISTIVITY SILICON: DEEP-LEVEL DOPING COMPENSATION USING ELEMENTAL GOLD

ABSTRACT

The rapid development of high speed devices increases the need for high resistivity substrate to improve noise isolation. The traditional method of using III-V semiconductor material for the substrate is associated with the problem of fabrication cost and complexity. Alternative solution such as silicon-on-insulator (SOI) has the thermal breakdown issue. Therefore, there is a need to produce high resistivity bulk substrate using silicon as a cheaper and less complex solution. Deep level doping compensation method using 3d transition element has been proposed to increase the bulk resistivity of p-type Czochralski silicon (CZ-Si) substrate. The purpose of this work is to investigate the potential of using transition elements as deep level dopants for n-type CZ-Si substrate. The enhancement of resistivity of n-type Si substrate provided by studied transition elements, i.e. gold (Au), silver (Ag), cobalt (Co), palladium (Pd), vanadium (V), manganese (Mn) and platinum (Pt) was determined and analyzed. The analysis on the resistivity plots of CZ-Si with background phosphorus concentration of 10^{14} cm^{-3} compensated using studied transition elements shows that Au and Ag are the best elements to be used as deep level dopants for n-type Si substrate. The highest theoretical resistivity enhancement provided by Au and Ag is about four order of magnitude, which is from 50 Ω-cm to $5x10^{5}$ Ω-cm with Au or Ag concentration of 10^{15} cm^{-3}. The use of Co and Pd are not desirable due to requirement of high solubility. V, Mn and Pt are disqualified as they do not provide compensation for n-type Si substrate. The significant difference between the results of theoretical calculation and measurement made on actual

n-type Au-compensated CZ-Si wafer, which are 500 kΩ-cm and 80 kΩ-cm respectively, is due to the existence of inactive surface Au layer on Si wafer and slight difference in assumed position of Au deep levels in Si bandgap used in the calculation.

CHAPTER 1
INTRODUCTION

1.1 Research Background

Monolithic microwave integrated circuit (MMIC) is a microwave circuit in which both active and passive components are fabricated on the same semiconductor substrate [1]. The development of MMICs has been augmented by the great demand for high-speed devices operating at microwave frequency ranging between 300 MHz and 300 GHz. Their advantages of being small, light, and cheap in large quantities have allowed the proliferation of high frequency devices such as cellular phones. MMICs have a large number of applications such as power amplifiers, low noise amplifiers, phase shifter, switches and mixer [2].

There is a need of high resistivity substrate in MMIC application for minimisation of substrate cross talk [3], [4] and transmission line loss [5], [6]. The III-V semiconductor materials such as gallium arsenide (GaAs), gallium nitride (GaN) and indium phosphide (InP) has been widely used in the production of high resistivity substrates due to their wide bandgap nature. However, III-V wafers are more expensive and fragile as compared to silicon (Si) [7]. Therefore, Si has been considered to be an alternative material for the III-V semiconductor compound due to less fabrication complexity and cost.

In 2009, International Technology Roadmap for Semiconductors (ITRS) has stressed the importance of high resistivity Si in radio frequency (RF) and analog/mixed signal (AMS) complementary metal-oxide-semiconductor (CMOS) application [8]. There have been efforts to use the silicon-on-insulator (SOI) and silicon-on-anything (SOA) technologies to produce high resistivity Si substrate. The SOI wafers can be produced by several methods: silicon-on-sapphire (SOS) [9], separation by implanted oxygen (SIMOX) [10], bond and etch-back SOI (BESOI) [11], Smart Cut™ [12], and epitaxial layer transfer (ELTRAN®) [13]. For SOS approach, a thin film of Si is epitaxially grown on sapphire substrate as shown in figure 1.1. On the other hand, the other four approaches use a similar cross section of SOI wafer as shown in figure 1.2(b) which consists of three layers: SOI layer (top layer), buried oxide (BOX) layer (middle

layer) and silicon substrate (bottom layer). The purpose of the BOX layer is to electrically insulate a fine layer of SOI layer (where the circuits are placed) from the rest of the Si wafer. The SIMOX approach uses implanted silicon dioxide, SiO_2 layer as the BOX layer to separate the top thin Si layer from Si substrate.

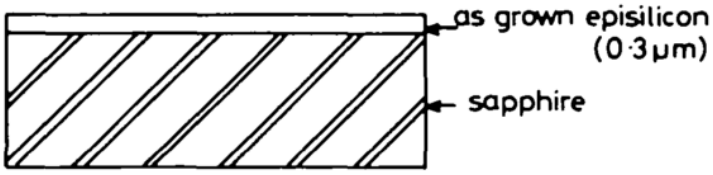

Figure 1.1: Cross-section of silicon-on-sapphire (SOS) wafer [14]

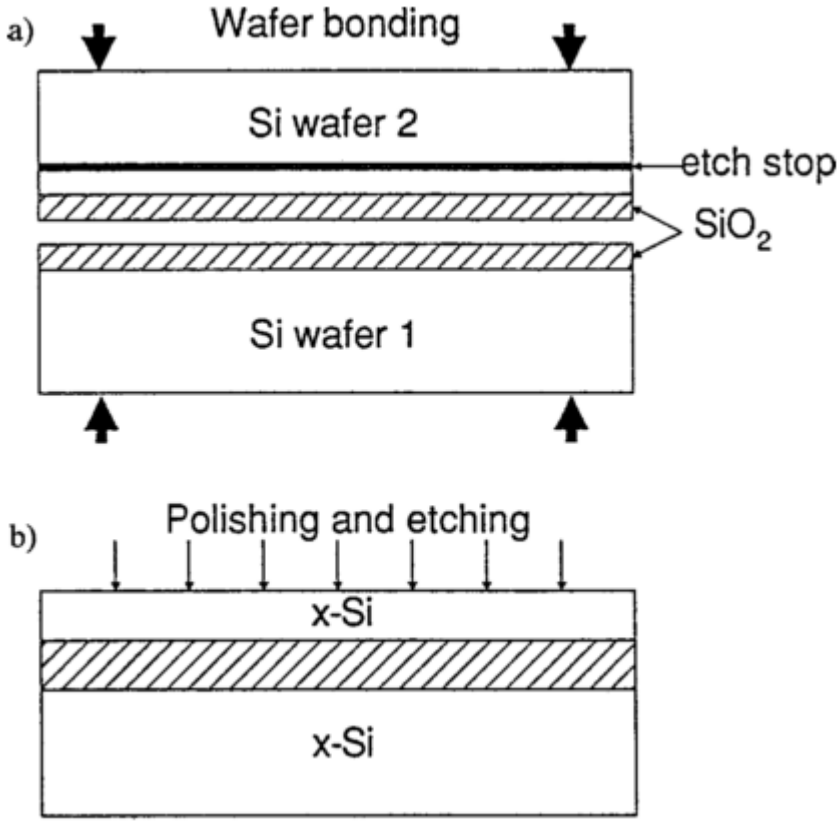

Figure 1.2: A schematic representation of bond and etch-back (BESOI) process [15]

Apart from the mentioned approaches, BESOI, Smart Cut™, and ELTRAN® methods involve the wafer bonding technique. For BESOI method, the thermally oxidised Si wafer 1 (also known as handle wafer) is bonded to Si wafer 2 which acts as bond wafer as shown in figure 1.2(a). After the wafer bonding process, the top wafer is etched to obtain the required thickness for SOI layer as shown in figure 1.2(b). Meanwhile, implantation of gas ions, most commonly hydrogen is made after the oxidisation process for Smart Cut™ method as shown in figure 1.3. The implantation process is meant for

layer splitting process to achieve required thickness of SOI layer after the wafer bonding process. The processes involved in ELTRAN® method is shown in figure 1.4. The ELTRAN® method uses similar procedures in Smart Cut™ with the difference in use of double layer porous Si layer instead of implantation of hydrogen ions. The advantage of using Smart Cut™ and ELTRAN® methods is that the initial wafer or seed wafer can be reused for the same process. Meanwhile, the SOA technology is achieved by gluing a fully-processed SOI substrate to another substrate such as glass and alumina [16]. Table 1.1 summarises the advantages and disadvantages of each SOI technology.

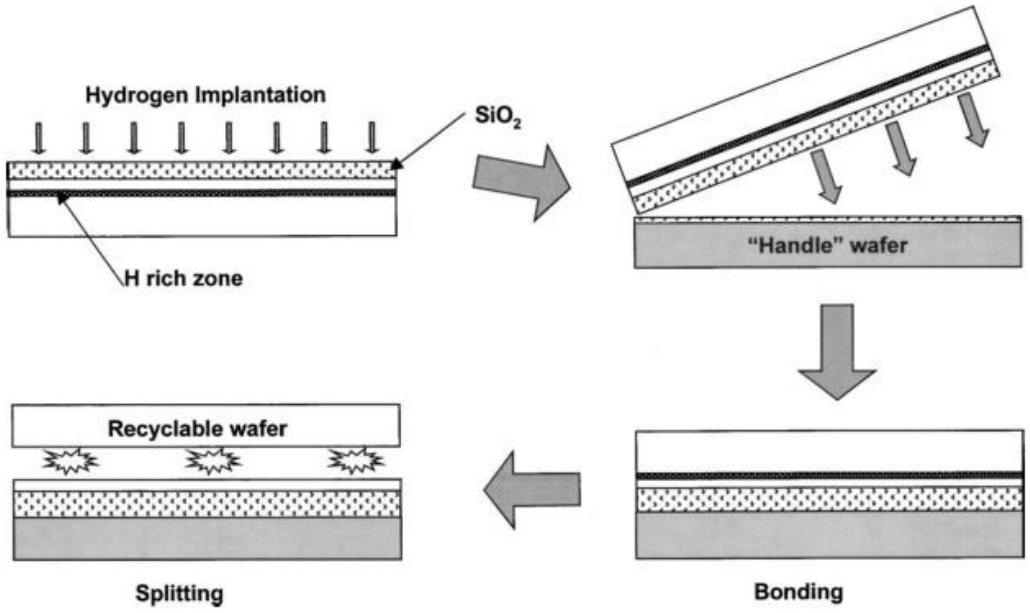

Figure 1.3: Smart Cut™ process for production of SOI wafers [15]

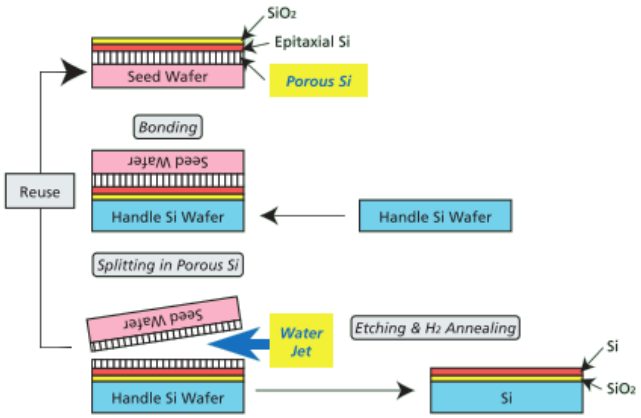

Figure 1.4: ELTRAN® process flow based on seed wafer re-usage [13]

However, the on-chip heat dissipation which causes thermal breakdown on SOI and SOA substrates have been proven to be a severe issue [17]. Therefore, there is a need

to look for the alternative to SOI and SOA wafers, which is the high resistivity bulk Si substrate. There are several methods to increase the bulk resistivity of Si substrate. These methods include proton implantation method and helium-3 ion irradiation technique, which reduce carrier lifetime by charge trappings. However, there are problems associated with both methods such as high product cost for proton implantation method, and insufficient high resistivity Si substrate produced using helium-3 ion irradiation technique. Meanwhile, in 2003, Mallik *et al.* [18] introduced a new idea in developing a semi-insulating silicon through a method called deep-level doping compensation using 3d transition elements. In this method, the high resistivity bulk Si substrate is achieved by reducing the background free carriers which result in degradation of circuit performance.

Table 1.1: Summary of advantages and disadvantages of each SOI technology.

Method	**Advantages**	**Disadvantages**
Silicon-on-sapphire (SOS)	Reduced self-heating effects and device parasitic capacitances [19]	Lower electron mobility, which diminishes its high frequency performance [20]
Separation by implanted oxygen (SIMOX)	Most mature SOI technology, reduced defect density, simpler process and cheap in terms of SOI materials [21]	Need of very large doses of oxygen and long term thermal treatment [22]
Bond and etch-back SOI (BESOI)	Silicon overlayer is not exposed to oxygen ion implantation at high dose, and wide flexibility is available in thickness of SiO_2 and silicon overlayer [23].	Two wafers to make one SOI wafer, which causes additional processing cost and some contamination due to etch-stop dopant [15]
Smart Cut™	Reduced cost of SOI wafer due to re-usage of seed wafer, and thickness of silicon film and/or buried oxide can be adjusted in a wide range [15]	Touch polishing required [15] and still expensive due to requirement of high dose of hydrogen implantation [24]
ELTRAN®	Reduced wafer material cost due to re-usage of seed wafer [13], more uniform SOI thickness and less surface roughness [25]	Requirement of expensive and complicated equipment such as water jet equipment [13]

1.2 Problem Statement

The idea introduced by Mallik *et al.* [18] on developing high resistivity bulk Si substrate through deep-level doping compensation is solely based on p-type CZ-Si. The reason is possibly that p-type substrate is mostly used in silicon based CMOS processing [26]. However, it has been shown in the work by Jordan *et al.* [27] that higher magnitude of Au-compensated high resistivity bulk Si substrate can be achieved by using n-type CZ-Si.

In addition, parasitic surface conduction (PSC) effect is more severe in n-type Si substrate as compared to p-type Si substrate. According to Reyes *et al.* [28], the resistivity at the surface of Si substrate decreases due to population of carriers during the formation of accumulation or inversion region. Higher attenuation is seen in the accumulation region for n-type Si substrate as compared to p-type Si substrate because electrons have higher mobility than holes. The potential and problem of using transition elements as the deep level dopants to produce high resistivity bulk n-type CZ-Si substrate have not been discussed by the work mentioned above.

1.3 Objectives of Research

The main objective of this research is to investigate the potential of using transition elements, i.e. gold (Au), silver (Ag), cobalt (Co), palladium (Pd), vanadium (V), manganese (Mn) and platinum (Pt) as deep level dopant for n-type CZ-Si substrate. This covers:

1. Perform numerical analysis on deep level doping compensation using MATLAB.
2. Evaluating the increase in bulk resistivity of n-type Si using deep level doping compensation.
3. Providing a comparative study on the resistivity and the effectiveness of the studied transition elements in enhancing the resistivity of Si.

1.4 Scope of Research

The scope of this project is to analyse the resistivity enhancement generated using deep level doping compensation through numerical calculation using MATLAB. The potential and effectiveness of each of the studied transition elements, i.e. Au, Ag, Co, Pd,

V, Mn and Pt as deep level dopants for n-type CZ-Si will be discussed in this work. The fabrication and experiment of high resistivity bulk n-type CZ-Si substrate will not be covered in this work. The experimental data used for comparison with the result of numerical calculation is obtained from [29] which was done at Southampton Nanofabrication Centre in 2015.

1.5 Thesis Outline

Chapter 2 discusses the techniques for the production of Si substrate. Thereafter, the methods used to produce high resistivity bulk CZ-Si substrate in some research work are also discussed, followed by the effect of impurity to the Si substrate and doping compensation. The basic principle of deep level doping compensation method is then explained in detail.

Chapter 3 presents the methodology used in this research. The equations and steps involved in the calculation of resistivity of n-type Si substrate compensated with studied transition elements are first explained. The deduction on most suitable transition elements as deep level dopants for n-type CZ-Si substrate is then made in later section.

Chapter 4 evaluates the resistivity enhancement of n-type CZ-Si substrate and compensation level provided by the studied transition elements. The most suitable transition elements for n-type Si are determined based on the resistivity plots calculated using MATLAB. The comparison between theoretical and experimental results are also discussed.

Last but not least, Chapter 5 summarises the work presented in the thesis.

CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

In previous chapter, it has been discussed that high resistivity Si substrate is important in MMIC application. Therefore, SOI and SOA technologies were introduced as a silicon-based solution for this purpose. However, thermal breakdown issue associated with both technologies calls for the need of developing high resistivity bulk Si substrate as an alternative solution.

In this chapter, the methods used to enhance the resistivity of bulk Si substrate, which include proton implantation method and helium-3 irradiation technique will be discussed. The effect of impurities in the substrate and another approach of producing high resistivity bulk Si substrate, which is known as compensation doping will also be studied.

2.2 Production of Silicon

The starting material for silicon is a pure form of sand (SiO_2) called quartzite. It is chemically processed to form a high-purity polycrystalline semiconductor from which single crystals are grown. There are generally two techniques for Si crystal growth: Czochralski (CZ) technique and float-zone (FZ) technique [30].

2.2.1 Czochralski Silicon

A simplified version of CZ puller, which is an apparatus used to produce monocrystalline Si ingots for CZ technique is shown in figure 2.1. The high purity polysilicon, known as electronic grade silicon (EGS) is melted in a rotating silica or quartz crucible. A seed crystal is placed in the melt and then slowly withdrawn from the melt. The molten silicon adhering to the crystal freezes or solidifies into a continuous crystal from the seed. The diameter of the crystal can be maintained by controlling the temperature of the crucible and the rotating speed of the crucible and the rod. However, the CZ process introduces contamination to the monocrystalline Si due to the presence of

oxygen, carbon monoxide and impurities such as boron and phosphorus. Hence, the resistivity of CZ-Si is low due to the presence of impurities in the substrate.

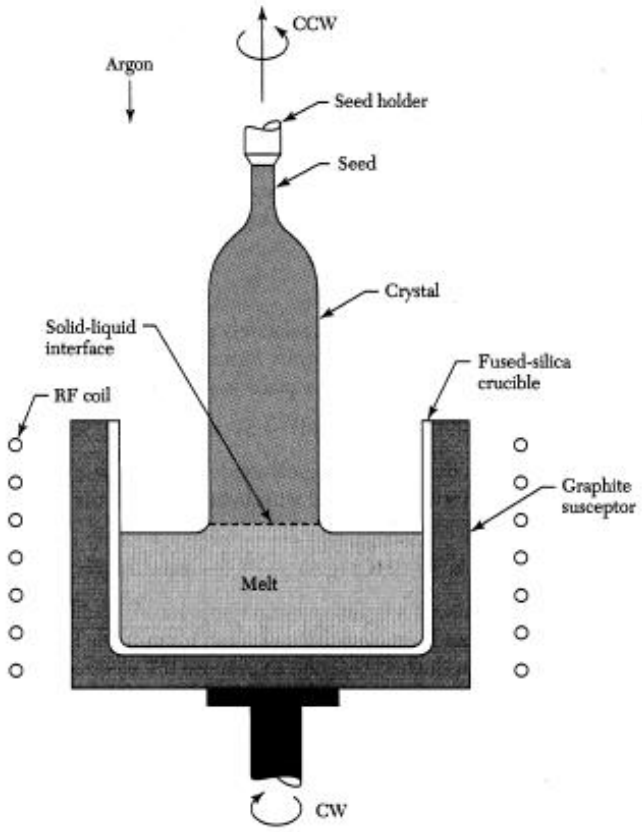

Figure 2.1: Czochralski crystal puller. CW represent clockwise rotation and CCW represents counter clockwise rotation [30]

2.2.2 Float-Zone Silicon

On the other hand, FZ process produces Si crystals with lower contamination as no crucible is used in the process. The schematic setup of FZ process is shown in figure 2.2. A high-purity polycrystalline rod is held vertically with a seed crystal at the bottom and rotated. A small molten zone (floating zone) is formed at the crystal by a radio-frequency heater. As the molten zone is moved upwards, a single-crystal Si solidifies at the retreating end of the zone and grows as an extension of the seed crystal. FZ process can be used to purify the crystal as the impurities tend to stay in molten zone rather than being incorporated into the solidified region. Thus, silicon with higher resistivity can be obtained through this process. FZ crystals are mainly used for high power and high voltages devices due to its high resistivity. There is a commercially available high resistivity FZ-Si technology called HiRes™ [31]. The bulk resistivity of Si produced through HiRes™ is up to 70 kΩ-cm, which is suitable for future GHz and THz application.

However, its maximum wafer diameter is limited to 8'', which increases the cost of production for modern CMOS processing as the standard wafer diameter is 12'' [32].

Therefore, there is a need to produce high resistivity bulk substrate using CZ-Si due to its advantage of larger wafer diameter (up to 18'') [33]. Thus, the production cost of CMOS processing can be reduced using CZ-Si wafer technology. The differences between CZ and FZ process for growth of Si crystal are summarised in table 2.1.

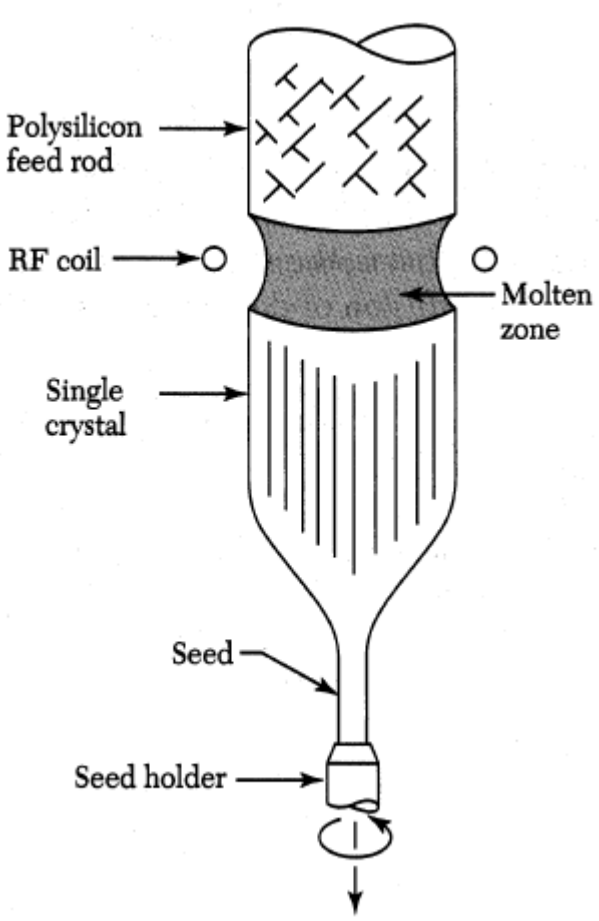

Figure 2.2: Schematic setup of float-zone process [30]

Table 2.1: Differences between Czochralski and float-zone process.

Characteristics	Czochralski Process	Float-zone Process
Crucible used	Yes	No
Purity	Poor	High
Seeding method	From top	From bottom
Resistivity	Not exceeding 100 Ω-cm	Up to 70 kΩ-cm by HiRes™
Wafer diameter	Up to 18''	Limited to 8''

2.3 Production of High Resistivity Bulk Silicon Substrate

One way to increase the resistivity of CZ-Si substrate is through ion implantation method. The bombardment of ions into Si bulk structure creates defects which can trap mobile carriers [34], [35]. Therefore, the carrier lifetime is low due to the presence of defects, which prevents the mobile carriers from conducting current freely in the substrate. The studies conducted to produce high resistivity bulk CZ-Si substrate using ion implantation method are summarised in table 2.2.

In 1989, Li [36] managed to produce a high resistivity layer beneath Si surface layer using proton implantation and two-step annealing process. The implantation of proton and annealing process formed the buried defect layer with a resistivity of up to 10^3 Ω-cm. Meanwhile, Liao *et al.* created semi-insulating regions within silicon substrate with a resistivity of 1 MΩ-cm [37]. It was achieved by bombarding proton beams at 30 MeV from a compact ion cyclotron to the surface of Si substrate. Following this work, the Si substrate with similar resistivity had been produced by Wu *et al.* using a lower proton implantation energy, which is 10 MeV [38]. In 2002, Rashid *et al.* reported a Si substrate with a resistivity of 0.1 MΩ-cm produced through their six-step implantation method using an implantation energy of 17.4 MeV [39].

The high-Q inductors and high transmission gain integrated antenna have been realised on the high resistivity Si substrate produced using proton implantation method by Liao *et al.* and Rashid *et al.* respectively [37], [39]. However, high process cost is needed for proton implantation method as an enormous dose of 10^{15} cm^{-2} is required to maintain the resistivity of the originally 15 Ω-cm Si substrate to be higher than 10^4 Ω-cm [34]. Therefore, there is a need to look for the alternative to proton implantation method.

Recently, high resistivity CZ-Si substrate produced by helium-3 irradiation technique has been reported. In 1987, helium-3 ion irradiation technique has been used for carrier lifetime control of silicon power devices [40]. Only until 2014, N. Li *et al.* reported to create a high resistivity region within CZ-Si substrate with a resistivity of over 1 kΩ-cm using a dose of 1.5-2.0 x10^{13} cm^{-2} of helium-3 ions [41]. The produced high resistivity Si substrate has been used by N. Li *et al.* for substrate noise isolation improvement in a CMOS process and quality factor improvement in on-chip spiral inductors [41], [42]. R. Wu *et al.* has also produced Si substrate with similar resistivity

using a dose of $3x10^{13}$ cm^{-2} of helium-3 ions in their work on radiation efficiency improvement in 60-GHz on-chip dipole antenna [35].

The helium-3 ion irradiation technique has the advantage of saving the product cost up to 97% as compared to proton implantation method by reducing the dose amount from $1.0x10^{15}$ cm^{-2} to $1.5x10^{13}$ cm^{-2} [41], [42]. However, the resistivity of CZ-Si substrate produced using this technique does not meet the minimum requirement of 3 kΩ-cm for low CPW loss and operation indistinguishable from GaAs substrates [6], [28]. Therefore, helium-3 ion irradiation technique is not suitable to produce high resistivity Si substrate for RF-MMIC application.

Table 2.2: Studies on high resistivity bulk CZ-Si substrate using ion implantation method.

Contributor	**Materials Used**	**Implantation Energy (MeV)**	**Dose (cm^{-2})**	**Starting Resistivity (Ω-cm)**	**Enhanced Resistivity (Ω-cm)**
Li [36]	Proton	0.18	$2.5x10^{16}$	8	10^3
Liao *et al.* [37]	Proton	30	10^{16}	1	10^6
Wu *et al.* [38]	Proton	10	10^{16}	10	10^6
Rashid e*t al.* [39]	Proton	17.4	10^{15}	10	10^5
N. Li *et al.* [41], [42]	Helium-3 ion	-	1.5-2.0 $x10^{13}$	6	1.0-1.5 $x10^3$
R. Wu *et al.* [35]	Helium-3 ion	-	$3x10^{13}$	6	10^3

2.4 Impurity and Compensation Doping

Pure or intrinsic Si has a relatively high electrical resistivity as compared to metal because Si is a semiconductor material which has a forbidden energy band gap, E_g of 1.1 eV. The energy band diagram of intrinsic Si is shown in figure 2.3, where E_C and E_V represent the bottom edge of conduction band and top edge of valence band respectively. It is shown that the intrinsic Fermi level, E_i is at the middle of Si bandgap.

However, impurities are easily introduced to monocrystalline Si due to the contamination from the crucible in CZ process. It is also a common approach to modulate the electrical properties of Si substrate by a process called doping. A large number of free carriers can be introduced to the Si substrate by introducing suitable impurities or dopants. Therefore, it is almost impossible to have pure Si substrate in reality.

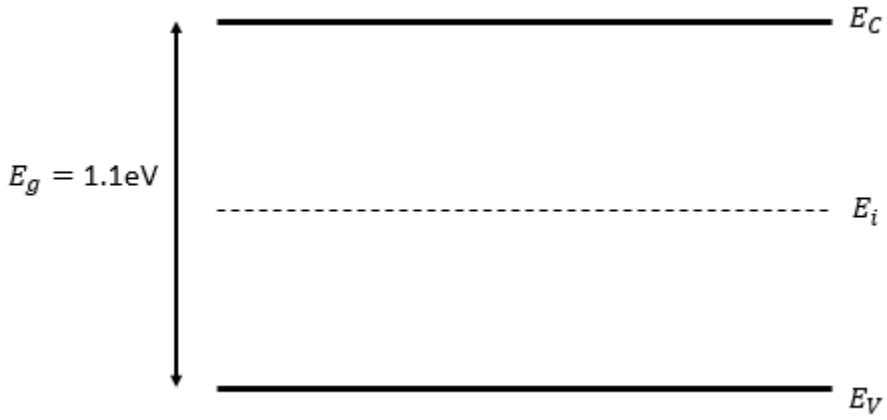

Figure 2.3: Energy band representation of intrinsic Si.

There are two types of impurities, namely shallow impurities and deep impurities. Shallow impurities introduce impurity levels within the energy bandgap of a material which is close to the band edge, either at the bottom of conduction band or at the top of valence band [43]. On the other hand, deep impurities have the impurity levels far away from the band edge.

The doping process in Si is always associated with shallow impurities from group III and V elements. Group III impurities such as boron are called as acceptors because each boron atom can accept an extra electron from Si atom, thus creating a hole. The Si substrate doped with acceptors are called p-type as holes carry positive charge. On the other hand, group V impurities such as phosphorus are known as donors because they donate electrons. The substrate doped with donors are known as n-type as electrons carry negative charge.

Figure 2.4 illustrates the energy band diagrams of Si with shallow donor and acceptor impurities. Donor level, E_D and acceptor level, E_A are introduced near the edge of conduction band and valence band respectively within the Si bandgap. With sufficient ionisation energy, electrons from E_D can be promoted to conduction band whereas holes from E_A can fall into valence band. The ionised electrons and holes subsequently become free carriers to conduct current within the bands.

There is an approach to develop high resistivity bulk Si substrate through a method called compensation doping. Compensation doping occurs when Si substrate is co-doped with shallow donors and acceptors. The electrons from donors at E_D level fall into E_A level to recombine with the holes from acceptors without generation of free

carriers. Thus, the concentration of background free carriers is reduced, which increases the resistivity of the substrate. The concentrations of donors and acceptors determine the type of Si substrate (n-type or p-type). The substrate becomes n-type when the donor concentration, N_D is greater than the acceptor concentration, N_A (as shown in figure 2.5) and vice versa. However, the free carriers are completely absent from the Si substrate when there is an equal number of N_D and N_A.

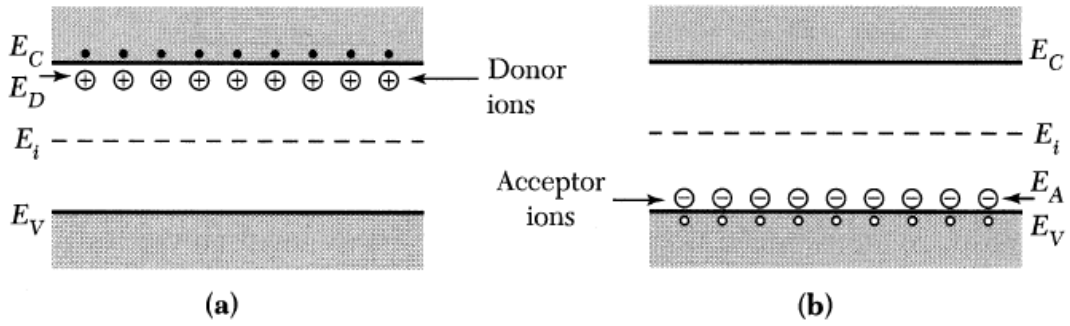

Figure 2.4: Energy band of Si with shallow (a) donor and (b) acceptor impurities [44]

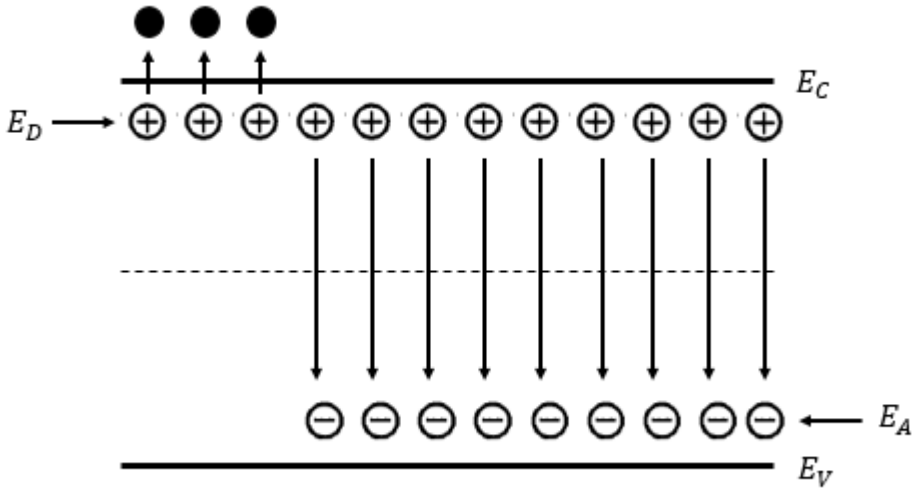

Figure 2.5: Compensation doping process in Si for $N_D > N_A$.

2.5 Deep-Level Doping Compensation Method

The idea of creating high resistivity bulk CZ-Si substrate using deep-level doping compensation has been proposed by Mallik *et al.* in 2003 [18]. The basic principle of this method is compensating shallow impurities with deep impurities, i.e. shallow donors are

being compensated by deep acceptors (as shown in figure 2.6) whereas shallow acceptors are being compensated by deep donors (as shown in figure 2.7).

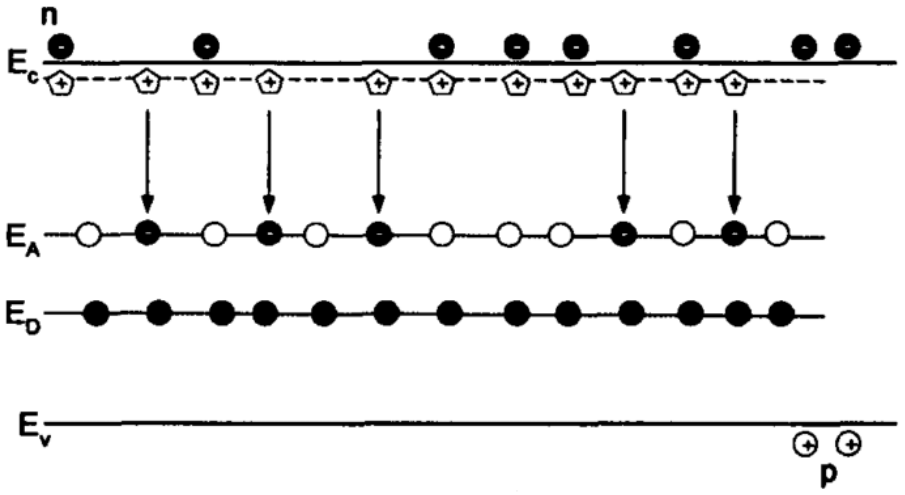

Figure 2.6: Compensation between shallow donors and deep acceptors [45]

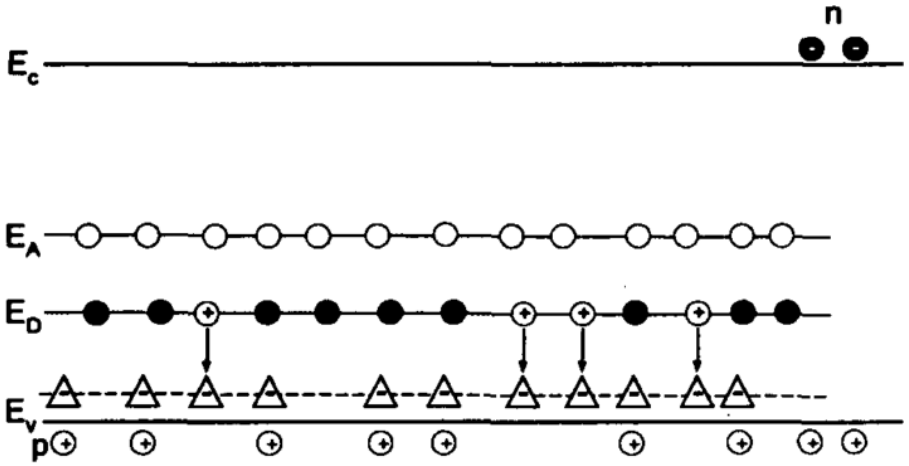

Figure 2.7: Compensation between shallow acceptors and deep donors [45]

As illustrated in figure 2.6, deep acceptors introduced an energy level at E_A, which is close to the intrinsic Fermi level. The deep acceptors which are negatively charged attract the minority carrier holes to be trapped at E_A level. The electrons from shallow donors are initially excited to the conduction band, then fall to E_A level to recombine with the holes. On the other hand, the positively charged deep donors introduced an energy level at E_D as shown in figure 2.7. The minority carrier electrons are attracted and trapped at E_D level while the holes from shallow acceptors fall into valence band. The trapped electrons at E_D level then fall into valence band to recombine with the holes. Therefore,

there is no generation of free carriers which reduces the resistivity of the substrate in both cases.

Figure 2.8 shows the resistivity of Si at 300 K with a background boron concentration of 10^{14} cm^{-3}, compensated using deep donor impurities with generic energy level positions below conduction band edge, E_D. It can be observed that the resistivity of Si increases until a maximum value is reached while the concentration of deep donors, N_D increases. The resistivity is low initially due to under-compensation caused by insufficient number of deep donors. The maximum value of the resistivity of Si is reached when deep donors exactly compensate for the boron acceptors. Further increase in N_D causes overcompensation which results in a fall in the resistivity of Si, making the substrate tends to become n-type.

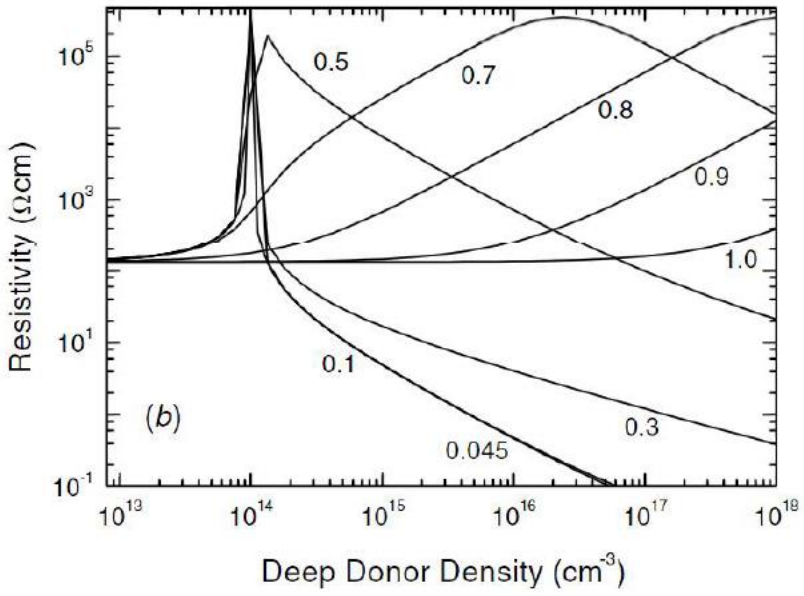

Figure 2.8: Calculated resistivity of Si at 300 K as a function of generic donor concentration for background boron concentration of 10^{14} cm^{-3} [18]

It can be noted that the resistivity peaks are sharper for E_D lower than 0.3 eV. Meanwhile, the resistivity remains high over a relatively wide range of concentration for larger values of E_D. For small values of E_D, almost all donors are ionised and take part in the compensation as the donor energy level is nearer to the conduction band than Fermi level. A slight increase in N_D causes the resistivity to decrease sharply, changing the material to n-type. On the other hand, for large values of E_D, the donor level is near intrinsic Fermi level and less fraction of deep donors is ionised. Therefore, the

compensation change gradually with the increase in N_D and the resistivity remain high over a wide range of N_D.

2.6 Transition Elements as Deep Level Dopants

The transition elements are used as deep level dopants as they introduce a pair of deep donor and deep acceptor levels into the Si band gap as shown in table 2.3. The deep dopant energy levels introduced by the transition elements pin the Fermi level near the middle of the Si band gap as shown in figure 2.9 [27]. Thus, high resistivity CZ-Si substrate can be achieved by capturing the free carriers by deep impurities, which reduces the concentration of background free carrier.

Table 2.3: Positions of energy levels of transition elements in Si [46]

Element	Donor level below E_C (eV)	Acceptor level above E_V (eV)
Co	0.89	0.82
Pd	0.84	0.9
Au	0.78	0.56
Ag	0.75	0.545
V	0.45	0.92
Mn	0.42	1.0
Pt	0.314	0.889

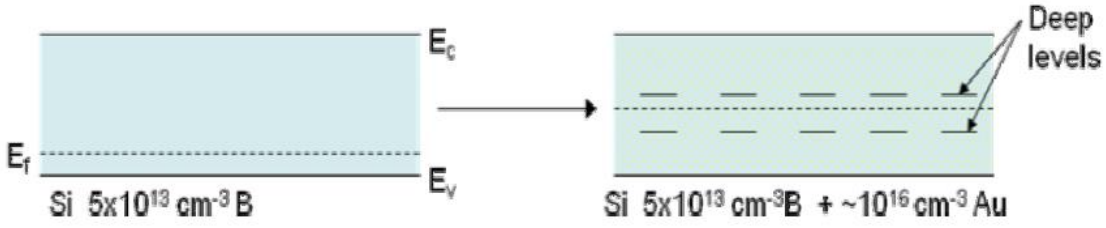

Figure 2.9: Fermi level pin by deep levels introduced by transition elements [27]

The transition element dopants are generally grouped into two categories: Au, Ag, Co and Pd are in first category whereas Pt, V and Mn are in second category. As illustrated in figure 2.10, the resistivity of p-type CZ-Si substrate increases with increasing concentration of the deep dopants in first category. The behaviour of impurities in first category is due to the presence of both deep donor and acceptor levels very near intrinsic

Fermi level of Si bandgap. For Au and Ag, the resistivity of Si reaches a plateau at the concentration of deep dopants over 10^{16} cm^{-3} for three different background boron concentration. The reason for the slight difference in the behaviour of Au and Ag is that both their donor and acceptor levels are nearer to the middle in the Si bandgap as compared to Co and Pd.

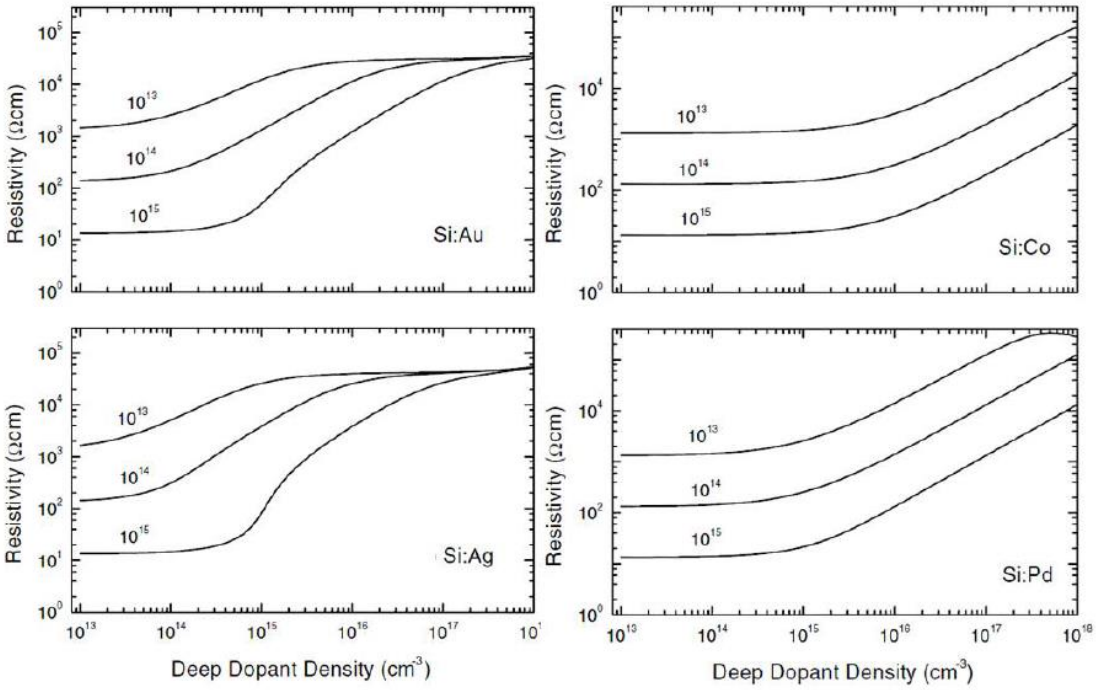

Figure 2.10: Calculated resistivity of Si at 300 K as a function of Au, Ag, Co and Pd for three different background boron concentration in cm^{-3} [18]

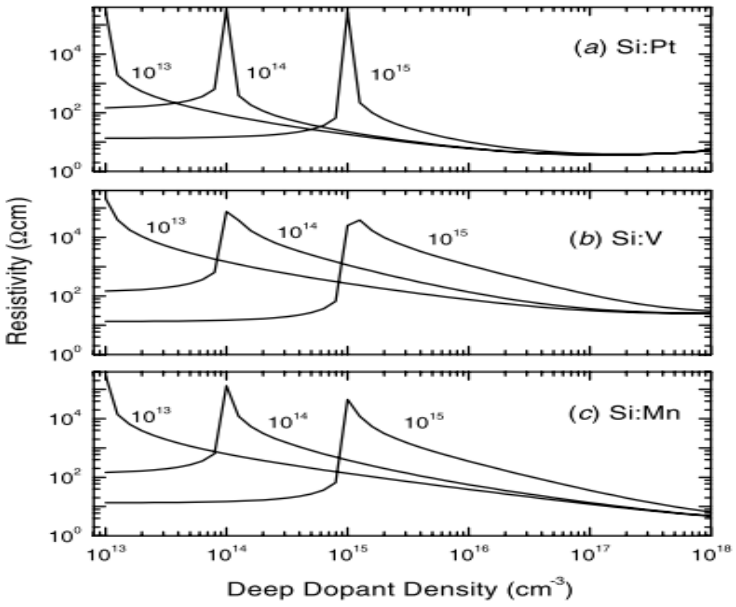

Figure 2.11: Calculated resistivity of Si at 300 K as a function of (a) Pt (b) V and (c) Mn concentrations for three different background boron concentrations in cm^{-3} [18]

For the second category of deep dopants, the resistivity of p-type CZ-Si reaches a peak and then reduce sharply with the increase in the concentration of the deep dopants as shown in figure 2.11. The reason of the difference in the behaviour is that the impurities in second category only have their donor levels near the intrinsic Fermi level. Therefore, the dopants in second category can only compensate for p-type doped silicon substrate.

The effect of using 3d transition elements as deep level dopants in n-type CZ-Si substrate has not been shown in the work by Mallik *et al.* Therefore, the analysis method based on the position of energy levels of studied transition elements was extended to n-type CZ-Si substrate which will be discussed in the next chapter.

2.7 Summary

The realisation of high resistivity bulk Si substrate using ion implantation method was studied. These include proton implantation method and helium-3 ion irradiation technique. Both methods use the charge trappings to enhance the resistivity of CZ-Si substrate. However, there are problems associated with each method such as high product cost for proton implantation method and insufficient enhancement of resistivity of Si substrate provided by helium-3 ion irradiation technique for RF-MMIC application. There is another approach to produce high resistivity bulk Si substrate which is achieved by compensation doping. The compensation between donor and acceptor impurities reduces the concentration of background free carriers which causes degradation of resistivity of Si substrate. The deep level doping compensation method involves the compensation between deep and shallow impurities.

CHAPTER 3
RESEARCH METHODOLOGY

3.1 Introduction

In previous chapter, it has been shown that compensation doping method can be used to increase the resistivity of CZ-Si substrate. Deep level doping compensation method is studied in this work to develop high resistivity CZ-Si substrate. The analysis of previous work is only based on p-type CZ-Si substrate. Therefore, the potential of using transition elements as deep level dopant for n-type CZ-Si substrate will be investigated in this research.

3.2 Project Implementation Flow

Figure 3.1 summarises the project implementation flow of this research.

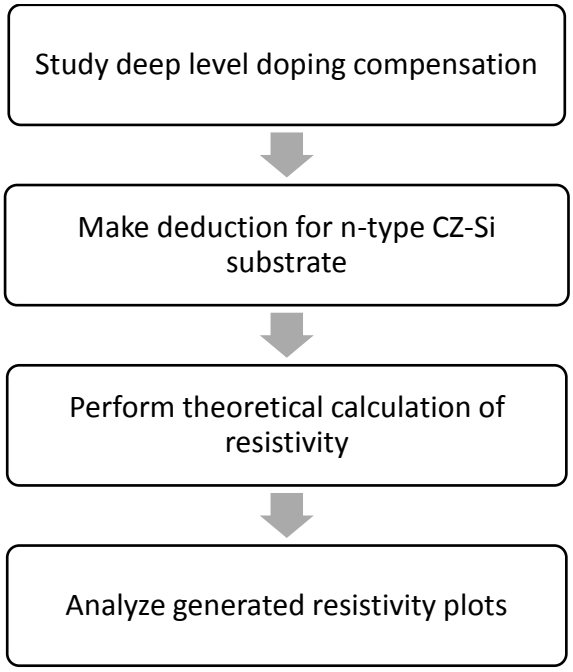

Figure 3.1: Project implementation flow

The study on the deep level doping compensation for p-type CZ-Si substrate was conducted based on the work by Mallik *et al.* [18]. The major factors which affect the resistivity plots are identified. The two identified factors as discussed in Section 2.5 are

positions of energy levels of deep dopant impurities in Si bandgap and deep dopant concentration. The analysis method used in the study was extended to n-type CZ-Si substrate.

The deduction on the suitability of the studied transition elements for n-type CZ-Si substrate was made based on the position of energy levels of these elements. It has been discussed in Section 2.6 that the deep dopant with its donor and acceptor levels near to the middle of Si bandgap provides better resistivity enhancement for p-type CZ-Si substrate. The most suitable transition elements as deep level dopants for n-type CZ-Si can be deduced with similar approach.

Then, the theoretical calculation of resistivity of n-type CZ-Si substrate compensated by studied transition elements was made using MATLAB software. The calculation methods used was based on the work by Mallik *et al.* [18]. The assumptions were determined for solving the errors occurred during the calculation. The justification for the assumptions was made by generating a similar graph in the work by Mallik *et al.* [18] using the theoretical calculation method in this research. The validity of the assumptions was determined by checking whether the result of theoretical calculation is in agreement with the work by Mallik *et al.* [18].

The resistivity plots obtained from the calculation were displayed in graphic form. The analysis on the resistivity plots of each studied transition element was made to verify the deduction made on the previous step. The resistivity enhancement provided by each transition elements was investigated to determine their suitability as deep level dopants for n-type CZ-Si substrate. The background phosphorus concentration was varied to verify whether varying the n-type background changes the nature of compensation provided by the studied transition elements to CZ-Si substrate. The comparison was made between the theoretical calculation and measurement on actual Au-compensated CZ-Si wafer.

3.3 Theoretical Resistivity of CZ-Si Substrate

The calculation and generation of resistivity plot of n-type CZ-Si were made using MATLAB software. Although other environments (e.g. Excel/VBA) or languages (e.g. Fortran 90, C++) are available, MATLAB offers a nice combination of handy programming features with powerful built-in numerical capabilities [47]. The steps of

calculation of resistivity of CZ-Si substrate for a range of deep dopant concentrations from 10^{13} cm^{-3} to 10^{18} cm^{-3} were summarised in figure 3.2. The upper limit is chosen to be 10^{18} cm^{-3} as the concentrations of studied transition elements in Si are limited by factors such as equilibrium solubility, diffusivity and segregation coefficient in the solid [18]. Hence, the practical attainable concentrations of transition elements are likely to be lower than 10^{18} cm^{-3}.

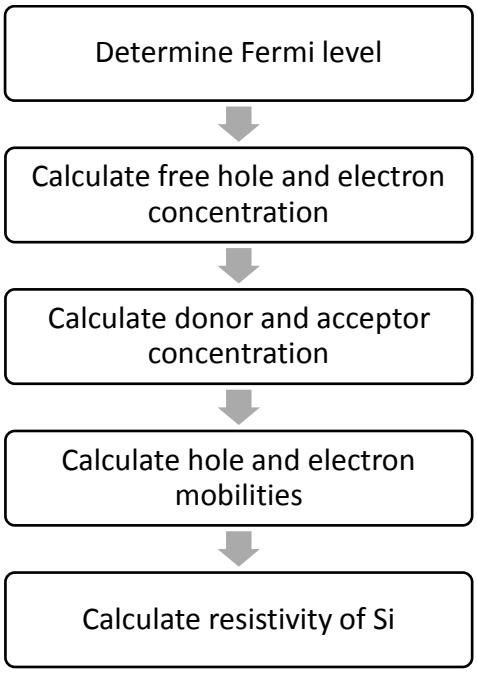

Figure 3.2: Process flow required for calculation of resistivity of Si.

The Fermi level E_F was determined by solving the charge neutrality equation given by [48]:

$$p + \sum_i N_{D_i}^+ - n - \sum_j N_{A_j}^- = 0 \tag{3.1}$$

In equation (3.1), p and n are the free hole and electron concentrations given by:

$$n = N_C \, e^{-(E_C - E_F)/kT} \tag{3.2}$$

$$p = N_V \, e^{-(E_F - E_V)/kT} \tag{3.3}$$

where k is the Boltzmann constant, and T is taken as 300 K. N_C and N_V are the temperature-dependent effective densities of states of the conduction (E_C) and valence (E_V) bands respectively. The values of N_C and N_V are taken as 2.8 x 10^{19} cm^{-3} and 1.04 x 10^{19} cm^{-3} respectively at 300 K [48].

The $N_{D_i}^+$ and $N_{A_j}^-$ are the *i*th and *j*th ionised donor and acceptor concentration for a total impurity density of N_{D_i} and N_{A_j} respectively. For shallow impurities, such as boron and phosphorus which only contributes single donor or acceptor level, the expression for $N_{D_i}^+$ and $N_{A_j}^-$ are given by [49]:

$$N_{D_i}^+ = N_{D_i}(1 + g_i\, e^{\frac{E_F - E_{D_i}}{kT}})^{-1} \quad (3.4)$$

$$N_{A_j}^- = N_{A_j}(1 + g_j\, e^{\frac{E_{A_j} - E_F}{kT}})^{-1} \quad (3.5)$$

where E_{D_i} (E_{A_j}) is the energy position of the *i*th (*j*th) impurity level, measured from the valence band for a donor (acceptor), g_i and g_j are the corresponding degeneracy of donor and acceptor impurity. It is assumed that deep level dopants only create a pair of donor (E_D) and acceptor (E_A) levels in Si bandgap. Therefore, the ionised concentration of deep donors and acceptors are given by [50]:

$$N_D^+ = N_D(1 + g_D\, e^{\frac{E_F - E_D}{kT}} + e^{\frac{2E_F - E_A - E_D}{kT}})^{-1} \quad (3.6)$$

$$N_A^- = N_A(1 + g_A\, e^{\frac{E_A - E_F}{kT}} + e^{\frac{E_A + E_D - 2E_F}{kT}})^{-1} \quad (3.7)$$

For n-type CZ-Si substrate, the total ionised donor concentration is the sum of ionised donor concentrations of phosphorus (equation 3.4) and deep dopants (equation 3.6). The energy position of phosphorus donor was taken as E_C – 0.045 eV, and degeneracy (g) for donor and acceptor are 2 and 4 respectively. The degeneracy of donor impurity level (g_i or g_D) equals 2 as each donor state can be unoccupied or occupied with an electron of either spin (spin-up or spin-down) [51], [52]. The degeneracy of acceptor impurity level (g_j or g_A) is 4 instead of 2 as both light and heavy sub-bands exist at the valence band edge. The charge neutrality equation was solved numerically to obtain the Fermi level E_F.

Then, the values of free hole (p) and electron (n) concentrations were calculated by substituting the values of E_F obtained from numerical solution. The total ionised deep donor (N_D^+) and acceptor (N_A^-) concentrations were calculated for deep dopant density ranged from 10^{13} cm^{-3} to 10^{18} cm^{-3}.

The hole (μ_p) and electron (μ_n) mobilities are required in the calculation of the resistivity of Si. The mobilities of the holes and electrons are limited by lattice scattering

and the active impurities scattering mechanisms. The expression for mobilities limited by both mechanisms are given by [53], [54]:

$$\mu_{lattice} = \mu_0 \left(\frac{T}{T_0}\right)^{-\alpha} \tag{3.8}$$

$$\mu_{impurities} = \frac{AT^{\frac{3}{2}}}{N_{scat}}\left[\ln\left(1+\frac{BT^2}{N_{car}}\right) - \frac{BT^2}{N_{car}+BT^2}\right]^{-1} \tag{3.9}$$

where N_{scat} represents the number of scattering sites introduced by impurities and N_{car} represents the number of free carriers available for screening. The parameters used in equations (3.8) and (3.9) for hole and electron mobilities are shown in table 3.1.

Table 3.1: Parameters used in equation (3.8) and (3.9) for hole and electron mobilities [53], [54]

Parameter	Hole	Electron
μ_0	473 $cm^2/V\ s$	1448 $cm^2/V\ s$
T_0	300 K	300 K
A	1.0 x $10^{17}/cm/V/s/K^{3/2}$	4.61 x $10^{17}/cm/V/s/K^{3/2}$
B	6.25 x $10^{14}/cm^3/K^2$	1.52 x $10^{15}/cm^3/K^2$
N_{scat}	$\sum_i N_{D_i}^+ + \sum_j N_{A_j}^-$	$\sum_i N_{D_i}^+ + \sum_j N_{A_j}^-$
N_{car}	$\sum_j N_{A_j}^- - \sum_i N_{D_i}^+$	$\sum_i N_{D_i}^+ - \sum_j N_{A_j}^-$

However, an assumption was made that the mobility due to impurity scattering, $\mu_{impurities}$ is removed from the calculation when N_{car} has a zero or negative value, i.e. the mobility of carriers is solely limited by lattice scattering, $\mu_{lattice}$. The reason is that error occurs in equation 3.9 when the natural logarithmic expression is undefined, which is caused by zero or negative value of N_{car}. The error is unavoidable as N_{car} used in the calculation for hole mobility is opposite of that for electron mobility as shown in table 3.1. Therefore, the assumption was made to solve the mentioned problem. Both hole and electron mobilities due to both mechanisms were combined using Matthiessen's rule given by [55]:

$$\frac{1}{\mu} = \frac{1}{\mu_{lattice}} + \frac{1}{\mu_{impurities}} \tag{3.10}$$

The obtained values for free hole and electrons concentrations (p and n) and mobilities (μ_p and μ_n) were used for the calculation of resistivity of n-type Si which is given by:

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)} \tag{3.11}$$

where q is the electronic charge given by 1.6 x 10^{-19} C.

To justify the assumption made previously on the calculation of hole and electron mobilities, the resistivity plot of CZ-Si substrate with background boron concentration of 10^{14} cm^{-3} compensated using generic deep donor impurities was generated based on the theoretical calculation method in this section. The background boron concentration is chosen to be 10^{14} cm^{-3} as it is difficult to produce CZ-Si wafers with p-type background lower than 10^{13} cm^{-3} due to contamination from the growth crucible [18]. The generated resistivity plot for p-type CZ-Si substrate is shown in figure 3.3. The result obtained from the theoretical calculation method in this research is consistent with the work by Mallik *et al*. [18] (see figure 2.8 in section 2.5). Therefore, the assumption made is valid.

The result is extended to n-type CZ-Si substrate by generating the resistivity plot of Si with background phosphorus concentration of 10^{14} cm^{-3} compensated with generic deep acceptor density impurities was generated. The background phosphorus concentration is chosen to be 10^{14} cm^{-3} as it is difficult to produce CZ-Si wafers with n-type background lower than 10^{13} cm^{-3} due to contamination from the growth crucible. The generated resistivity plot for n-type CZ-Si is shown in figure 3.4. The trend of the obtained result is similar to that of p-type CZ-Si substrate compensated with deep generic donor impurities (see figure 3.3) where the sharp resistivity peaks are observed for deep acceptor level, E_A lower than 0.3 eV. The resistivity remains high over a relative wide range of concentration for larger values of E_A. The optimum range of values of E_A for relatively stable resistivity enhancement is between 0.5 eV and 0.7 eV, which is near intrinsic Fermi level. Hence, the transition elements are suitable candidates as deep level dopants for n-type CZ-Si substrate as they introduce a pair of deep donor and acceptor levels into Si bandgap.