PHASE LOCKED LOOP FOR BLUETOOTH RADIO

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PHASE LOCKED LOOP FOR BLUETOOTH RADIO

by

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I would like to take this opportunity to extend my heartfelt gratitude and acknowledgement to the contribution of all those that have helped me out during my research work in order to make this project a success.

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LIST OF ABBREVIATION

CP Charge Pump

DPLL Digital Phase Locked Loop

FM Frequency Modulation

LPF Low Pass Filter

LPLL Linear Phase Locked Loop

PFD Phase Frequency Detector

PLL Phase Locked Loop

SPLL Software Phase Locked Loop

VCO Voltage Controlled Oscillator

“PHASE LOCED LOOP” UNTUK RADIO BLUETOOTH

ABSTRAK

“Phase locked loop” merupakan satu sistem litar tertutup yang diguna pakai dalam banyak aplikasi untuk pelbagai fungsi. Manakala “Bluetooth” merupakan salah satu protokol piawaian untuk rangkaian tanpa wayar jarak dekat. Dengan menggunakan “Bluetooth” transmisi data boleh dibuat dengan objek statik atau bergerak. Sebuah “Phase Locked Loop Bluetooth” Radio telah dinyatakan dalam kajian ini. Rekaan sistem tertutup yang dicadangkan adalah stabil. “Phase Locked Loop”(PLL) yang direka merangkumi sebuah pengesan fasa dan frequensi (PDF), pam cas (CP), “Current- Starved” Voltan Pengayun Terkawal dan kaunter bahagi dengan 2. PLL disimulasikan dan lingkungan kunci ialah 28.57 MHz hingga 66.67 MHz. Frekuensi bebas untuk Voltan Pengayun Terkawal ialah 589.74 MHz. Masa mengunci ialah masa diambil oleh PLL mencapai hasil yang stabil. Masa mengunci untuk projek ini ialah 110 ns. PLL dari projek ini boleh menghasilkan isyarat dalam frekuensi 2.41 GHz dengan “duty cycle” berjumlah 51% apabila isyarat denyut berfrekuensi 50 MHz dibagi sebagai input.

PHASE LOCKED LOOP FOR BLUETOOTH RADIO

ABSTRACT

Phase locked loop is a closed loop system and is being used in many applications for various purposes. While Bluetooth is one of the four protocol standard for short range wireless networks. With Bluetooth data transmission can be done either in fixed or mobile devices. A Phase Locked Loop Bluetooth Radio is specified in this study. The close loop in the design proposed is stable. This Phase Locked Loop (PLL) was designed with Phase Frequency Detector (PFD), Charge Pump (CP), Current-Starved Voltage-Controlled Oscillator, and Divide-By 2 counter. The Phase Locked Loop is simulated and the lock in range is from 28.57 MHz to 66.67 MHz. The free running frequency of Voltage Controlled Oscillator is 589.74 MHz. The lock in time is 110ns which is the time taken for the Phase Locked Loop to achieve a stable output of 2.41 GHz. This Phase Locked Loop can produce a 2.41 GHz frequency signal with 51% duty cycle when a 50 MHz pulse signal is given as input.

CHAPTER 1

INTRODUCTION

1.1 Overview

One of the fastest growing technologies which make it possible for people to have access to network and service is wireless communication. There are advantages as well as some disadvantages in this wireless approach. Mobility is considered as the biggest advantage of wireless compared to the casual cabled devices which hinders the free movement due to the requirement of plugging. In addition, a new user can connect or disconnect the network, change to different networks, and create ad hoc networks according to their needs. Moreover, it is easier to deploy a wireless networks and they are cheaper than wired networks. On the other hand, the disadvantages of wireless networks are data security, lower reliability because of the interferences, higher power consumption, threats because of inherent broadcast properties of the radio medium, worries about user safety due to continued exposition to radio frequency, and lower data rates. Bluetooth (over IEEE 802.15.1) is one of the four protocol standards for short range wireless networks. Bluetooth works in the open Industrial, Scientific, Medical (ISM) band from 2.40 GHz to 2.48 GHz [1]. A Phase Locked Loop for Bluetooth Radio is proposed in this work.

Phase locked loop (PLL) is a negative feedback circuit which includes a phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO) and a frequency divider [2] as shown in the Figure 1.1. Phase locked loop is used in many applications for variety of uses. It is used in space communication for demodulation extension, bit synchronization, symbol synchronization, demodulation of

frequency modulated signals, clock recovery, and frequency synthesis for instrumentations [3] [4].

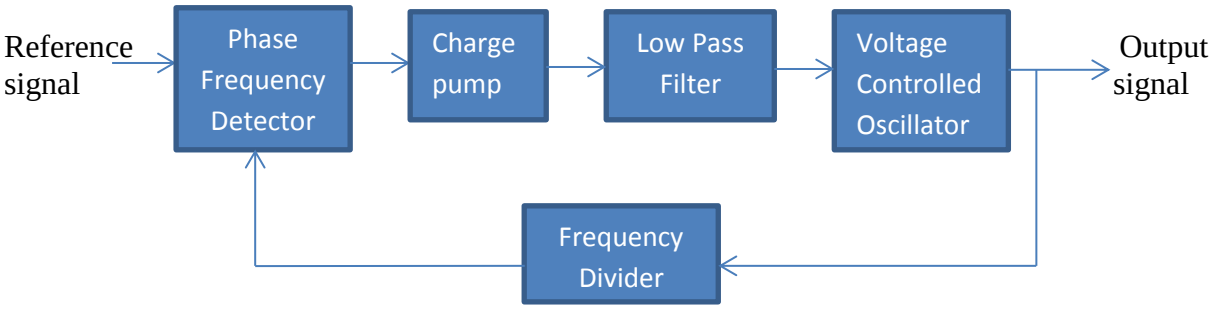


Figure 1.1 : PLL circuit structure

This feedback system makes the output signal to track the reference signal's frequency and phase. It is said to be in locked condition when both the frequency and phase are synchronized. One input of the PFD is connected to input signal while the other input is with output of frequency divider or commonly known as divide by N counter [5].The output of PFD is an "error" voltage proportional to the difference of phase and frequency between both signals. A charge pump is used because of PFD. The output of PFD is fed into input of CP and based on the input CP "pumps" current into or out of the circuit [6]. Then the LPF will filter out the high frequency components [3] and determines the control voltage, V_{CTRL} for the VCO. Based on the $V_{CTRL,}$ VCO will produce the output signal which will undergo frequency division before being compared with the input signal in PFD.

1.2 Problem Statement

Nowadays, it is common to see the usage of phase locked loop in numerous applications with specific modification in the design. Although there are several types of PLL a linear PLL is being used in this work. It is found that this type of PLL have drawbacks which are longer switching or lock in time. Other than that, the circuit complexity is high and it needs to be redesigned for every new design because its process parameters are sensitive [7].

Phase locked loop developed by Joy et.al [3] used JK phase detector (PD), loop filter (LF), digital controlled oscillator (DCO) and a divide by N counter. The limitation in this work is caused by the use of K counter loop filter which only works with XOR and JK flip flop.

Next, the phase locked loop design implemented by Marlette et.al [8] is also for Bluetooth application. In this design, $\Delta\sum$ modulator and a programmable divider is being used. The limitation with this design is the circuit become more complex as the PLL's non-linear characteristics make the noise folding down near the carrier and this required a very linear circuit design and appropriate filtering.

Lastly, the Fully Programmable Multi-Modulus Divider used by Theil et.al [9] has a limitation which is the maximum operating speed is constrained by the parasitic capacitance which is caused by feedback from the first stage. Apart from that, the overall circuit design became very complicated by using this method.

1.3 Research Objective

1) To design a Phase Frequency Detector, Charge Pump, Low Pass Filter, Voltage Oscillator and divide-by 2 counter circuit in LTSpice.

2) To integrate a functioning PLL circuit designed specifically for Bluetooth Radio at 2.40 GHz.

3) To validate the PLL functionality using LTSpice.

1.4 Scope of Project

This project will cover the following scope:

1. This project focuses on phase locked loop for Bluetooth radio. There are many different ways to implement this and to improve the performance. This project will focus on design of phase locked loop which is simple and can yield an accurate result for the Bluetooth radio application.

2. This study will also include the steps to build and design a phase locked loop Bluetooth radio using LTSpice. Tests will be conducted to make sure the output serves the requirement for Bluetooth radio.

1.5 Outline of Thesis

There are 5 chapters in this research.

Chapter 1 introduces the phase locked loop blocks, the function of each block and the applications in which it is being used in various fields with a short overview of the previous researches and their limitation and also briefly explains the scope of the research.

Chapter 2 describe the background of phase locked loop and its applications in various field including in Bluetooth applications. This chapter also covers about the limitation in previous researches in this research area.

Chapter 3 explain the design of phase locked loop that is going to be used for Bluetooth radio application. In addition, the procedures of the research will be explained in detail. This chapter will also compare the design used from the previous study with the current one.

Chapter 4 discuss on the results acquire from the assigned phase locked loop. The acquired date from the result will be followed by explanation and discussion.

Chapter 5 concludes the finding of this study and future works that can be done.

CHAPTER 2

LITERATURE REVIEW

2.1 Background

Phase locked loop is commonly abbreviated as PLL. Although it sounds like a discovery of recent times, it has history since 1932. Due to the cost factor which was expensive at that time, the technology was not improved as it is now. After the field of integrated circuit undergone advancement, PLL has turned out to be an important building block in the electronics technology. PLL has found its purpose in the area of technical such as frequency synthesizing, FM demodulation, data recovery, frequency control and signal synchronization [10]. The PLL is closed loop system which synchronizes the output signal with the reference signal in phase and frequency. The phase error between output signal and reference signal in synchronised or 'locked' state is zero or remains constant. If the phase error increases, a control mechanism will function in a way to reduce the phase error. By this way, the phase of the output signal is really locked to the phase of reference signal. This is the reason why this system is called phase locked loop. There are many classes of PLL available each with different design and for different purposes. They are:

1) Analog or Linear PLL (LPLL)

2) Digital PLL (DPLL)

3) All Digital PLL (ADPLL)

4) Software PLL (SPLL)

In this study we are going to focus on the Linear PLL. The major PLL blocks used in this study are Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Voltage-Controlled Oscillator (VCO) and Divide-by-N blocks. The input to the PLL is called reference signal and the value of input signal is depends on the user [11].There are many researches have been done on each block and different techniques have been used to create PLL for various applications.

As mentioned earlier a PFD has two inputs which are connected to input signal which works as the reference signal and output of divide by N counter. There are two outputs in PFD called UP and DOWN which will be generated based on the difference of phase and frequency of the inputs of PFD [6]. Figure 2.1 shows the high level block diagram of PFD.

Figure 2.1 : PFD Highest Level Block Diagram

The PFD produce the outputs either UP or DOWN based on which input signal leads the other as the inputs for the CP. There are several types of architecture for PFD. A NAND based PFD is preferred in Complementary Metal-Oxide Semiconductor,CMOS design. Figure 2.2 shows the NAND based PFD utilized as a part of this work.

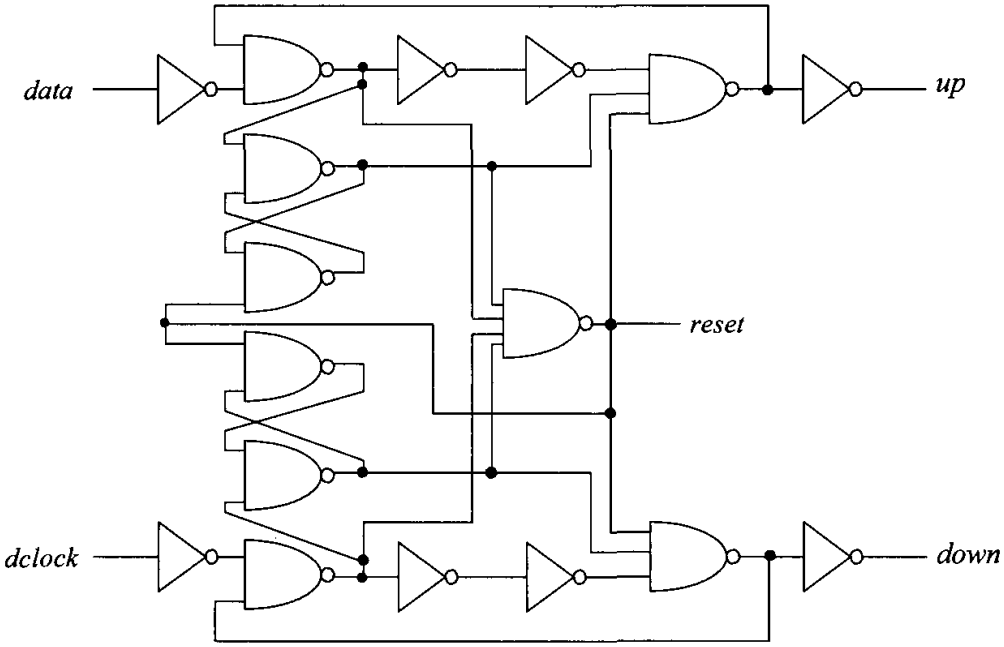


Figure 2.2: NAND based PFD [12]

A charge pump, CP converts the PFD outputs into charge. The PMOS and NMOS transistors work as switch. The motivation behind CP is to change the logic states of PFD to appropriate analogue signals for controlling the VCO. [13] Figure 2.3 shows the basic CP design. When the PFD outputs UP, M2 transistor turns on and current, I_{PDI} which is proportional to the pulse width will flow out while the M1 turns off. When PFD yields an output of DOWN, M1transistor will be active and current, I_{LPF} will be discharged to ground. I_{LPF} is the output current and can be written as [14],

$$I_{LPF} = \frac{I_{Pump}-(-I_{Pump})}{4\pi} \times \Delta\emptyset = K_{PFD} \times \Delta\emptyset$$

Where $\Delta\emptyset = Phase\ difference$ and, $K_{PDI} = \frac{I_{Pump}}{2\pi}$

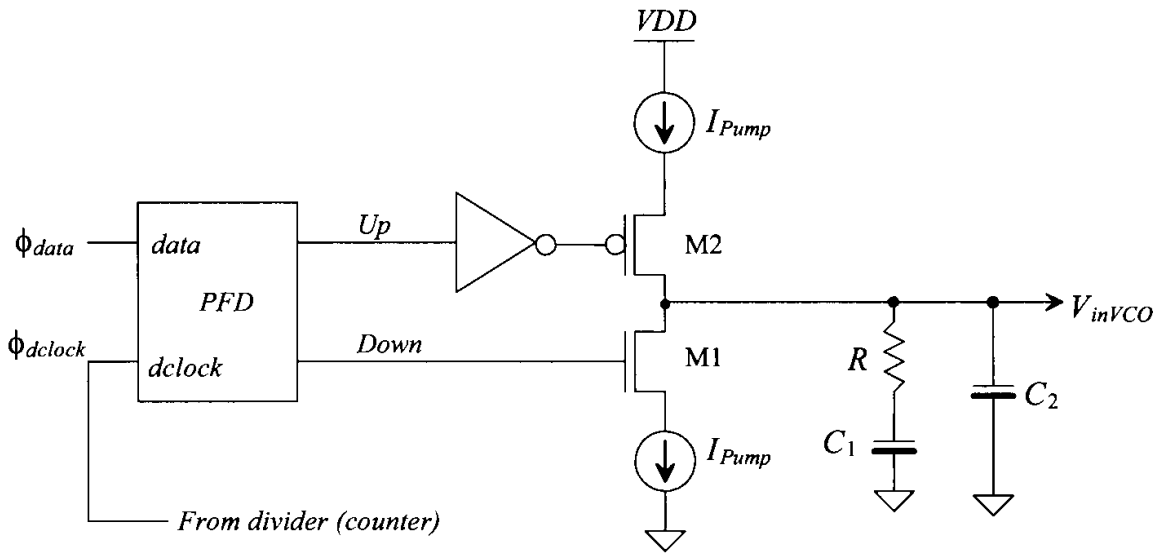


Figure 2.3: Basic Charge Pump Circuit with Low Pass Filter [12]

The I_{LPF} will have high dc components and some amount of ac components. The loop filter is used to filter those ac components. In this work we used a passive low pass filter, LPF. It is an important component for maintaining the stability. The LPF ideally helps in providing a constant voltage to VCO's input [14].

The next block is Voltage Controlled Oscillator. VCOs are crucial integral part in phase locked loops, frequency synthesizer and in nearly all digital and analog systems. This electronic device which uses amplification, feedback, and resonant circuit produce a repeating voltage waveform at specific frequency. [15]The clock frequency produced by VCO very controllable. There are several types of design for VCO for example Current-Starved VCO and Source-Coupled VCO. A Current Starved VCO is used in this work. Figure 2.4 shows a basic Current-Starved VCO.

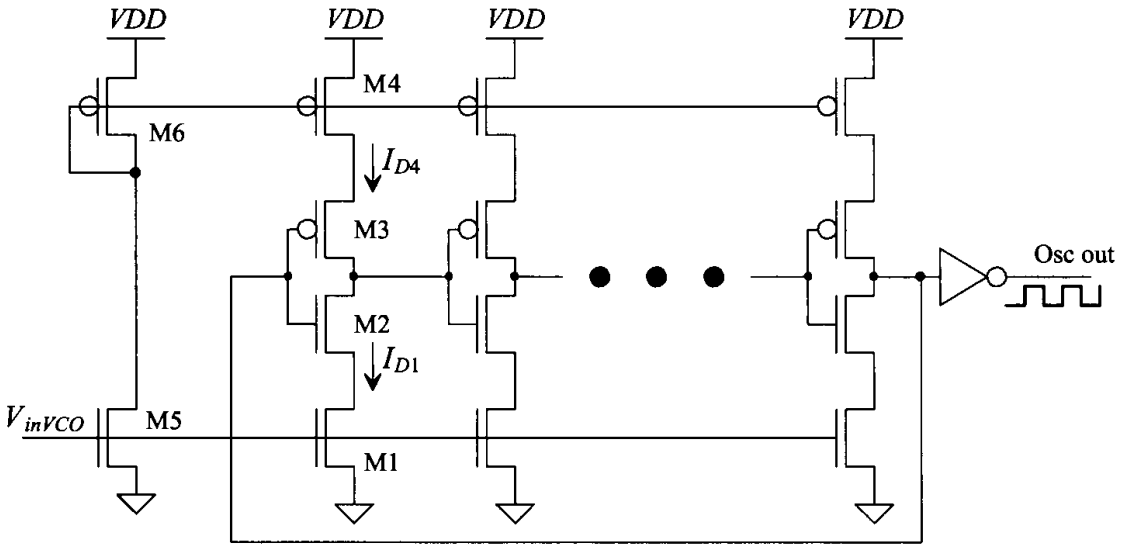


Figure2.4 : Current Starved VCO [12]

The last block in PLL is the divide by N counter. The function of this block is to divide the frequency of the VCO output signal [2]. Then then output of this block will be connected as one of the input of PFD. PLL use frequency divider in order to yield frequency which is a multiple of the reference frequency. The relationship between reference frequency and output frequency is,

$$f_{out} = N \times f_{ref}$$

2.2 Past Researches and Its Limitations

Many have tried new techniques to solve problems arrive in PLL. One of the problems faced in PLL is longer settling time. The papers [16] [17] [18] [19] emphasis on the minimising the settling time. Table 2.1 show the comparison between those three researches.

Technology	0.13µm CMOS[15]	0.18µm CMOS[16]	0.65µm CMOS[17]	0.6µm CMOS[18]
Input Frequency, GHz	10	10	138-148.5	10
Output Frequency, GHz	2.32-2.56	5.27-5.6	8.9-9.5	-
Locking time, µs	2.48	60	4.23	10
Supply Voltage, V	1.2	1.8	1.2	3.0
Power consumption,	-	-	63.9mW	15mW

Table 2.1 Comparison of Techniques

In the study [16] a Phase Error Cancellation technique is implemented. This method works by cancelling the phase error when the output frequency of PLL is near to target value which directly cut off the extra time needed for the overshoot to occur. While in [17] they used a method in which during the locking process the polarity and magnitude of the phase error at the phase-frequency detector will be observed. If phase error is detected, by changing the divide ratio of the frequency divider it will be solved. In this design the phase error will be kept small throughout the process of frequency acquisition thus reducing the settling time. Furthermore an auxiliary charge pump is added in the design to improve the locking speed.

In [18] Fast-Lock Hybrid PLL Combining Fractional-N and Integer-N Modes of Differing Bandwidths method is being used. By using this method, the PLL will operate in narrower-bandwidth, integer-mode during phase lock while during transient it will operate in wider-bandwidth, fractional-mode.

While the method used in [19] is Adaptive Bandwidth control. The working principle of this method is the PLL increases the loop bandwidth when the phase error is large and the other way around when the phase error is small. There are studies done in charge pump phase locked loop as in [20]. In this research linear and nonlinear models were used to analyse digital sequential phase frequency detector. First order, Second order and Third order PLLs were introduced and explained in detail. Finally importance of loop delay and its functions were discussed in the paper.

In [21] a conventional charge pump is modified using due to the drawback which is the voltage jump phenomenon which in turn cause the VCO output frequency to be unstable. The technique used was current steering and to increase the switching speed and decrease power consumption a gain enhancement technique is implemented. This charge pump design can be used in low power consuming PLL. The Voltage-Controlled Oscillator is the brain of a PLL. Paper [22] researched on ways to maximise the oscillation frequency of CMOS. The first technique is concentric layout technique in which effort is taken in minimising the drain and source area. Next method is use NMOS transistor as active load as the VCO's frequency increase together with transconductance per unit capacitance (gm/C) of the active load. Other than that, combination of both methods was used and the result is a 4 GHz high operation frequency is yielded.

In [23], two designs for Current-Starved Voltage Controlled Oscillator are discussed. Those are Current-Starved NAND based VCO (CSN-VCO) and Current-Starved Delay based VCO (CSD-VCO). The design of ring oscillator using series of delay cell stages is preferred due to several reasons as stated below.

1) Oscillation require lower control voltage

2) Electrical tuning and wide range.

3) Low power dissipation while providing higher frequency of oscillations.

4) Possibility to obtain multiphase output due to their basic structure

This study shows that CSN-VCO and CSD-VCO have large gain and higher tuning range and are appropriate for PLL application which requires wide band and quick locking.

Next, [24] researched on frequency divider. Methods on how to design a Divide-By-4 frequency divider is explained in detail. The technique used is Injection Locked Frequency Divider (ILFD). This circuit has two stage ring oscillator and two injectors. A differential and Single-Ended injection was practiced. The mechanism is, after a signal is injected an asymmetric electrical characteristic will be created. There are two ways to do this. One is Single-ended signal is injected at the same time to both injectors, and another is signal is injected to one injector and to ground the gate of another injector. The locking range of divde-by-4 can be extended by changing the dc bias of the injector gate.

Last, in [2] an Integer-N based divider is used for Bluetooth receiver. This design of PLL includes a tri state PFD with charge pump, LC Quadrature VCO with capacitor bank, third order phase loop and a programmable divider. The frequency divider has prescaler value of 8/9, 3-bit counter and 5-bit counter. The limitation of this method is the frequency tuning step is higher than that needed by Bluetooth specification channel spacing. A delta-sigma modulator is suggested to add in the design to get a Fractional-N PLL.

CHAPTER 3

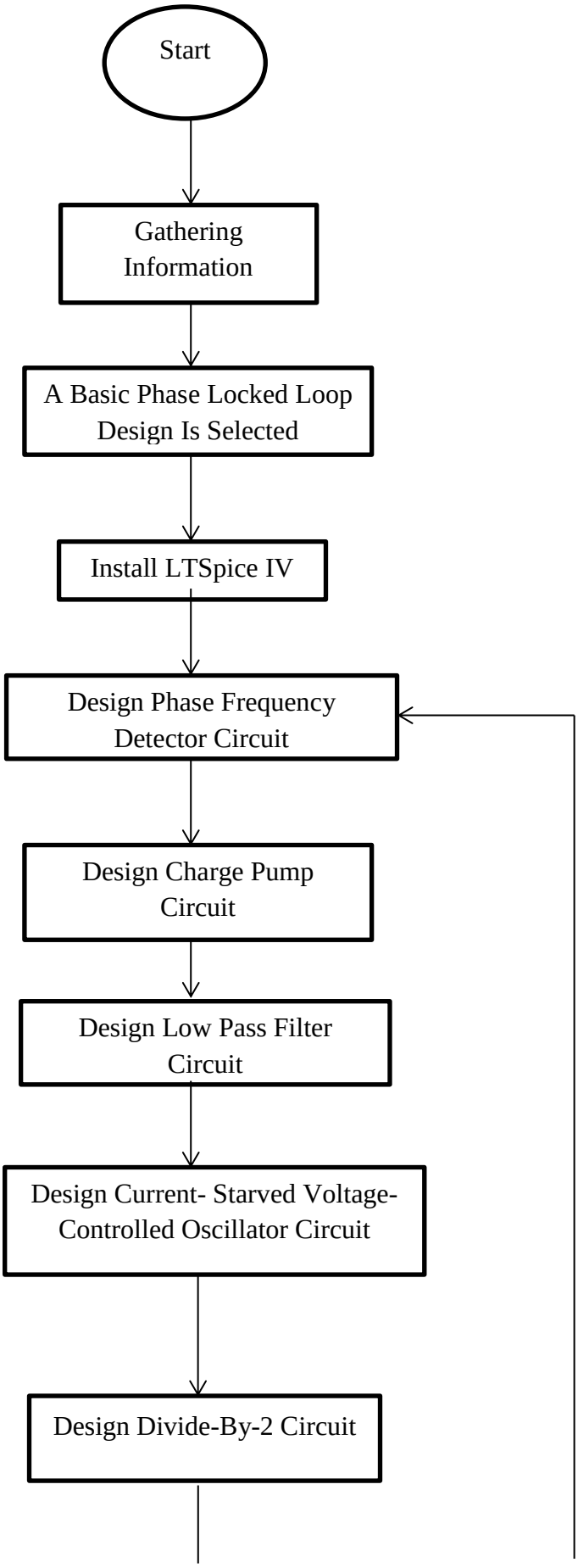
METHODOLOGY

3.1 Introduction

This chapter details the methodology carried out in this research. Preliminary works need to be done before proceeding to the simulation of the phase locked loop, in order to produce and outline of the process involved in the designing process. In the preliminary stage, a basic phase locked loop structure will be selected with phase frequency detector, charge pump, low pass filter, voltage-controlled oscillator and divide-by-2 counter. Then according to the specification needed for the Bluetooth radio, modifications will be done on the basic structure. In this project the basic Phase Locked Loop circuit is obtained from Jacob Baker's website [25]. Figure 3.1 is the Flow chart that shows the overall process of the research.

3.2 Project Implementation Flow

A project flow chart is done to control and to ensure the whole project can be completes systematically and successfully. Information is to be gathered first before anything. Literature review, journals, proceedings and more related to this project are gathered to support and improve the project. A basic phase locked loop design is chosen and developed in LTSpice IV. Check the design whether is meets the specifications needs or not. If it meets the project ends. If it doesn't, reengineer the design and test again. Figure 3.1 show the overall flowchart for this project implementation.


Start
Gathering Information
A Basic Phase Locked Loop Design Is Selected
Install LTSpice IV
Design Phase Frequency Detector Circuit
Design Charge Pump Circuit
Design Low Pass Filter Circuit
Design Current- Starved Voltage-Controlled Oscillator Circuit
Design Divide-By-2 Circuit

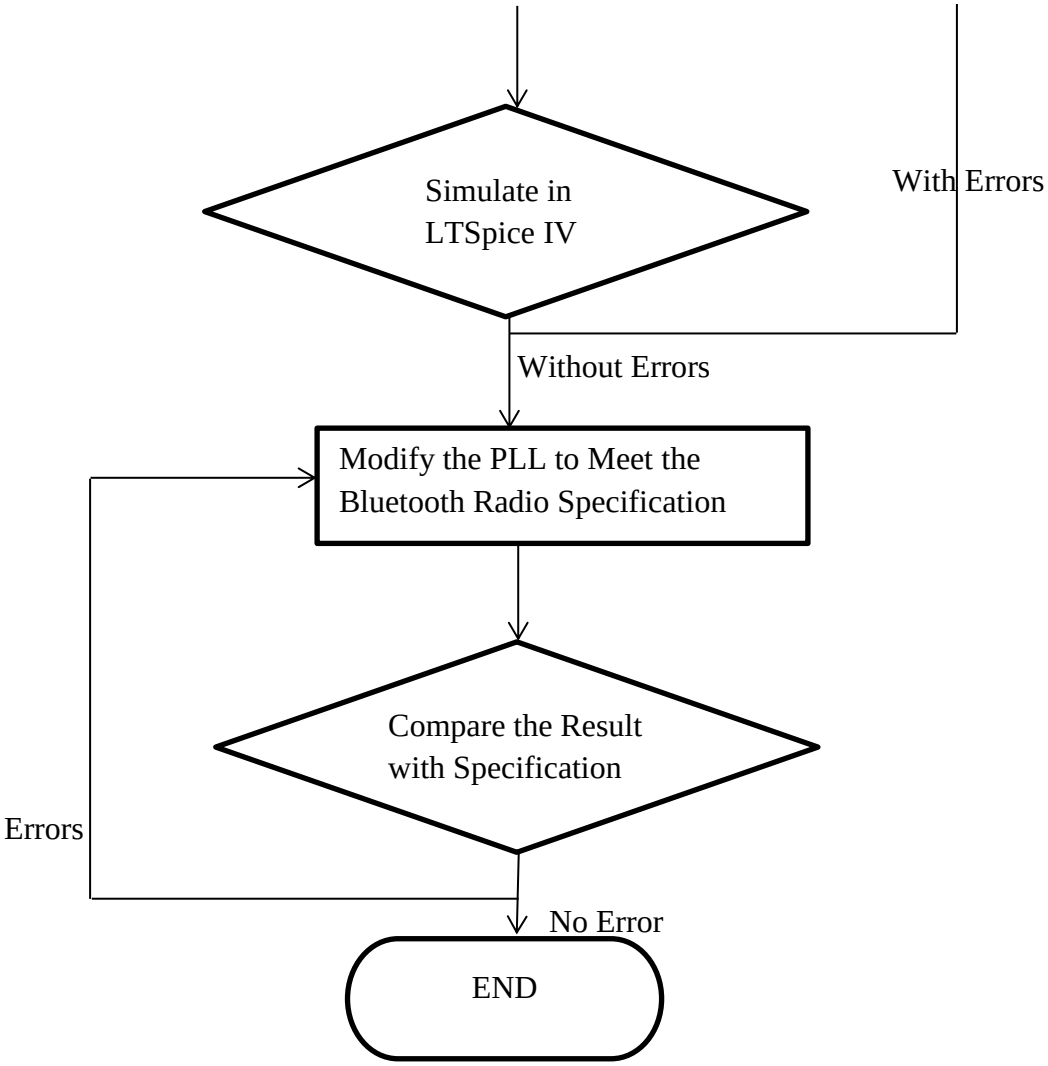


Figure 3.1 Overall Project Implementation Flow Chart

3.3 Designing Phase Frequency Detector

Phase Frequency Detector has two inputs. One is from the divide-by-2 counter and another from reference signal. The PFD used in this study is NAND based. In this design of PFD nine NAND gates and eight inverters were used. The delay through the two inverters can be used to set how *up* and *down* behave and to increase the delay so the PFD works smoothly. Figure 3.2 shows the PFD circuit used in this design. Figure 3.3 shows the NAND gate with 4 inputs. Figure 3.4 shows NAND gate with 2 inputs and Figure 3.5 shows Inverter used in the circuit. The outputs of the PFD are connected to inverters before entering charge pump.

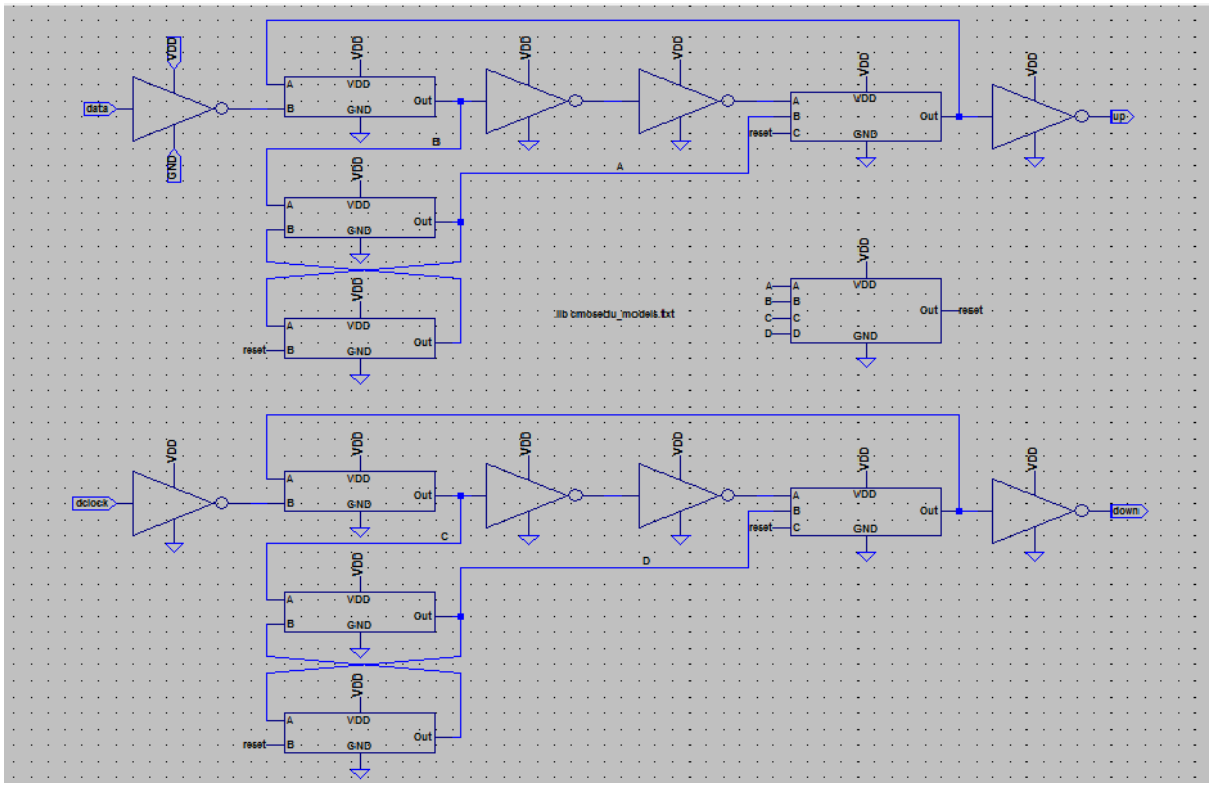


Figure 3.2 NAND Based Phase Frequency Detector

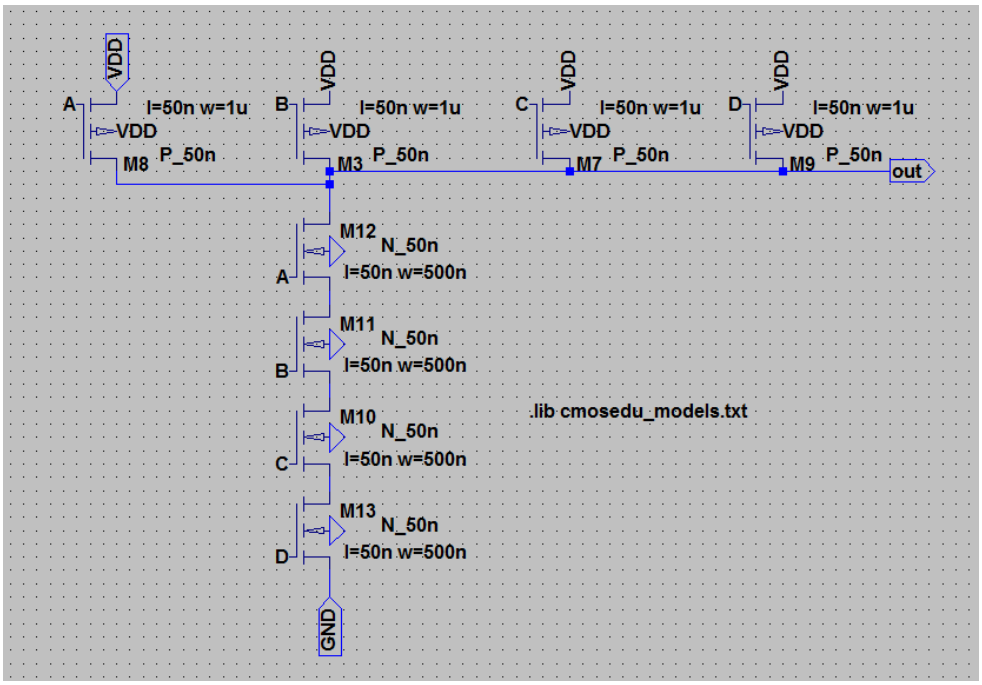


Figure 3.3 4 Input NAND Gate

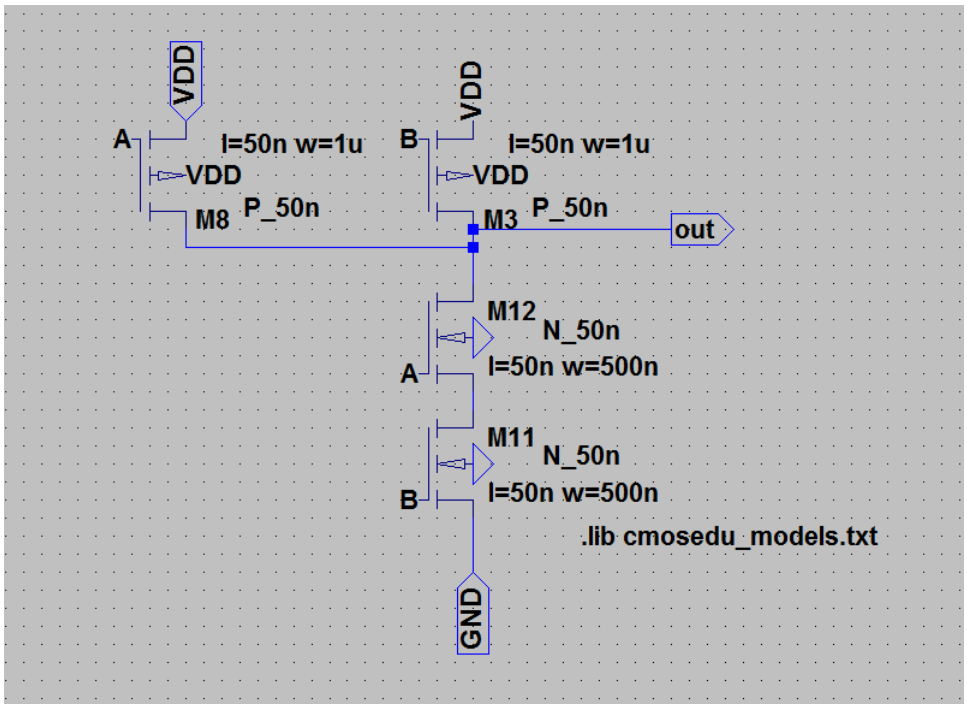


Figure 3.4 2 Input NAND Gate

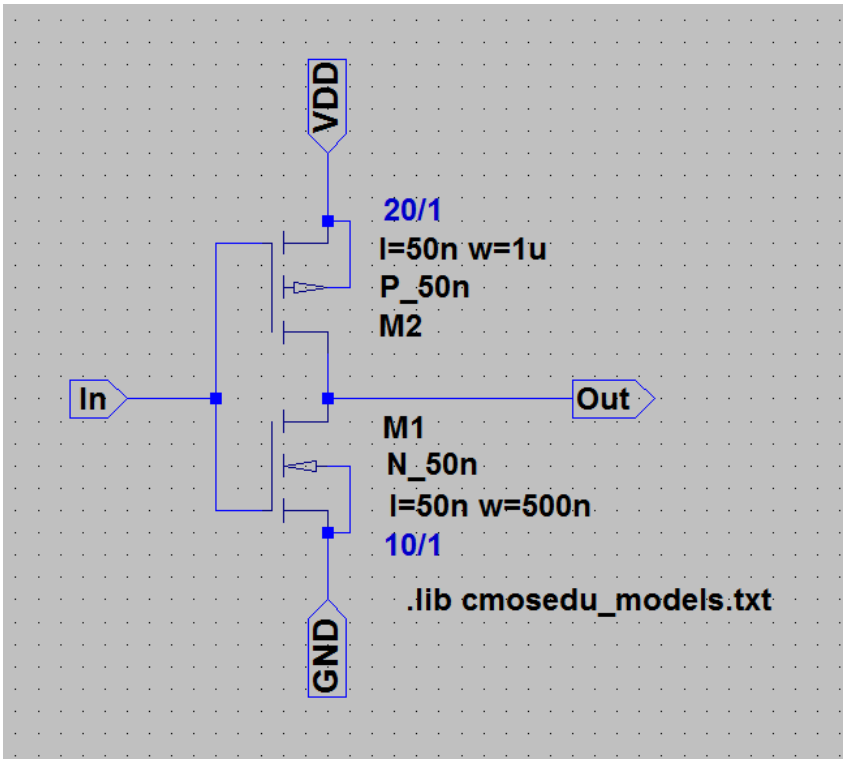


Figure 3.5 Inverter

3.4 Designing Charge Pump and Low Pass Filter Circuits

A basic charge pump circuit is modified as there were issues with the conventional design. In this study, the bias voltages come from diode-connected MOSFETs and from current mirrors. The current supplied was 2 mA. The W/L ratio of the diode connected transistors had to be much larger than the transistors connected to their bases to prevent channel width modulation as well as making sure the current mirror was able to pass enough current to keep the transistors in their required area of operation. The inverted outputs from PFD called UPI and DOWNI is channelled into M2 and M3 respectively. A passive low pass filter is used in this PLL. The capacitance value C1 is 310 pF. The resistor used has a value of 10 Ω.This charge pump and low pass filter is the modified version of the basic circuit. In the basic circuit the charge pump is able to provide 647.10 mV as the biasing voltage. Other than that all the width to length ratio of transistors are altered to provide the required voltages.

Furthermore, the low pass filter used in the basic circuit is replaced with the low pass filter with above mentioned specifications. Figure 3.6 shows the charge pump and low pass filter circuit.

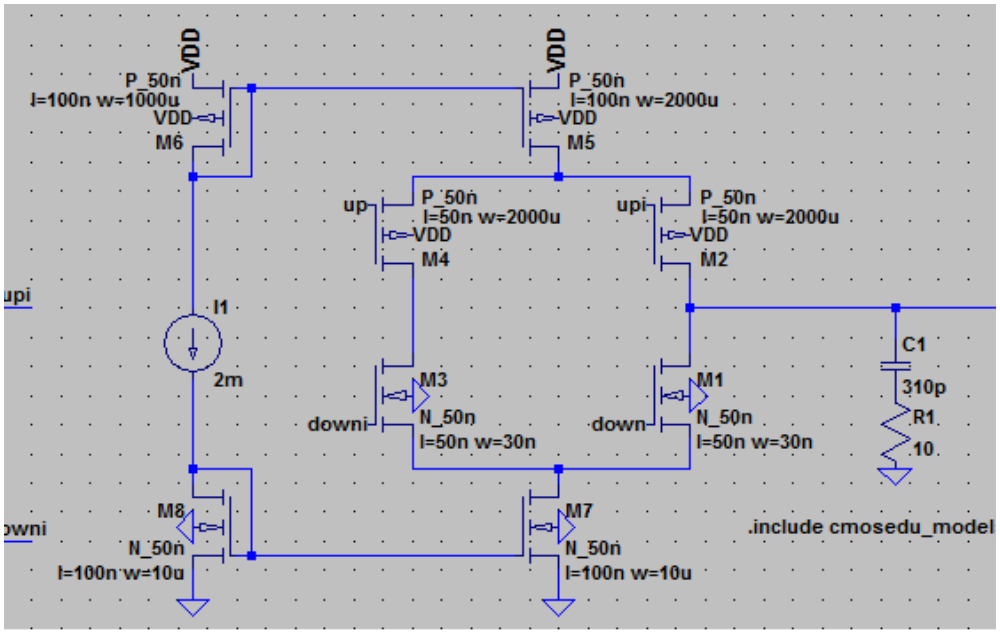


Figure 3.6 Charge Pump and Low Pass Filter

3.5 Designing a Current-Starved Voltage-Controlled Oscillator

Voltage-Controlled Oscillator is the brain of PLL. In this study, a current-starved VCO is used. The number of stages of ring oscillator must be odd number. There are 5 stages in this VCO circuit. The basic circuit obtained from Jacob Baker's website has 21 stages. The maximum frequency of the signal obtained from that circuit is 187.46 MHz which was far less than this project's requirement. Thus the circuit was modified to give output with 2.4 GHz. Based on the control voltage from the low pass filter, the VCO will outputs signal with varying frequency. Figure 3.7 shows the CS-VCO circuit. Figure 3.8 shows the schematic circuit of Current Starved Inverter, CS-INV used in this research.

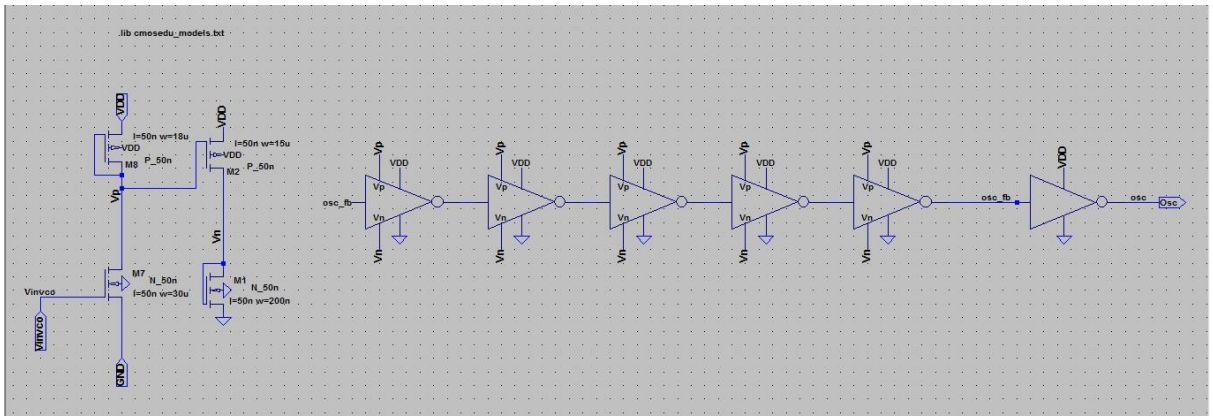


Figure 3.7 Current-Starved Voltage-Controlled Oscillator

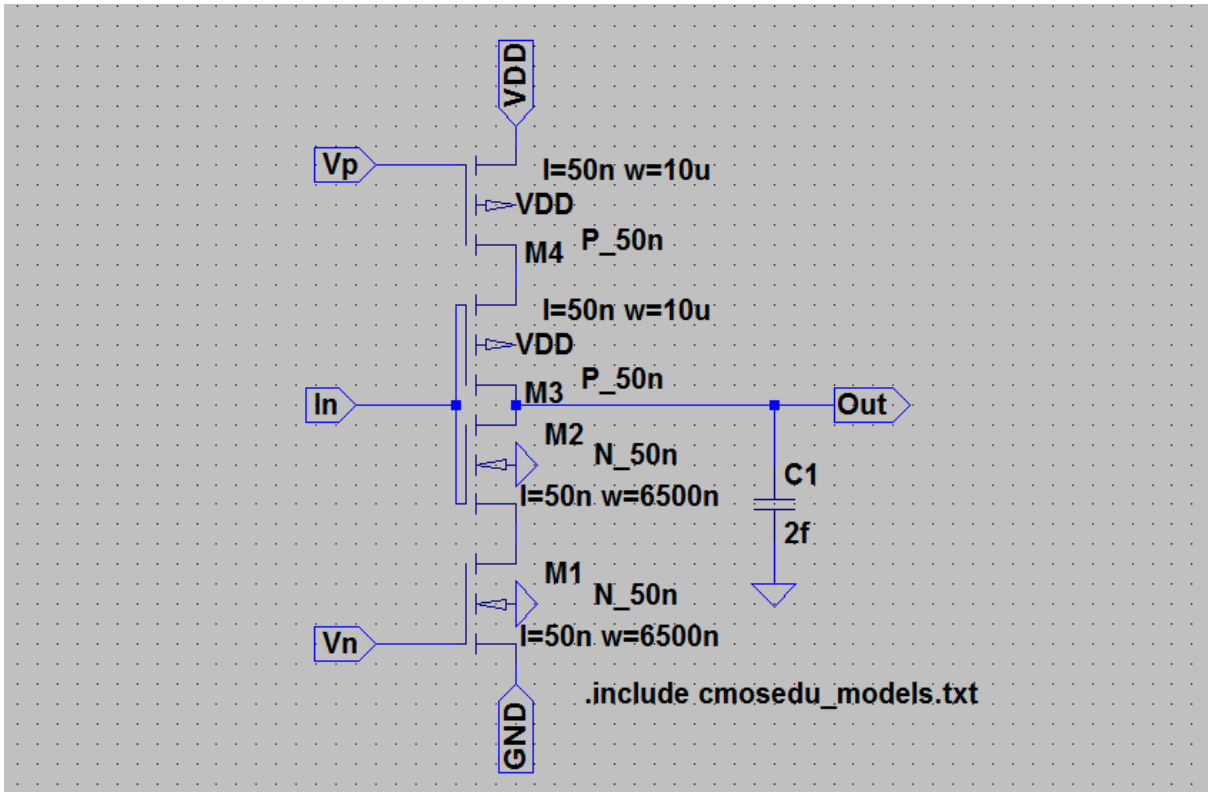


Figure 3.8 Schematic circuit of CS_INV

3.6 Designing Divide-by-2 Counter

This is basically a frequency divider. The divide-by-2 circuit was done using True Single Phase Clock (TSPC). It uses nine transistors. Figure 3.8 shows an example of output form TSPC divide-by-2 circuit. Figure 3.9 shows the TSPC divide-by-2 circuit used in this

study. Figure 3.10 shows five TSPC divide-by-2 circuit blocks being connected in series in this PLL. This made the overall divider value to become 32.

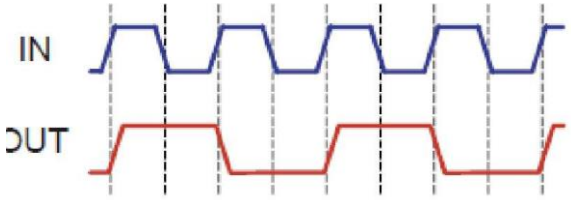


Figure 3.9 Example of Divide-By-2 Circuit Output

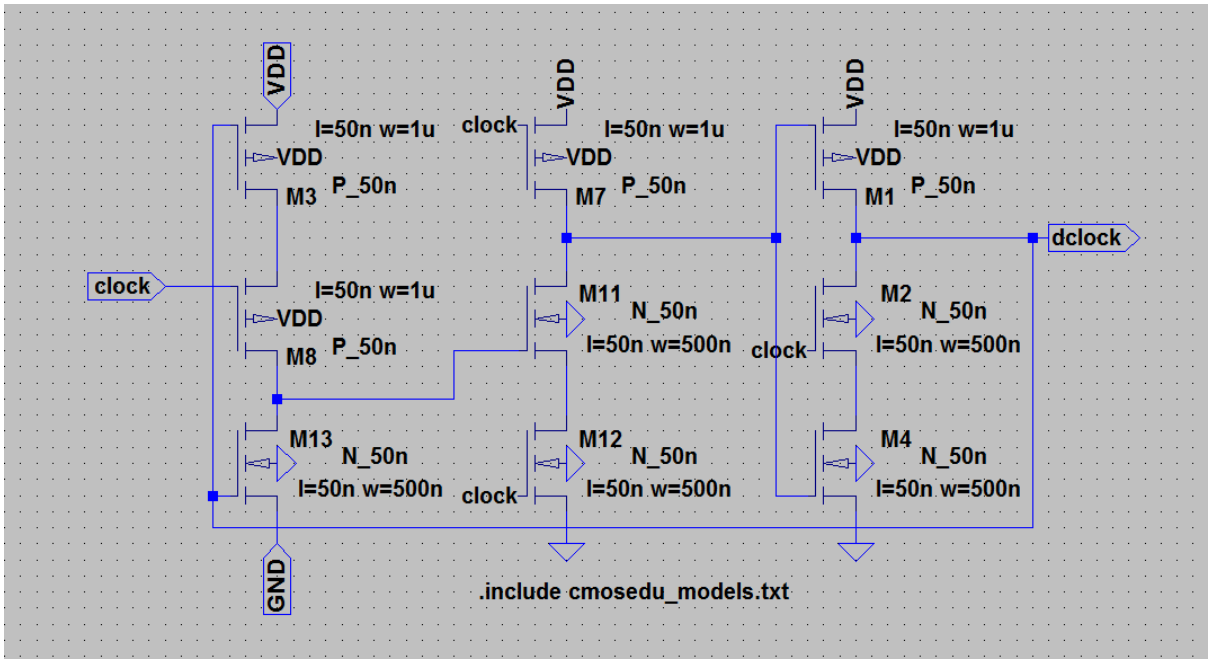


Figure 3.10 Divide-By-2 Circuit Using TSPC Topology

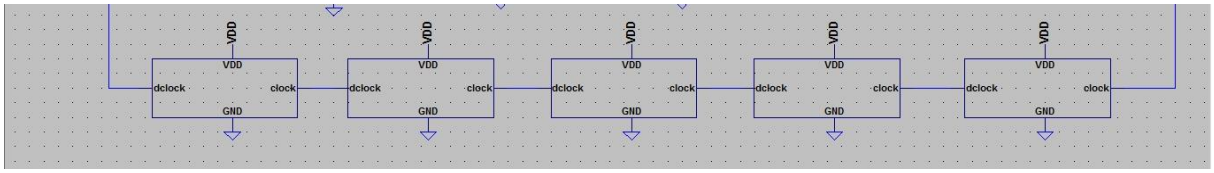


Figure 3.11 Five TSPC divide-by-2 Circuit Blocks Connected in Series

3.7 Integration of All Parts.

After designing the circuits individually, the integration was done. Figure 3.11 shows the overall PLL circuit.

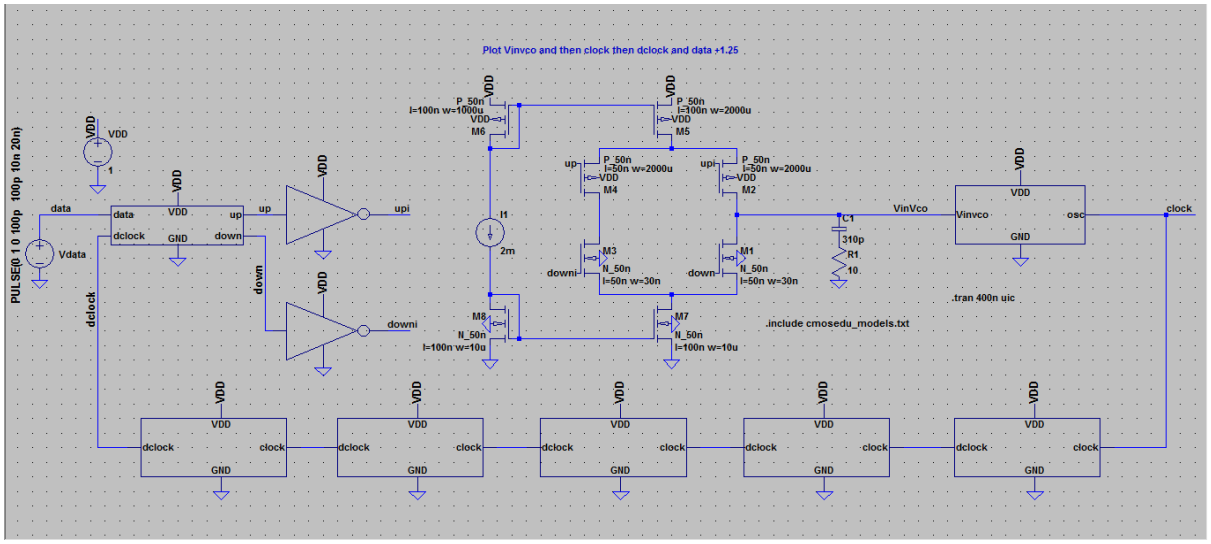


Figure 3.12 Overall PLL Circuit

CHAPTER 4

RESULTS AND DISCUSSION

This chapter shows the simulation results and discussion in this research. An input value is fixed in order to achieve an appropriate output value in the simulation. The input value used in this research is 50 MHz. The input is chosen to be 50 MHz which is within the lock in range of the PLL. The lock in range is 28.57 MHz to 66.67 MHz. The tool used for simulation is LTSpice IV Version 4.231.

4.1 Phase Frequency Detector Output

Once the inputs of the Phase Frequency Detector are given after the power supply of 1V is connected it gives outputs either UP or DOWN. The Phase Frequency Detector gives an Up signal when the reference signal which is 50 MHz leads the output from the series blocks of divide-by-2 counters. It gives a DOWN signal if the situation is other way around. Figure 4.1 shows the inputs and outputs of Phase Frequency Detector. The red line shows UP signal, light blue line shows DOWN signal, dark blue line shows output of Frequency Divider and green line shows input signal. The results shows that the output from the series connected divide-by-2 blocks which is “dclock” signal leads the reference signal which is “data” signal almost all the time except at the beginning. This is because of output goes to high-impedance mode where it keep on producing either positive or negative current pulses. This is the drawback of this design.