MODELLING AND SIMULATION OF LARGE SIGNAL AND POWER DELIVERY NETWORKS ON IC AND PCB

SARVVIN A/L T.KALITHAS

UNIVERSITI SAINS MALAYSIA

2017

MODELLING AND SIMULATION OF LARGE SIGNAL AND POWER DELIVERY NETWORKS ON IC AND PCB

by

SARVVIN A/L T.KALITHAS

Thesis submitted in partial fulfilment of the requirements for the degree of Bachelor of Engineering (Electronic Engineering)

JULY 2017

TABLE OF CONTENTS

| TABLE OF CONTENTSii |
|--|
| LIST OF FIGURESiv |
| LIST OF TABLES |
| LIST OF ABREVIATIONvii |
| ABSTRACTviii |
| ABSTRAKix |
| CHAPTER 1: INTRODUCTION |
| 1.1 Overview |
| 1.2 Problem Statement |
| 1.3 Research Objectives |
| 1.4 Research Scope |
| 1.5 Thesis Outline |
| CHAPTER 2: LITERATURE REVIEW6 |
| 2.1 Overview |
| 2.2 Signal and Power integrity |
| 2.3 PDN modelling and Circuit Simulation Technology7 |
| 2.3.1 PDN modelling7 |
| 2.4 Latency Insertion Method (LIM) |
| 2.4.1 Basic Linear Formulation of LIM10 |
| CHAPTER 3: METHODOLOGY 15 |

| 3.1 | Introduction | 15 |
|--------|---|----|
| 3.2 | Flow Chart | 16 |
| 3.3 | Project requirements | 17 |
| 3.4 | Project design 1 | 19 |
| 3.5 | Summary | 20 |
| СНАР | TER 4 | 21 |
| 4.1 | Introduction | 21 |
| 4.2 | PDN Modelling | 21 |
| | 4.2.1 PDN Modelling for 10 nodes | 21 |
| | 4.2.2 PDN MODELLING FOR 100 NODES | 26 |
| 4.3 | Simulation result | 30 |
| | 4.3.1 Simulation results for 10 node PDN model | 30 |
| | 4.3.2 Simulation result for 100 nodes PDN model | 34 |
| 4.4 \$ | Summary | 37 |
| СНАР | TER 5: CONCLUSION | 38 |
| 5.1 | Conclusion | 38 |
| 5.2 | Recommendation | 38 |
| REFEI | RENCES | 39 |
| APPE | NDIX3 | 9 |

LIST OF FIGURES

| | | Page |
|-------------|--|------|
| Figure 1.1 | (a) Voronoi diagram of conductor surface; (b) Equivalent | 2 |
| | circuit [4] | |
| Figure 2.1 | Discrete distributed model for uniform transmission line [9] | 9 |
| Figure 2.2 | Network with interconnect topology [10] | 9 |
| Figure 2.3 | LIM branch equivalent circuit [9] | 10 |
| Figure 2.4 | LIM node equivalent circuit [9] | 11 |
| Figure 2.5 | Result obtained from basic LIM and improved LIM [5] | 14 |
| Figure 3.1 | Flowchart of the project | 16 |
| Figure 3.2 | Flow chart for voltage in current LIM formula | 18 |
| Figure 4.1 | Voronoi diagram for 10 nodes | 21 |
| Figure 4.2 | Delaunay triangulation for 10 nodes | 22 |
| Figure 4.3 | Voronoi diagram for 100 nodes | 23 |
| Figure 4.4 | Delaunay triangulation for 100 nodes | 24 |
| Figure 4.5 | Simulated circuit using Ltspice software | 30 |
| Figure 4.6 | Graph of voltage at node 1 using Ltspice software | 30 |
| Figure 4.7 | Voltage at node 1 by LIM formula | 31 |
| Figure 4.8 | Voltage at node 1 by voltage in current LIM formula | 31 |
| Figure 4.9 | Comparison between LIM voltage in current and basic LIM | 32 |
| | with different time steps | |
| Figure 4.10 | Voltage at node 9 LIM formula | 32 |
| Figure 4.11 | Voltage at node 9 by voltage in current formula | 32 |

| Figure 4.12 | Comparison between LIM voltage in current and basic LIM with different time steps | 33 |
|-------------|---|----|
| Figure 4.13 | Graph of voltage at node 1 using LtSpice | 34 |
| Figure 4.14 | Voltage at node 1 using LIM fomula | |
| Figure 4.15 | Voltage at using node 1 simulated using voltage in current | 35 |
| | LIM formula | |
| Figure 4.16 | Comparison between LIM voltage in current and basic LIM | 35 |
| | with different time steps | |
| Figure 4.17 | Voltage at node 9 using LIM fomula | 36 |
| Figure 4.18 | Voltage at node 9 using voltage in current LIM fomula | 36 |
| Figure 4.19 | Comparison between LIM voltage in current and basic LIM | 36 |
| | with different time steps at node 99 | |

LIST OF TABLES

| | | Page |
|-----------|---|------|
| Table 1.1 | Comparison of run times between SPICE and LIM [5] | 2 |
| Table 2.1 | Numerical result comparison between LIM and LILIM [4] | 12 |
| Table 2.2 | Comparison between LIM, LtSPICE and Proposed Method | 13 |
| | [3] | |
| Table 3.1 | Parameters involved in capacitor and inductor calculation | 17 |
| Table 4.1 | Calculated areas of the voronoi diagram | 23 |
| Table 4.2 | Calculated value of length of voronoi edge | 23 |
| Table 4.3 | Calculated value of length of triangular mesh | 24 |
| Table 4.4 | Capacitor values for 10 nodes | 25 |
| Table 4.5 | Inductor values for the branch | 25 |
| Table 4.6 | Capacitor values for 100 nodes | 28 |

LIST OF ABREVIATION

| ADAMS | Automated Dynamic Analysis of Mechanical Systems |
|-------|---|
| IC | Integrated Circuit |
| KCL | Kirchhoff's current law |
| LILIM | Locally Implicit Latency Insertion Method. |
| LIM | Latency Insertion Method |
| M-TEM | Multilayer Triangular Method. |
| PCB | Printed Circuit Board |
| PDN | Power Distribution Network |
| SPICE | Simulation Program with Integrated Circuit Emphasis |
| SSN | Simultaneous Switching Noise |
| VLSI | Very-Large-Scale Integration |

MODELLING AND SIMULATION OF LARGE SIGNAL AND POWER DELIVERY NETWORKS ON IC AND PCB

ABSTRACT

This project presents the PDN model and simulation of PDN and large power networks. The PDN network was simulated using MATLAB software. The PDN modal was built by using some efficient method. To get an accurate answer for the simulation the PDN modal was built using triangular meshes method. The built model will be simulated with LIM formula in MATLAB. Since the basic LIM formula has numerical stability problem. The formula was altered and updated to overcome the stability problem. The altered formula was used to simulate the built model. The built model will be simulated using SPICE simulator. The result obtained in two kind of simulator will analysed and discussed in this project. The obtained result from this experiment is that for basic LIM formula we have to use smallest time step to ensure the numerical stability of the formula. While for the altered LIM formula we can use larger time step compared to the time step used in basic LIM formula.

PEMODELAN DAN SIMULASI BESAR SIGNAL AND POWER DELIVERY NETWORKS ON IC DAN PCB

ABSTRAK

Projek ini membentangkan model PDN dan simulasi PDN dan rangkaian kuasa besar. Rangkaian PDN telah simulasi menggunakan perisian MATLAB. The PDN modal dibina dengan menggunakan kaedah beberapa cekap. Untuk mendapatkan jawapan yang tepat untuk penyelakuan yang PDN modal dibina menggunakan kaedah jerat segi tiga. Model dibina akan disimulasikan dengan LIM formula dalam MATLAB. Sejak formula LIM asas mempunyai masalah kestabilan berangka. formula yang telah diubah dan dikemaskini untuk mengatasi masalah kestabilan. Formula diubah digunakan untuk mensimulasikan model yang dibina. Model dibina akan disimulasikan menggunakan SPICE simulator. Keputusan yang diperolehi dalam dua jenis simulator akan dianalisis dan dibincangkan dalam projek ini. keputusan yang diperolehi dari eksperimen ini ialah untuk formula asas LIM kita perlu menggunakan terkecil langkah semasa bagi memastikan kestabilan berangka formula. Manakala bagi formula LIM yang diubah kita boleh menggunakan lebih besar langkah masa berbanding langkah masa yang digunakan dalam formula LIM asas.

CHAPTER 1

INTRODUCTION

1.1 Overview

The vigorous evolution in the integrated circuit (IC) industry and development of wireless communication and portable computer markets at both electronic chip and package level made the transistors are consistently migrated to smaller dimension and becoming more efficient [1]. Besides that, when the size reduces, the cost per unit decreases as well. The above situation has led to complication related with power distribution due to the voltage reduction.

The current inclination in the very-large-scale integration (VLSI) industry towards miniature designs, low power consumption, and increased integration of analog circuits with digital blocks has made the signal integrity analysis a challenging undertaking [2]. It is very important to ensure the power and signal integrity so that the circuit or printed circuit board (PCB) maintain optimum function and can fulfil its fundamental characteristics. Technologies has made the IC circuits to package in small area. Irregular shaped Power Distribution Networks (PDN) are arranged in chips just to supply power to every single system. The simultaneous switching noise (SSN) produced by expanded power density and shorter signal edges straightforwardly lowers the power integrity of the recent low-voltage PDN [3]. To ensure the power and signal integrity of the chip, PDN must be modelled and simulated efficiently and correctly. One of the efficient modelling method is with triangular mesh. This modelling types utilize Delaunay triangulation, which will produce Delaunay mesh and Voronoi diagram. The Voronoi diagram and its equivalent circuit is shown in Figure 1.1[4].



Figure 1.1 (a) Voronoi diagram of conductor surface (b) Equivalent circuit [4]

Circuit simulation is a fast and cheap way to estimate the operation of circuits before fabricating them. Furthermore, circuit simulation is the industry-standard way to validate the operation and actual function of the circuit. The difficulty of simulation increases as the components in the circuit increases. A conventional circuit simulator, such as Simulation Program with Integrated Circuit Emphasis (SPICE) relies on the solution of large matrix equation which is slow. The Latency Insertion Method is a suitable method to perform fast simulation of very large circuits. LIM is a faster method to simulate the circuit compared to SPICE. This is shown in Table 1.1 by comparing the run times between the two methods.

| Number of Nodes | SPICE (sec) | LIM (sec) |
|-----------------|-------------|-----------|
| 1,000 | 9 | 0.25 |
| 10,000 | 334 | 4 |
| 15,000 | 701 | 6 |
| 20,000 | 1224 | 9 |
| 25,000 | 1892 | 11 |
| 30,000 | 2935 | 13 |

Table 1.1 Comparison of run times between SPICE and LIM [5]

LIM needs to exploit the latencies in the circuits by having latency elements in each node and branch. Although LIM is the efficient method of circuit simulation but it has its own limitations. The numerical stability is the disadvantage in LIM. So, to ensure the numerical stability few improved formulations has introduced. One of it is voltage-incurrent formulation. With this formulation, we can ensure numerical stability of LIM [5].

1.2 Problem Statement

Power and signal integrity is one of the major challenge faced in large signal and power delivery networks (PDN). Thus, to ensure the power and signal integrity we must model PDN and simulate it by using the exact methods. Usually PDN has a lot of nodes, thus more will be required to simulate the circuit by using SPICE. Many algorithms were introduced to solve this problem. One of the algorithm was the LIM. LIM is faster because it uses explicit methods based on finite-difference formulation. This algorithm ensures an efficient simulation even if all node voltages are calculated at each time step [6]. The LIM has some disadvantages also, and one of the highlighted problem of LIM algorithm is numerical stability. The maximum time step Δt , relies on the smallest inductance and capacitance in circuit [6]. In order to overcome the mentioned problem, a little alteration was made to the LIM formula to get an updated formula. The updated formula was the voltage-in-current LIM.

1.3 Research Objectives

- 1. To build a model of the large signal and power delivery networks.
- 2. To simulate the built model by using the LIM algorithms in MATLAB software.
- 3. To analyse the built model and simulation result based on the basic LIM algorithm and voltage in current LIM algorithm.

1.4 Research Scope

The research scope of this project can be divided into three parts which is model design, simulation and analysis. Firstly, the PDN model must be designed. Then, by researching the model designing method, the suitable method will be chosen. The designed PDN model must follow its requirements.

The built model will undergo the simulation process. The model used is the improved LIM formulation and will be simulated in MATLAB. Finally, will be the analysis. The simulated result will be analysed. Comparison will be done with other types of simulation method of the same model. Certain criteria will be analysed and discussed.

1.5 Thesis Outline

This research comprises of 5 chapters. In chapter 1, we discuss about the introduction of the research. A universal outline of the history, theory and concepts of circuit simulations, modelling method and the use of Latency Insertion Method are briefly discussed. The problem statement was then identified. Research scope with its objective is also presented in chapter 1.

Chapter 2 is the literature review activity that focuses on the important concepts and theory for research which have been carried out and established by researchers all over the world. The theory and modelling procedure are also presented in the literature review.

Chapter 3 revolves around the methodology of the research on the process of modelling and simulation of PDN. This chapter will give an in-depth idea on how the design procedures and algorithms that are performed and implemented. This chapter also shows the process flow involved in planning and taking to task of this project.

Chapter 4 highlights the result and discussion in the initial designing, application stage and also the analysis of the process. The result which are the generated from the simulation will be discussed and analysed.

Lastly, chapter 5 is the overall conclusion drawn after this project is accomplished. Experience and concrete knowledge is stated in this chapter. Practical recommendations to further enhance the research also presented in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

This section will introduce the basic concepts involved in this thesis. The technology in circuit simulation and various researches on building the model, formulation and algorithm of Latency Insertion Method (LIM) are presented. Firstly, the fundamentals involving the signal integrity and power integrity will be discussed. After that, key information in conjunction with modelling and simulation of large signal and power delivery networks in IC and PCB, then followed by PDN modelling and circuit simulation technology will be presented. The last part of this section will be used to discuss the previous work regarding LIM algorithm and alteration. Problems because of LIM and how alteration was made to the LIM formula to overcome it will also be discussed.

2.2 Signal and Power integrity

Signal integrity is defined as a set of measures of the output of an electrical signal. The easiest way to explain it is signal must be conserved and must be in the shape that we want. In the other side power integrity is defined as a study to check whether the needed voltage or current has received at a destination from the source. Power integrity and signal integrity are relatable because to maintain signal integrity, we need to design model for power integrity. Unfortunately, the relationship between signal and power integrity is not straightforward. In this advanced semiconductor world, designing for power integrity refers to managing the power supply noise across the voltage and ground terminals of the transistors in such they function at a speed [7]. Researchers had successfully brought up solutions in designing power and signal integrity.

2.3 PDN modelling and Circuit Simulation Technology

High speed applications, systems and components have gained much attention concurrently with the invention of smaller transistor. As the technology getting more advance, the simulation methods also has to be invented because new simulation methods has a great demand nowadays. The success of such technology are reliant on the need of profitable technology which is suitable for whole productions[2]. A lot of software follows this approach, with common examples being the SPICE family of electric circuit simulators and Automated Dynamic Analysis of Mechanical Systems (ADAMS) simulator for multi solid-body mechanics.

The simulation of large network is one of the major problem faced in computeraided design of integrated circuits. The simulation is more time consuming as network get bigger. So, some algorithms were introduced to simulate the circuit faster and also to gets the exact result. Thus, Latency Insertion Method (LIM) was introduced and this algorithm is very convenient for users as it can simulate large circuits in a fast manner.

2.3.1 PDN modelling

Current technologies have made the IC circuits to package in small areas. This made the PDN modelling more challenging. PDN must be modelled and simulated efficiently and correctly to ensure power and signal integrity. So, researchers came up with many methods that can be implemented in building the PDN model. Some of those methods includes square mesh method, triangular mesh method and multilayer triangular method (M-TEM).

For square mesh, it undergoes staircase approximation from the corner of the geometric structure[4]. The increment of unknown variables causes this problem. Thus,

square mesh is not a PDN modelling method and this needs further research on PDN modelling method.

Further research has led to the invention of triangular mesh modelling method. This method is one of the efficient method compared to square mesh method. This modelling method utilizes Delaunay triangulation, which will produce Delaunay mesh and Voronoi diagram. The Voronoi diagram and its equivalent circuit is shown in Figure 1. The value of capacitor and inductance of the circuit can be calculated using the following equations:

$$C_a = \varepsilon \frac{A_a}{h}$$
(2.1)

where, h = dielectric thickness (m)

 $\epsilon = permitivity$ $\mu = permeability$

 A_a = area of the vornoi diagram behind the node (m^2)

$$L_{ab} = \mu h \frac{d_{ab}}{l_{ab}}$$
(2.2)

where, $\mu = permeability$

 $d_{ab} = length of the Vornoi edge (m)$

 $l_{ab} = length of the edge in triangular mesh (m)$

Later on, researchers invented the multilayer triangular element method (M-TEM). This method creates a mesh using triangulation and its dual graph on the surface of a plane and applies Kirchhoff's current law (KCL) and Maxwell-Ampere's circuital law on the mesh [8].

2.4 Latency Insertion Method (LIM)

LIM is a method that approaches a circuit as a grid which is made up of branches that interconnects with nodes. In this study, distributed networks[9] are often used to describe signal propagation on uniform transmission lines as shown in Figure 2.1. This model is also a high frequency representation of an interconnection.



Figure 2.1 Discrete distributed model for uniform transmission line [9] Figure 2.2 shows a more general interconnection topology in which signals can propagate in more than one direction.

Such a model can be viewed as the high-frequency representation of an arbitrary network. In analysing an arbitrary network, we can define a branch as a connection between two nodes (excluding the ground reference node).



Figure 2.2 Network with interconnect topology [10]

LIM uses a finite difference formulation. Besides that, LIM will obtain the currents and voltage in a leapfrog manner. Leapfrog manner means that voltage and current are dependent on the pervious value. Furthermore, voltage and current are staggered by half a time step. Current are computed at whole time intervals, which will get I^n , I^{n+1} , I^{n+2} while for voltage are computed at half intervals where the sequence will be $V^{n-\frac{1}{2}}$, $V^{n+\frac{1}{2}}$, $V^{n+\frac{3}{2}}$. In each branch of LIM, there will be an inductor, resistance and a voltage source. This combination is shown in Figure 2.3.

In defining the desired topology for such analysis, each branch must have inductor to generate latency at the branch. Same goes to node, there must be a grounded capacitor so that it can generate latency at that node.



Figure 2.3 LIM branch equivalent circuit [9]

2.4.1 Basic Linear Formulation of LIM

As mentioned before, for LIM algorithm, each branch of the circuit must consist of inductance while each node must consist of capacitor. If a circuit does not obey this conditions, capacitor and inductance are added to the node and branch respectively to generate latency. The circuit shown in Figure 2.4 is used to express the discrete time equation for voltage.



Figure 2.4 LIM node equivalent circuit [9]

First, by applying Kirchhoff's voltage law for the circuit in Figure 2.4, the discrete time equation can be expressed as follows;

$$V_i^{n+\frac{1}{2}} - V_j^{n+\frac{1}{2}} = L_{ij} \left(\frac{I_{ij}^{n+1} - I_{ij}^{n}}{\Delta t} \right) + R_j I_{ij}^{n} - E_{ij}^{n+\frac{1}{2}}$$
(2.3)

Solving for the unknown current I_{ij}^{n+1} :

$$I_{ij}^{n+1} = I_{ij}^{n} + \frac{\Delta t}{L_{ij}} \left(V_i^{n+\frac{1}{2}} - V_j^{n+\frac{1}{2}} - R_j I_{ij}^{n} + E_{ij}^{n+\frac{1}{2}} \right)$$
(2.4)

Then, by using Kirchhoff's current law for the circuit in Figure 2.4, the equation can be expressed as shown:

$$C_{i}\left(\frac{V_{i}^{n+\frac{1}{2}}-V_{i}^{n-\frac{1}{2}}}{\Delta t}\right) + G_{i}V_{i}^{n+\frac{1}{2}} - H_{i}^{n} = -\sum_{k=1}^{M_{i}}I_{ik}^{n}$$
(2.5)

Which can be further rearranged to:

$$V_{i}^{n+\frac{1}{2}} = \frac{\frac{C_{i}V_{i}^{n-\frac{1}{2}}}{\Delta t} + H_{i}^{n} - \sum_{k=1}^{M_{i}} I_{ik}^{n}}{\frac{C_{i}}{\Delta t} + G_{i}}$$
(2.6)

where,

 M_i = Total number of branches connected to node i (excluding connection to the ground)

$$i = 1, 2...N$$

For each time step, node voltages and branch currents are computed using the updated expressions from Equation 2.5 and Equation 2.6. Node voltages are computed first then all branch current is updated.

Although the basic LIM formulation is recognized as the fastest way to simulate large network circuits but LIM has its disadvantages. The basic LIM's limitation is that it must fulfil time step size to obey the numerical stability condition[4]. The maximum step is dependent on the values of C and L of the circuit. Where the maximum step time must obey the following equation:

$$\Delta t < \sqrt{LC} \tag{2.7}$$

Due to this problem, researchers came out with an improved LIM which is called Locally Implicit Latency Insertion Method (LILIM). In which LILIM utilizes a locally implicit scheme rather than explicit leapfrog method [10]. Then the expected result from the LILIM algorithm could be obtained. It can simulate fast and it is numerically stable. The comparison results from LIM and LILIM method are displayed in Table 2.1.1.

Table 2.1 Numerical result comparison between LIM and LILIM [4]

| Method | CPU Time (s) | Speed-up |
|--------|--------------|----------|
| LIM | 59.719 | 1.00 |
| LILIM | 16.406 | 3.64 |

On the other side, further studies were made and researchers came up with a fullyexplicit and unconditionally stable difference scheme[3]. The idea of proposed method is main cause of the instability of the explicit method was determined by eigenvalue decomposition and then easy algebraic operation was performed to eliminate the stability. This proposed method gave an excellent result. The results are as shown in Table 2.2.

| Method | $\Delta t (ps)$ | CPU Time (ms) | Speed-up |
|----------|-----------------|---------------|----------|
| D 1 | 0.9 | 3140 | 109 |
| Proposed | 20 | 16 | 21462 |
| LIM | 0.9 | 16765 | 20 |
| | 20 | N/A | N/A |
| LtSPICE | 0.9 | 8143530 | 0.04 |
| | 20 | 343390 | 1 |

Table 2.2 Comparison between LIM, LtSPICE and Proposed Method [3]

Finally, new studies had invented updated formula which was named as Voltagein-current for the LIM. The main idea of this improved formula was implicitly substitute the voltage in the current is presented. By substituting node voltage formula into branch current formula and rearranging the equation obtained is as shown:

$$I_{ij}^{n+1} = \frac{\frac{L_{ij}}{\Delta t}I_{ij}^{n} + \frac{\frac{C_{i}}{\Delta t}v_{i}^{n} - \sum_{k=1,k\neq j}^{M_{i}}I_{ik}^{n+1} + H_{i}^{n+1}}{\frac{C_{j}}{\Delta t}v_{j}^{n} - \sum_{k=1,k\neq j}^{M_{j}}I_{jk}^{n+1} + H_{j}^{n+1}}{\frac{C_{j}}{\Delta t} + G_{i}} + E_{ij}^{n+1}}_{R_{ij} + \frac{L_{ij}}{\Delta t} + \frac{C_{i}}{\Delta t} + G_{i}}^{-1} + (\frac{C_{j}}{\Delta t} + G_{j})^{-1}}$$
(2.8)

So, the Voltage-in-current formulation has been stated as a successful improved formula because it is numerically stable. The graph below show the results obtained.



Figure 2.5 Result obtained from basic LIM and improved LIM [5]

CHAPTER 3

METHODOLOGY OF RESEARCH

3.1 Introduction

In this chapter, the methods of conducting this research will be discussed. The overall flow chart of the research will be discussed. The research stars with PDN modelling and will be end with PDN simulation result analyses. Then flow chart of voltage in current formula execution will discussed. Requirements and design of the research also will be discussed in this chapter. Finally, it send with the summary of the project.

3.2 Flow Chart



Figure 3.1 Flowchart of the project

The first stage for this research is the designing the PDN model. This PDN model was done by triangular mesh method. The capacitor and inductor values will be calculated by using equation 2.1 and 2.2. The following parameters were used.

| Parameters | Value |
|-------------------------|------------------------|
| Dielectric thickness, h | 0.245×10 ⁻² |
| Permittivity, ε | 4.70 |
| Permeability, µ | 1 |

Table 3.1 Parameters involved in capacitor and inductor calculation

The built model will be simulated using Ltspice, LIM formula and voltage in current LIM formula. the output results will be compared and analysed. The result from LIM formulas will verified using the Ltspice output result. The comparison between different time steps will be done for LIM out and voltage in current LIM.



Figure 3.2 Flow chart for voltage in current LIM formula

Flow chart explains how does the voltage in current LIM working. First of all, the loop will update the branch. When it comes to the second branch it will check the availability of t+1 value. If there is no availability of t+1 value, it will use the t value to update the following branch. Then it will update the node.

3.3 Project requirements

Since this is a software oriented project, so there won't be any hardware involved in this project. Software that will be used in this project is SPICE and MATLAB. SPICE will be used to simulate the built model. MATLAB will be the main software in this project. LIM formula will be implemented in MATLAB coding. The codes will be built is such way so that it can solve the circuit by using the LIM formula. The simulated result will be recorded. Lastly, the SPICE and MATLAB results will compared and analysed in Chapter 4.

3.4 Project design

The project over flow has been shown in Figure 3.1. It starts by building the PDN model. After further studies, triangular mesh will be used in building the PDN model. The capacitor and inductance value will be set in codes. The built model will be reviewed and checked whether it follows the specification of the method. If it follows the specification, then LIM formula will be applied on the built model. While if it does not meet the requirements, the model will build again by adjusting the limitation. Basic formula of LIM will be applied to the built model and it will be simulated. The result will be analysed whether it is numerically stable or not. If it does not achieve numerically stability, the LIM formula will be altered and the updated new formula will be used to

simulate the built model. The flow will continue until an updated LIM formula that gives numerical stability to the result. If the simulated result is numerical stable, then it will be analysed. The simulated result will be analysed along with the result from the simulation of built model by LtSPICE. The simulation time and some other characteristics will be analysed.

3.5 Chapter Summary

Flow chart given in Section 3.2 will be the fundamental key concept in the execution of the project. Basic LIM will be used at first. Then it will be updated until the numerical stability of the result gained. In this project, the result from MATLAB and LtSPICE will be compared and analysed. The analyzation will be done in Chapter4.

CHAPTER 4

RESULTS AND DISCUSSIONS

4.1 Introduction

This chapter will discuss on the results that have been obtained from the circuit modelling part and the simulations of the circuit with LtSPICE, basic LIM formula and also the Voltage in Current LIM formula. Firstly, the circuit modelling which was done by using triangular mesh method will be discussed. Then the output graph obtained from simulation of the modelled circuit will be analysed.

4.2 PDN Modelling

4.2.1 PDN Modelling for 10 nodes

Modelling of PDN networks were done by using triangular mesh method. For this research Voronoi diagram was plotted using MATLAB software. Figure 4.1 show the Voronoi diagram obtained for 10 nodes of PDN.



Figure 4.1 Voronoi diagram for 10 nodes

From Figure 4.1, the red dots are representing the nodes of the circuit. The blue polygons behind the dots are representing the Voronoi diagram. Further MATLAB coding script were added in the previous code to get a Delaunay Triangulation. Figure 4.2 shows the Delaunay Triangulation for the 10 nodes of PDN.



Figure 4.2 Delaunay triangulation for 10 nodes

From the Figure 4.2 each red line is representing the branch. The total number of branches for 10 nodes are 19. From the LIM theory, each branch and node will consist inductor and capacitor respectively. The value of capacitor and inductors were calculated using equation 2.1 and 2.2. The calculated values for voronoi diagram areas, length of vornoi edge and the length triangle edge also shown in the tables below.

| Node | Area of the vornoi diagram behind the node (m^2) | |
|-----------------|--|--|
| N ₁ | 0.5×10^{-5} | |
| N ₂ | 0.5×10^{-5} | |
| N ₃ | 0.5×10^{-5} | |
| N_4 | 0.5×10^{-5} | |
| N_5 | 1×10^{-4} | |
| N ₆ | 1×10^{-4} | |
| N ₇ | 0.5×10^{-5} | |
| N ₈ | 0.5×10^{-5} | |
| N ₉ | 0.5×10^{-5} | |
| N ₁₀ | 0.5×10^{-5} | |

Table 4.1 Calculated areas of the voronoi diagram

Table 4.2 calculated value of length of voronoi edge

| Branch number | Length of Voronoi edge (m) |
|------------------|----------------------------|
| Nr.1 | 1.12×10 ⁻² |
| N ₅₂ | 1.12×10 ⁻² |
| N ₅₄ | 1.00×10^{-2} |
| N ₅₆ | 1.00×10^{-2} |
| N ₅₈ | 1.12×10^{-2} |
| N ₅₉ | 1.12×10^{-2} |
| N ₆₃ | 1.12×10^{-2} |
| N ₆₇ | 1.00×10^{-2} |
| N ₆₉ | 1.12×10^{-2} |
| N ₆₁₀ | 1.12×10^{-2} |
| N ₆₂ | 1.12×10^{-2} |
| N ₇₃ | 1.12×10^{-2} |
| N ₇₁₀ | 1.12×10^{-2} |
| N ₄₁ | 1.12×10^{-2} |
| N_{48} | 1.12×10^{-2} |
| N ₁₂ | 1.00×10^{-2} |
| N ₂₃ | 1.00×10^{-2} |
| N ₈₉ | 1.00×10^{-2} |
| N ₉₁₀ | 1.00×10^{-2} |

| Branch number | Length of the edge of the triangular mesh(m) |
|------------------|--|
| N ₅₁ | 0.55×10^{-2} |
| N ₅₂ | 0.55×10^{-2} |
| N ₅₄ | 0.76×10^{-2} |
| N ₅₆ | 0.76×10^{-2} |
| N ₅₈ | 0.55×10^{-2} |
| N ₅₉ | 0.55×10^{-2} |
| N ₆₃ | 0.55×10^{-2} |
| N ₆₇ | 0.76×10^{-2} |
| N ₆₉ | 0.55×10^{-2} |
| N ₆₁₀ | 0.55×10^{-2} |
| N ₆₂ | 0.55×10^{-2} |
| N ₇₃ | 0.55×10^{-2} |
| N ₇₁₀ | 0.55×10^{-2} |
| N ₄₁ | 0.55×10^{-2} |
| N_{48} | 0.55×10^{-2} |
| N ₁₂ | 0.38×10^{-2} |
| N ₂₃ | 0.38×10^{-2} |
| N ₈₉ | 0.38×10^{-2} |
| N ₉₁₀ | 0.38×10^{-2} |

Table 4.3 Calculated value of length of triangular mesh