LOW POWER DESIGN TECHNIQUES FOR ANALOG CIRCUIT

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LIST OF ABBREVIATIONS

ABBREVIATIONS	DESCRIPTION
ADC	Analog to digital memory
CAD	Computer aided design
CMOS	Complementary metal oxide semiconductor
DC	Direct current
DTTS	Dual threshold transistor stacking
FPGA	Field programmable gate array
GND	Ground
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
MTCMOS	Multi-threshold CMOS
NMOS	N channel MOSFET
PMOS	P channel MOSFET
RC	Resistance capacitance
SCCMOS	Super cut-off CMOS
TPD	Total propagation delay
TPH	Rising time difference of the output and input
TPL	Falling time difference of the output and input

LIST OF SYMBOLS

SYMBOL	DESCRIBTION
V_{BS}	Bulk source voltage
V_D	Drain voltage
V_{DD}	Drain supply
V_{DS}	Drain Source voltage
V_G	Gate voltage
V_{GS}	Gate source voltage
V_{IH}	Input upper limit
V_{IL}	Input low limit
V_N	Inverting input
V_{OH}	Output upper limit
V_{OL}	Output lower limit
V_{OS}	Offset voltage
V_{OUT}	Output voltage
V_P	Non-inverting input
V_{SS}	Source voltage
V_{TN}	NMOS threshold voltage
V_{TP}	PMOS threshold voltage
V_{BN}	NMOS bulk biasing
V_{BP}	PMOS bulk biasing

REKABENTUK TEKNIK KUASA RENDAH BAGI LITAR ANALOG

ABSTRAK

Pembanding adalah litar analog yang membandingkan dua insyarat analog dan menghasilkan keluaran digital daripada perbandingan tersebut Permanding berkuasa rendah dan berkelajuan tinggi amat penting bagi memepercepatkan pertukaran data analog kepada data digital dalam masa yg sama beroperasi dalam kuasa yang rendah. Pengunaan litar kusa rendah amat menjadi perhatian bagi alat-alat elektronik lebih-lebih lagi alat elektronik yang menggunakan bateri untuk beroperasi. Jadi, permintaan alat elektronik berkuasa rendah semakin menjadi sambutan tanpa menjejaskan pretasinya. Dalam kajian ini pembanding konvensional, pembanding dengan MTSCStack & DTTS, pembanding dengan bulk-driven telah direka dan disimulasi dengan mengunakan perisian Silterra cadence teknologi 0.13 µm process CMOS. Matlamat kajian ini adalah untuk mencari dan membina dengan mengambungkan teknik-teknik tersebut bagi menghasilkan pembanding beroperasi dalam kuasa yang rendah tanpa menjejaskan prestasi sedia ada. Teknik MTSCStack mengurangkan arus bocor dalam mod aktif dan mengekalkan logik asal. Manakala DTTS mengurangkan arus bocor tanpa menjejaskan prestasi litar tersebut dan teknik bulk-driven, keperluan V_{TH} dikeluarkan daripada laluan isyarat apabila insyarat input dijadikan pada bulk. Di bawah keadaan ini, kejatuhan voltan yang lebih rendah diperlukan seluruh input and keluaran terminal pemacu. Pembanding dicadang menunjukkan keputusan 13.6 mV bagi mengimbangi, 25.8 mV bagi resolusi, 19.3 gandaan voltan, 3.46 ns bagi perambatan lengah, 7.71 µW bagi kuasa statik dan 16.44 µW bagi kuasa dinamik.

LOW POWER DESIGN TECHNIQUES FOR ANALOG CIRCUIT

ABSTRACT

Analog comparator is a circuit that compares two analog signal and produce a digital output from the comparison. Low power consumption and high speed comparator is very important to exchange the analog signal to digital signal at the same time can operate in low power. Use of low power circuit is such a demand for electronic devices even more for electronic devices use batteries to operate. So, designing of low power consumption and high speed comparator become an attention without affecting the performance. In this study, the conventional comparator, comparator with MTSCStack & DTTS, and comparator with bulk-driven has been designed and simulated using Silterra Cadence technology software using 0.13 µm CMOS process. The aim of this study is to find and build the combination of these techniques to produce a comparator that can operate in low power without compromising existing performance. The function of MTSCStack technique is to reduce leakage current in active mode and at the same time retain the original state. While, DTTS is reduce leakage current without affecting the performance of the circuit and bulk-driven technique is be able to remove the need of V_{TH} from the signal path when the input signal is applied to bulk. Under this condition, the voltage drop across is required across input and output terminals of the drive. Proposed comparator shows result of 13.6mV for offset, 25.8mV for resolution, 19.3 for voltage gain, 3.46ns for propagation delay, 7.71µW for static power and 16.44 µW for dynamic power.

CHAPTER 1

INTRODUCTION

1.1 Background

Portability becomes the main point in every electronic equipment that requires battery life to operate like laptop, mobile phone, mp3 device and others. For now, all those devices can operate only in short time using the battery. Although the improvement of battery has been made for the lithium battery but there is no dramatic improvement in lithium battery life. There is only 30% improvement in battery performance can be achieved in next 5 years of research. Since there is no drastic improvement in that battery life performance, other alternative ways have to be make in order to increase the lifespan of portable devices that are using batteries[1].

The main reason why the portable devices using the battery have a shorter time of standby mode is because of the power consumption of the circuit. In integrated circuit, there are two types of power consumption which are the static power and dynamic power. Static power is the leakage current of the transistor when the transistor is in the inactive state. The leakage current happens due to low threshold voltage when V_{TH} of the transistor. This is because of the non-scalable thermal voltage characteristic (V_T = kT/q), which cause relatively fixed sub-threshold at the constant temperature [2].

Dynamic power happens when in the integrating circuit the transistor keeps charging and discharging at the load in order to transmit information. Continuous of charging and

discharging contribute to the switched power dissipation. In order to reduce the total power dissipation, same of the techniques have to be applied to the integrated circuit. Some possible techniques are Multi-Threshold Supercut Stack (MTSCStack) with Dual threshold Transistor Supercut of Stack (DTTS) and bulk-driven.

1.2 Problem Statement

All electronic devices need some amount of power in order to work properly without having any problem. There are lots of techniques and research have been conducted to reduce the power consumption in electronic circuits. However, many of these researches are concentrate on the digital circuits. The reason behind this is because in the analog circuits are much more complex and complicated. Analog-to-Digital Converter (ADC) is the most rapid growing building block for the analog circuit and the most important component in ADC is comparator [3]. Since all electronic devices become faster in processing, so ADC technology itself have to catch up. Since that, power consumption is becomes the main issue because in order to get a faster ADC high V_{DD} have to be used. High power consumption in analog circuit leads to increase the cost packaging and cooling in order to minimize the heat dissipation.

Therefore, we have to find the techniques that can reduce the power dissipation of the analog circuit without affecting the performance of ADC such as speed, time delay, operational frequency and resolution.

1.3 Objective of Research

1. To conduct a study on the existing conventional comparator circuit and digital low power techniques.

2. To design a low power comparator circuit using low power reduction technique.

3. To analyze the performance of the comparator based on the combination of low power techniques.

1.4 Scope of Project

This project is conducted to analyze the best power reduction technique that is going to be applied to the conventional comparator circuit. The result and performance for each technique will be compared to one to another. The comparison is based on the time delay and power dissipation for each power reduction techniques that apply on conventional comparator circuit. The simulation of this project was performed using Silterra's Cadence software. The design was implemented in 0.13 µm CMOS process technology.

1.5 Thesis Overview

This thesis consists of 5 chapters, like the list chapter in the introduction, followed by literature review, methodology, result and discussion and finally the conclusion.

Chapter 1 is on the introduction of this research. It describes the background study, problem statement, objectives of this research and the scope of the project.

Chapter 2 will discuss on the literature review on the researches that are related to this work. Advantage and drawbacks of each power reduction technique are also discussed in this chapter. In additions, types and characteristics of comparator and bulk driven technique are included.

Chapter 3 is focusing on the methodology of this project. This chapter includes the schematic of the conventional comparator and the proposed comparator with more detailed explanation on the circuit operation.

Chapter 4 is representation of the result. Cadence software is used to run the pre-layout simulation of the conventional comparator, comparator with MTSCStack & DTTS, comparator with bulk-driven and proposed comparator. The result of the simulation is observe and be compare based on time delay and power consumption, offset, resolution and voltage gain.

Chapter 5 is about the conclusion of this project. At the end of this project, the best technique is identify based on the performance of the comparator. Other than that, any further improvement is discussed in order to improve the overall performance of the comparator with the power reduction technique.

CHAPTER 2

LITERATURE REVIEW

This chapter discusses on the low power design techniques in integrated circuit. Power dissipation is categorized under 2 types, dynamic power and static power. The various low power consumption techniques discussed in this chapter to be implement in the comparator circuit. Review on the performance of each low power consumption technique is given to understand the comparator circuit limitation and performance.

2.0 Power consumption

Static power and dynamic power are the main components that lead to power dissipation in every digital and analog circuit. Since dynamic power is proportional to the square of the supply voltage, $V_{DD,}$ and static power is proportional to V_{DD} lowering the V_{DD} is the most effective way to reduce the power consumption. By scaling down the supply voltage V_{DD}, threshold voltage, V_{TH} should also be scaled in order to meet the performance requirement. Unfortunately, such scaling leads to an increase in leakage current which becomes the utmost concern in designing low-voltage high-performing circuit [4]

2.1.1 Static Power

Static power dissipation occurs when there is a leakage current in the transistor when it is in idle mode, short circuit and bias pn junction.

2.1.2 Leakage Current

The leakage current in transistor happens due to low threshold voltage V_{TH}. From equation 2.1, the leakage current is the combination of sub-threshold and gate-oxide leakage [5];

$$I_{leak} = I_{sub} + I_{ox} \quad (2.1)$$

From the equation above, sub-threshold current I_{sub} happens when the gate to source voltage, V_{GS} is more than the inversion point but still below the threshold voltage, V_{TH}. The sub-threshold region is so important in the analog circuit because the circuit will operate in low power mode. So, only small voltage is required for biasing. Sub-threshold leakage is the major contributor to the static power in the analog circuit. Sub-threshold current is shown in equation below 2.2.

$$I_{sub} = K\left(\frac{W}{L}\right) e^{(VGS-VTH)} \left(1 - e^{-\frac{VDS}{VT}}\right) \quad (2.2)$$

Where, K is Boltzmann's constant (1.38 x 10^{-23} J/K), n is the technology parameter, W/L is width and length, V_{TH} is threshold voltage, V_{DS} is drain-source voltage, and V_{GS} is gate-source voltage. From equation (2.2), increase the leakage sub-threshold current will increase with reduction of V_{TH}. Equation below (2.3) shows the oxide current;

$$I_{ox} = KW\left(\frac{V}{T_{OX}}\right)^2 e^{-\alpha T_{OX}/V} \quad (2.3)$$

Where, K is Boltzmann's constant (1.38 x 10^{-23} J/K), W is the gate width, T_{ox} is thickness oxide and V is the voltage. The term that is important in the equation (2.3) is the oxide thickness, T_{ox}. From the equation above, if the oxide thickness is increase the gate leakage current will be reduced however, this will consequently decrease the transistor effectiveness because oxide thickness must decrease proportionally with the process scaling to avoid the short channel effect. Therefore, increasing oxide thickness is not an option and therefore, thickness of oxide is under the control of the and not the circuit design [6].

2.1.2 Reverse biased pn-junction current.

Reverse Biased PN-junction leakage occurs when an active transistor charges up and down the drain while the other transistor is off. The leakage occurs between the diffused region and substrate with respect to the former's bulk potential is active and another is off in an inverter. Therefore, leakage current existence when the transistor is in idle state since the diode is reverse-biased. Equation 2.4 expressed the reverse biased PN-junction leakage current.

$$I_D = I_s(e^{\frac{qv}{KT}} - 1) \qquad (2.4)$$

Where, I_S is reverse saturation current, V is diode voltage, K is Boltzmann's constant (1.38 x 10^{-23} J/K), q is Electronic charge and T is temperature.

2.2 Dynamic Power

Dynamic power dissipation could be categorized into 2 classes which are, capacitance and short circuit power. Capacitance is leads to dynamic power dissipation during the charging and discharging of the parasitic load capacitances. While short circuit power is due to conducting path between NMOS and PMOS transistor. It happens when the NMOS and PMOS are in active mode at a time which leads direct current between supply voltage to the ground and due to the presence of unwanted signal which is called glitch that generates from the transition [7].

2.2.1 Dynamic Capacitance power

Charging and discharging of capacitance is required to change the transistor state from ON to OFF. Continuously charging and discharging of the load capacitance is important in order to transmit information in the circuit. This occurrence contributes to the switched power dissipation. The equation below 2.5 below shows the overall distribution in dynamic capacitance power dissipation.

$$P_{dynamic} = F_{switching} V_{DD} V_{swing} C_L \qquad (2.5)$$

Where, $F_{switching}$ is switching activity of the logic gates, V_{DD} is supply voltage, V_{esting} is voltage swing, C_L is Load capacitance. The switching power is usually the dominant term as shown in equation 2.6 below.

$$P_{switching} = \alpha C_L V_{DD}^2 f_{CLK} \quad (2.6)$$

Where, α is the activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, and f_{CLK} is the clock frequency. Clearly from the equation (2.6), the way to reduce the power charge and discharge load capacitance, is by reducing the supply voltage however it will affect the performance of the circuit unless the V_{TH} is scale down as well so that gate drive,$(V_{GS} - V_{TH})$ remain large enough. Since the propagation delay in a CMOS gate can be approximated by;

$$T_{pd} \; \alpha \; \frac{C_L V_{DD}}{(V_{DD} - V_{TH})\alpha} \quad (2.7)$$

Where α is for modeling short channel effect. Based on equation (2.7), by reducing the supply voltage, the switching power is reduced but scaling down the threshold voltage causes rapid increase in sub-threshold leakage current. As the power supply and threshold voltage continuously scales down, the increased leakage power can dominate the dynamic switching power [8].

2.2.2 Dynamic short-circuit power

There will be a small period of time when both the NMOS and PMOS transistors are in ON mode during the switching period. Since both the NMOS and PMOS transistors are in the ON mode, it will lead to the direct current path from the supply voltage and the ground. As a result, the short circuit current will flow for a short period of time which leads to power dissipation. Equation 2.8 showed the short-circuit power dissipation;

$$P_{sc} = t_{sc} V_{DD} I_{peak} F \quad (2.8)$$

Where, P_{sc} is the short circuit power t_{sc} is slope of the input signal, V_{DD} is supply voltage, I_{peak} is short-circuit current, and F is frequency.

2.3 Power Reduction Technique

From year to year, there are tons of improvement have done in CMOS technology. Same goes with the power reduction techniques, for decades there are many techniques that have been developed to reduce the power dissipation in digital circuit such as Body-biasing, Super Cut Off CMOS (SCCMOS), Multi-Threshold CMOS (MTCMOS), Stack transistor, Sleepy keeper technique, or combination of some techniques and the Bulk-driven technique. All these techniques will be discussed in detail in this thesis and they were also implemented in comparator analog circuit in this project.

2.3.1 Dynamic Voltage and Frequency Scaling and Body Biasing

Body biasing is implemented in the IC design circuit which can minimize the standby leakage power dissipation. This technique is important in the mobile phone technology since the mobile phones most of the time are in idle mode. The optimum point occurs as the leakage of the sub-threshold current is reduced, however at the expense of an increase in the junction band-to-band leakage current component across the junction. As the increase of the junction band-to-band tunneling leakage current, so new junction engineering technique should be

invented to find the solution to overcome the junction band-to-band tunneling leakage current to ensure the effectiveness of reverse body biasing. In biasing, the bulk of NMOS is connected to the ground while the bulk of PMOS is connected to the supply voltage, V_{DD}. This ideal schematic of PMOS and NMOS are shown in figure 2.1.

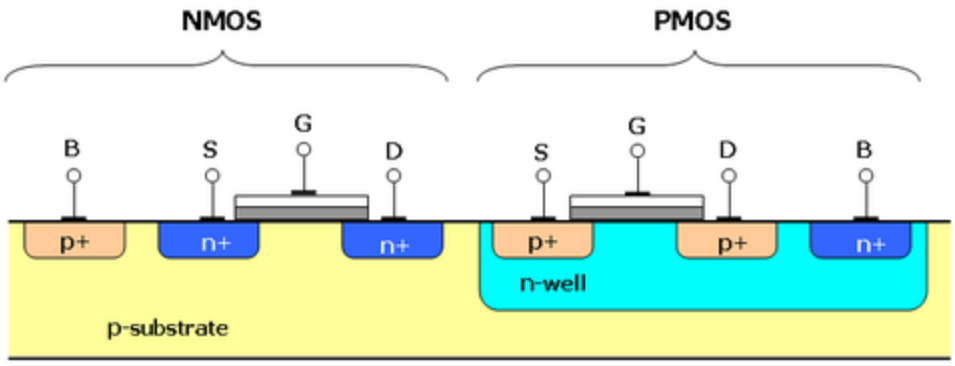

Figure 2.1: NMOS and PMOS transistor.

The leakage current occurs because of the increasing in sub-threshold current leakage. The sub-threshold current leakage happens since the supply voltage is scaled down along with the threshold voltage. The standby leakage power consumption (P_{SB}) of the chip with the reverse body biased is applied to both NMOS and PMOS transistor devices consist of two component, firstly is the leakage current I_{DD} in the power supply voltage and the leakage current I_{BP} and I_{BN} through the NMOS and PMOS body pins, as shown in equation 2.9 below;

$$P_{SB} = V_{DD} I_{DD} + (V_{DD} + V_{BS}) I_{BP} + V_{bs} I_{BN} \qquad (2.9)$$

The leakage current, I_{DD} is the component of the sub-threshold leakage current and source/drain-to-body junction leakage current. Only junction leakage current contributes to the I_{BP} and I_{BN}. As the V_{BS} increases, the leakage current I_{DD} firstly will be reduced and become saturates as the sub-threshold leakage current falls below the junction leakage. At, the same time, I_{BP} and I_{BN} increase because of both surface and bulk band-to-band junction

leakage tunneling increase strongly with larger reverse body bias. Therefore, there is an optimum reverse body bias characteristic of the technology which minimizes the standby leakage current [9].

2.3.2 Stack Transistor Technique

Stacking transistor technique can reduce the leakage current in the integrated circuit when more than one transistor in the stack is turned off together. This technique is done by splitting the transistor and stacking one or more of the transistor to the half width of the total transistor and connecting the stacking transistor in series[10][11].

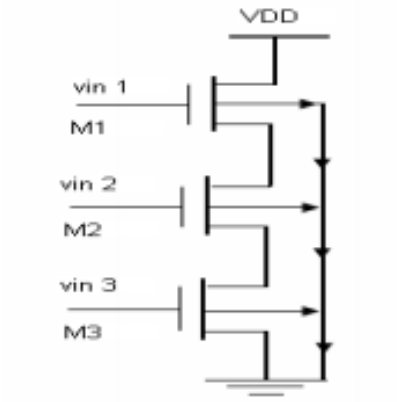

Figure 2.2: Transistor stacking technique

Figure 2.2 shows the stack transistor where three NMOS transistor is stacked. The leakage current can be reduced due to negative V_{GS} because of the positive potential on the central node of the stacked transistor [11]. This technique however reduces the drive current which increase the delay since the number of transistors is double compare to the original transistor,

2.3.3 Sleepy Keeper Approach.

Sleepy keeper is another reduction power technique. The purpose of this technique is to reduce the leakage current using the leakage feedback technique. In the sleep keeper approach, both additional sleep PMOS transistor is placed between the supply voltage and the pull-up network and an additional sleep NMOS transistor is placed between the pull-down network and ground. The circuit is turn off when the sleep transistor cuts off the power rails. Figure 2.3 shows the structure. Once the circuit is in the active mode, the sleep transistor will be turned on and then turn off as the circuit is in the idle mode. Since the power source is cut off, this can reduce the leakage power effectively. However, the technique leads to the destruction of state and a floating output voltage because output will be floating after the sleep mode [12].

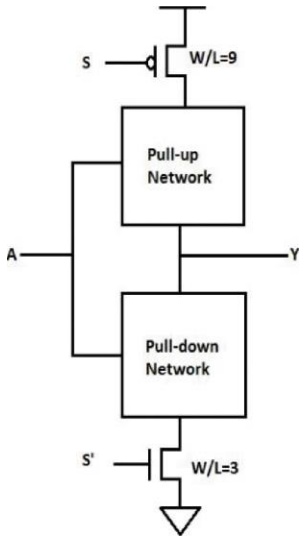

Figure 2.3: Structure of Sleepy Keeper Technique.

2.3.4 Sleepy Stack Transistor Technique

Structure of sleepy stack transistor technique is the solution for static power consumption problem. This technique has the combination advantage of two different circuit techniques, the sleep transistor technique and the stack transistor technique. This circuit has a merit whereby the transistor technique can retain the original state unlike the sleep transistor. Moreover it can utilize the high V_{TH} to achieve up to two orders of magnitude of leakage power reduction unlike the stacking technique. However, the design sleepy stack transistor technique has a trade-off in terms of larger area and delay in return to the ultra-low leakage power consumption. The stack inverter breaks existing transistor into two transistors with half the size of the width of the original transistor and forces a stack structure to take advantage of the stack effect as shown in figure (2.4).

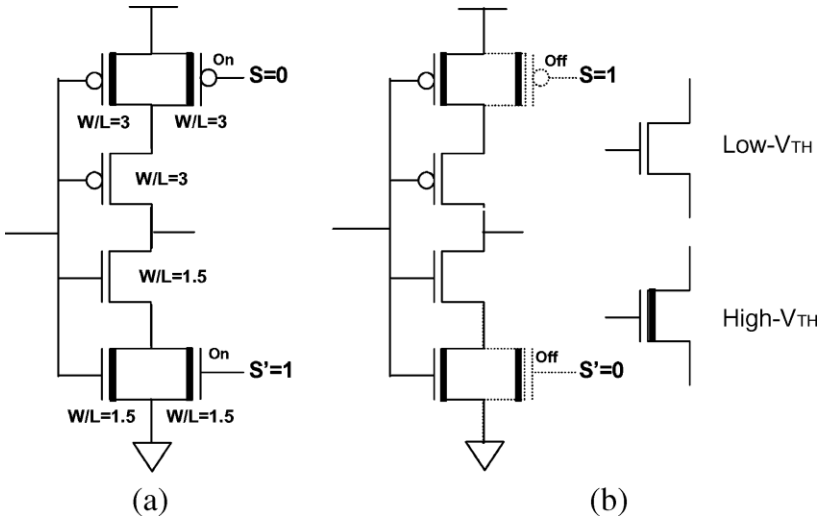

Figure 2.4: (a) Sleepy stack inverter in active mode. (b) Sleep mode

Figure 2.4 shows that the sleep inverter isolates existing logic network using sleep transistors. From the previous discussion, the stack structure can save leakage power consumption during sleep mode. The bulk-sleep transistor is biased with high voltage to achieve the higher V_{TH} in order to get the larger leakage power reduction. The sleep transistors are added in parallel to one of the transistors in each set of two stacked transistors.

There are two operations in the sleepy stack technique which are the active mode and sleepy mode. The sleepy stack technique operation is similar to the sleep transistor when the transistors are turned on during active mode and the transistors are turned off during sleep mode. Based on the figure 2.4, during the active mode; S=0 and S'=1 are asserted, and all transistors are turned on. There are two ways how the sleepy stack technique can reduce circuit delay, firstly all transistors able to achieve faster switching time compared to stack the structure because all transistors are always on during the active mode.

Specifically, the voltage at the source of sleep transistor is always ready at the connected sleep transistor drain so that, the current is able to flow immediately to the threshold voltage transistor connected to the gate output. Meanwhile during sleep mode, as shown figure 2.4; S=1 and S'=0 are asserted and both sleep transistors are turned off. Although, the sleep transistors are turned off the sleepy stack structure can maintain the exact logic state. The reduction of leakage current is achieved by two ways which; firstly high V_{TH} is applied in the sleep transistor and the transistors that are parallel to the sleep transistors. Secondly, stacked and turned off transistor induce the stack effect which reduces the leakage power consumption. Therefore, by combining both structures, the sleepy stack technique is able to

achieve ultra-low leakage power consumption during sleep mode while maintaining the exact logic state [13].

2.3.5 Multi Threshold CMOS technique (MTCMOS)

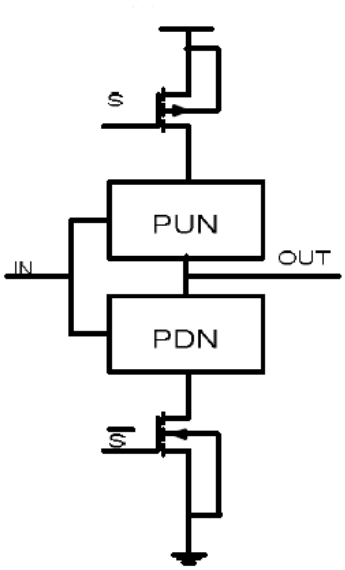

Figure 2.5: Multi Threshold CMOS Structure. [14]

Figure 2.5 shows the structure of multi-threshold CMOS technique (MTCMOS). This technique is able to control the leakage current in combinational logic effectively. Even so, there is a slight drawback with this technique when the output will be floating after the sleep mode [14]. The MTCMOS technique consists of inserting an additional PMOS sleep transistor in series between the pull-up network and supply and one additional NMOS transistor between pull-down network and ground.

During the active mode, sleep transistors with high V_{th} are turned on and sleep bar transistors are turned off. The low V_{th} transistor in pull-up transistors and pull-down transistors will operate normally during the active mode. While in idle mode, the sleep transistors are turned off and the sleep bar transistor become on. From this technique, the leakage current reduction can be achieved by cutting off the power source through high V_{th} transistor. As discussed before, with the high V_{th}, current leakage can be reduce during idle mode so power consumption also can be reduce [15].

2.3.6 Super Cut-Off CMOS (SCCMOS)

Super Cut-off CMOS (SCCMOS) is another reduction technique to reduce power consumption in the circuit. In the SCCMOS technique, the voltage supply is removed when it is in the idle mode. Instead of using V_{TH} for sleep transistor like in the MTCMOS technique, super cut-off technique uses low V_{TH} with inserted gate bias generator. The structure of SCCMOS technique is shown in figure 2.6.

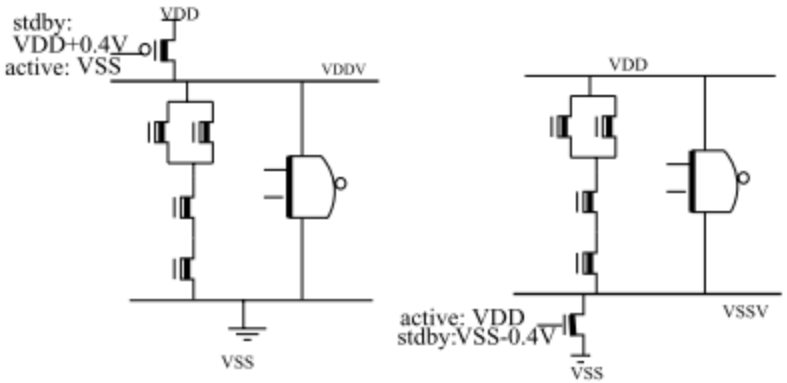

Figure 2.6: (a) SCCMOS structures with pmos transistor and (b) with nmos transistor. [15]

During the active mode, for the pmos transistor the gate is applied to 0V and the virtual supply voltage V_{DDV} line is connected to the supply voltage V_{DD}. Meanwhile, for the idle mode, the gate is applied with V_{DD}+0.4V in order to cut off the leakage current. Different for nmos transistor, during the active mode the gate is applied to V_{DD} and the virtual voltage V_{SSV} line is connected to V_{SS}. Then during the idle mode, the gate is applied V_{SS}-0.4V in order to cut off the leakage current [15][16].

2.3.7 Dual Threshold Transistor Stacking Technique (DTTS).

Dual threshold transistor stacking technique is the combination of multi threshold cmos technique (MTCMOS) and stacking technique. As a result, DTTS technique has advantage of power reduction during both idle and active modes. A higher V_{TH} is assigned to some transistors in noncritical transistor paths so as to reduce leakage current. Since the assign of higher V_{TH} is only to noncritical path, the performance id maintained due to the low V_{TH} transistors in the critical paths. Therefore, no additional transistors are required and both high performance and low power can be achieved simultaneously. Figure 2.3.7(a) shows signal path of the circuit in DTTS [16].

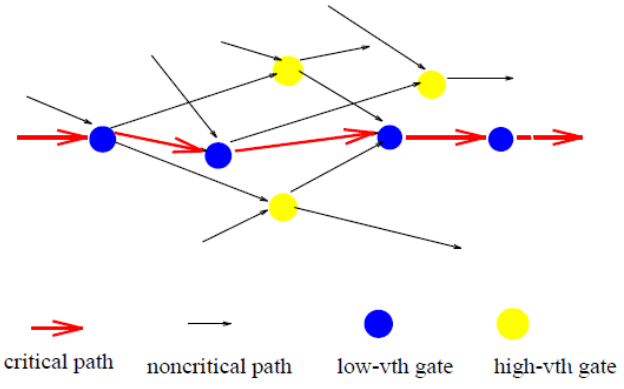

Figure 2.7: Signal path in DTTS CMOS circuit. [16]

2.3.8 Multi Threshold Supercut of Stack Technique (MTSCStack).

MTSCStack technique is the combination of three power reduction. The combination consist of Multi-Threshold CMOS (MTCMOS), Supercut CMOS (SCCMOS) and Stacking transistors techniques. Therefore, MTSCStack technique is able to reduce power consumption during active mode at the same time can retain the exact logic state unlike MTCMOS and SCCMOS technique and unlike stacking technique, MTSCStack is able to save power consumption during idle mode. Figure 2.8 shows the structure of MTSCStack technique.

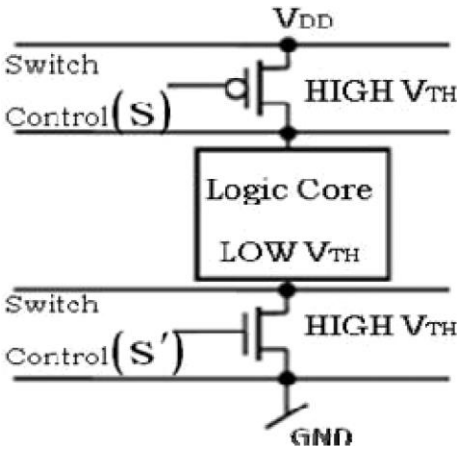

Figure 2.8: Schematic diagram of MTSCStack. [17]

Sleep transistor on the MTSCStack structure works the same way as the MTCMOS when the sleep transistor is on during active mode and the sleep transistor is off during idle mode [17]. During active mode, switch control signal S=0 and S'=1 are inserted, so all sleep transistors and transistors parallel with sleep transistors are turned on. The delay can be reduced in this structure and stack transistors structure able the leakage current to be reduced. Then for the

sleep mode, S=1 S'=0 are inserted, thus all sleep transistors will be off. In order to maintain the value of '1' in idle mode, nmos transistor in parallel to the pmos sleep transistor is the only source of V_{DD} to the pull-up network. As well as to maintain the value of '0', pmos transistor parallel with the nmos sleep transistor is the only source of ground to the pull-down network[17].

2.3.9 Bulk-Driven Technique.

Bulk-driven technique only can be applied to the MOSFET that can be fabricated in its own separate well. A cross section of a p-type MOSFET in an n-well. The operation of the bulk-driven MOSFET id much like a JFET. The inversion layer shaping the conduction channel beneath the gate is established by intertwining the gate terminal to a fixed voltage of sufficient magnitude to form a channel. The conduction channel of the JFET is the MOSFETs inversion layer under the gate structure. The thickness of the depletion layer beneath the source, inversion layer, and drain of the MOSFET is determined by the bulk potential. By varying the bulk-source voltage, this depletion layer thickness changed, and the inversion layer through which the drain current is flowing is modulated. This channel current can be modulated with very small dc values of the bulk-source potential resulting in a device that is extremely useful for low voltage application.

In the Bulk-Driven technique, the signal is applied at bulk-drain instead of gate-drain connection. Since the signal is applied to the bulk-driven, requirement of V_{TH} is removed from the signal path. Under this circumstance, a lower voltage drop is required across input

and output terminals of the drive. With the fixed voltage at the gate terminal ensures the dependency of the MOSFET current on the bulk-driven voltage based on the equation 2.9;

$$I_D(sat) = \frac{\beta}{2}(V_{GS} - V_{TH0} - \gamma\sqrt{|2\Phi_F| - V_{BS}} + \gamma\sqrt{|2\Phi_F|})^2, V_{DS} > V_{GS} - V_{TH} \qquad (2.9)$$

Where $\beta = \mu C_{ox} W/L$, μ is the mobility of the carriers, C_{ox} is the gate oxide capacitance per unit area, W/L is aspect ratio of MOSFET, ϕ_F is the absolute fermi potential, V_{T0} is zero bias threshold voltage and γ is the body-effect coefficient.

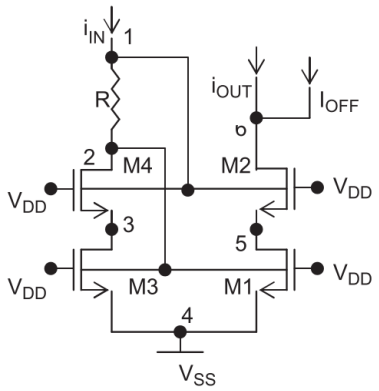

Figure 2.9: Bulk-Driven design structure. [18]

Figure 2.9 shows the design structure of the bulk-driven technique. By using equation (2.9), the current across the MOSFET can be determined. Precaution must be taken that the value of V_{BS} is such that bulk-source junction either reverse biased or slightly forward biased with V_{BS} less than V_{TH} to ensure the negligible bulk current in the circuit. Constant bulk source is applied to get the operation current mirror of the bulk-driven circuit, M1 and M3 MOSFETs and the same being copied to MOSFET M2 and M4, respectively. The bulk-driven technique

operates as soon as the supply is switched on due to channel formation, MOSFETs behave like junction field effect transistor. Unlike the conventional gate-driven technique, the input signal in the bulk-driven technique is applied to the bulk terminal $V_{IN}=V_{BS}$ rather than the gate terminal [18].

2.4 Comparator

Comparators are used in the Analog-to-Digital converter (ADC) for the data transmission application, switching power regulators and many other application. The binary output of the comparator is produced by comparing the voltage that appears at the input with reference voltage at comparator. The comparator is the critical component in analog-to-digital (ADC) converter. Using smaller supply voltage in the design of comparators is a great challenge especially in maintaining high-speed. The main reason for reducing smaller voltage supply in comparator is to reduce the power consumption. To attain high speed, transistor with increased width and length values are required to compensate the reduction of supply voltage, which means increasing chip area and power. Figure 2.10 shows the symbol of comparator also known as amplifier because comparator and amplifier share many similar characteristic. Comparator tends to operate in open-loop configuration without the negative feedback. The gain of the comparator circuit is usually high and the slew rate and propagation delay are designed at their minimum [19].

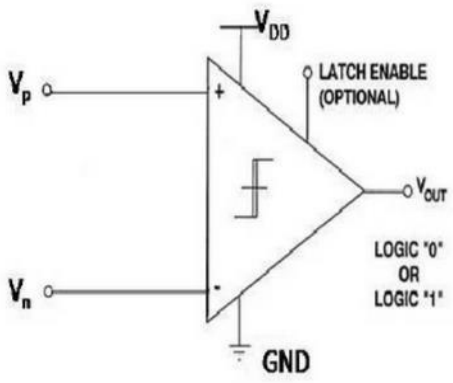

Figure 2.10: Voltage Comparator.

Figure 2.11 show the ideal curve of a comparator where V_{OH} is the upper limit output voltage, V_{OL} is the lower limit output voltage, V_{OUT} is the output voltage, and V_{IN}-V_{REF} is the different between the non-inverting input voltage and inverting input voltage which produce either high or low output. The comparator produced high output voltage when there is positive difference between the V_{IN} and V_{REF} and low output voltage is produced when there is negative difference between the V_{IN} and V_{REF} [19].

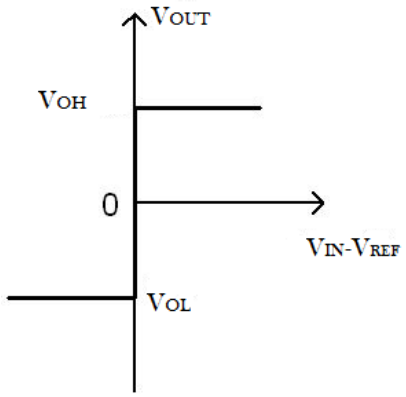

Figure 2.11: Comparator Ideal Transfer Curve

Usually, the ideal transfer curve of the comparator as shown figure 2.11 is not realizable in real life comparator. Figure 2.12 shows the non-ideal transfer curve for the comparator. The figure shows the input voltage difference V_{IH} and V_{IL} and V_{IN}-V_{REF} at upper and lower limit respectively. The resolution of the comparator is known as the input voltage difference of the comparator. The output of the comparator is change when the input voltage is zero in ideal comparator. But the output of the comparator may change at non-zero input voltage difference because of the manufacturing effects like transistor mismatch [19].

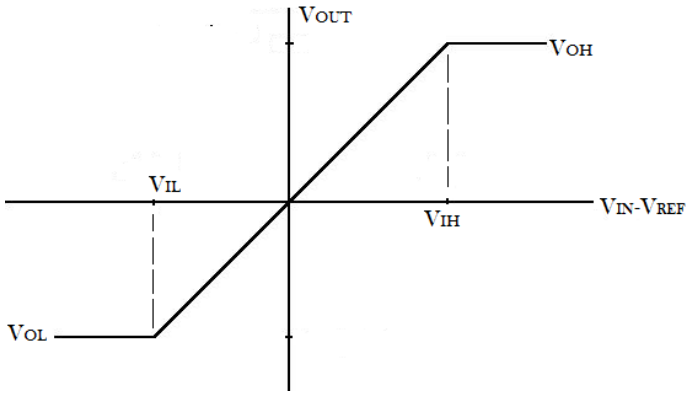

Figure 2.12: Comparator Non-Ideal Transfer Curve

The figure 2.13 shows the offset voltage of a comparator circuit. From the figure, the output of the comparator is unchanged until there is a positive difference (different between V_{IN} and V_{REF}) and negative different (different between V_{IN} and V_{REF}). The offset voltage, V_{OS} is known as the input voltage at which its output changes from one logic level to the other [19].