EFFECTIVE RESISTIVITY ANALYSIS USING CPW TRANSMISSION LINE MODEL FOR Au-COMPENSATED HIGH RESISTIVITY SILICON SUBSTRATE

WONG SOO THENG

UNIVERSITI SAINS MALAYSIA

2017

EFFECTIVE RESISTIVITY ANALYSIS USING CPW TRANSMISSION LINE MODEL FOR Au-COMPENSATED HIGH RESISTIVITY SILICON SUBSTRATE

by

WONG SOO THENG

Thesis submitted in partial fulfillment of the
requirements for the degree of
Bachelor of Engineering (Electronic Engineering)

JUNE 2017

ACKNOWLEDGEMENT

I would like to genuinely show my appreciation towards School of Electrical and Electronics, Universiti Sains Malaysia for giving such a wonderful opportunity for me to implement all my knowledge into the undergraduate project and let me gain new and valuable skills in the field of Analog and Radio Frequency.

This would not make possible without the help and support from many people who had given me their earnest assistance in accomplishing this project. Firstly, I would like to dedicate my deepest gratitude to my project supervisor and advisor, Dr. Nur Zatil 'Ismah Hashim, for providing me ultimate guidance and important information throughout the undergraduate project. I am very grateful for her constant supervision as well as her support in completing this project.

Secondly, I would like to thank my FYP examiner, Dr. Mohamed Fauzi Packeer Mohamed, for giving me great guidance and wonderful suggestions for my project. It is such an honor to have this opportunity to learn from him.

Thirdly, my appreciation goes to my fellow friends, Mr Tan Jia Yiing and Mr Yap Chee Seong for their valuable suggestion, ideas, knowledge, support and friendship. Without their guidance and expertise in Analog and RF, I would not able to complete my project with ease.

Finally, I would like to take this advantage to thanks my parents and family members for giving me encouragement and moral support even if they are miles away. With their love and support, I am able to face all the challenges to complete my project.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS AND ABBREVIATION

Al-Si	Aluminium compensated silicon substrate
Ar	Argon
Au	Gold
Au-Si	Gold compensated silicon substrate
CMOS	Complementary metal-oxide semiconductor
Cz-Si	Czochralski-silicon
dB	Decibel
DC	Direct current
D_{it}	Density of traps
E-beam	Electron beam processing
Fz-Si	Float-zone Silicon
GaAs	Gallium Arsenide
HWCVD	Hot-wire chemical vapor deposition
Hz	Hertz
LPCVD	Low pressure chemical vapor deposition
MIM	Metal insulator metal
PSC	Parasitic surface conduction
ppma	parts per million atoms
Q_{ox}	Fixed oxide charges
RF	Radio frequency
t_{ox}	Thickness of oxide
V	Voltage
V_a	Bias voltage
ρ_{eff}	Effective resistivity

ANALISASI KERINTANGAN EFEKTIF MENGGUNAKAN MODEL GARISAN TRANSMISI CPW UNTUK Au-KOMPENSASI SILIKON KERINTANGAN TINGGI

ABSTRAK

Pembangunan komunikasi tanpa wayar yang pesat telah menjurus kepada keperluan peranti elektronik yang pantas. CMOS integrasi kini menghadapi masalah kehilangan tenaga yang tinggi dan faktor ini boleh disingkirkan dengan menggunakan substrat silikon kerintangan tinggi. Namun begitu, kelemahan penggunaan substrat silikon kerintangan tinggi adalah kewujudan caj-caj pembawa bebas di ruang antara oksida dan silikon yang berpunca daripada konduksi permukaan parasit. Walaupun pengedopan kompensasi aras mendalam menggunakan emas berpotensi untuk menindas konduksi permukaan parasit dan membekal kerintangan yang tinggi kepada substrat silikon, namun begitu, tiada bukti yang pejal untuk menyokong kaedah ini. Dengan demikian, matlamat bagi projek ini adalah untuk mengkuantitikan potensi Au-kompensasi silikon kerintangan tinggi dalam menindas konduksi permukaan parasit. Kehilangan atenuasi garisan transmisi CPW atas substrat perlu diukur terlebih dahulu dengan menggunakan parameter S yang telah diekstrak. Kaedah angka merit pencirian kerintangan efektif digunakan untuk menganalisis dan mengkuantitikan kebolehan substrat. Hasil daripada analisis matematik telah membuktikan potensi Au-kompensasi silikon kerintangan tinggi dalam menindas konduksi permukaan parasit kerana ia menunjukan pincang yang tidak bersandar ketika voltan pincang digunakan ke atas peranti tersebut.

EFFECTIVE RESISTIVITY ANALYSIS USING CPW TRANSMISSION LINE MODEL FOR Au-COMPENSATED HIGH RESISTIVITY SILICON

ABSTRACT

The rapid development of wireless communication has led to the need for high-speed electronic device. The current integrated complementary metal oxide semiconductor (CMOS) suffer from high energy losses and this factor can be eliminated using high resistivity silicon substrate. However, the drawback of using high resistivity silicon substrate is the presence of free carrier charges at oxide-silicon interface due to the parasitic surface conduction. Though deep level doping compensation using gold has shown a potential of suppressing the parasitic surface conduction effect and providing a high resistivity to the silicon substrate, there are no solid evidence to support this method. Thus, the goal of this project is to quantify the potential of Au-compensated high resistivity silicon substrate in suppressing the parasitic surface conduction. The attenuation losses of the Coplanar Waveguide Transmission Line on the substrate is firstly measured using the extracted S-parameter data. The figure of merit technique using effective resistivity characterisation is then used to analyse and quantify the capability of the substrate. The outcomes of the numerical analysis had shown a constant value of effective resistivity for Au-compensated high resistivity silicon substrate thus justifying the potential of Au-compensated high resistivity silicon substrate in suppressing the parasitic surface conduction as it shows bias-independent results when bias voltage is applied to the device.

CHAPTER 1

INTRODUCTION

1.1 Research Background

The development of wireless communication has changed the way people live. Undoubtedly wireless technology had an enormous impact towards technology development by improving communication in many ways. As the growth of wireless communication industry gradually increase over the past decade, the demand for higher efficiency and more convenient wireless technology has also increase hastily. Thus, leading to the need for high speed electronic device which boosted the development of monolithic microwave integrated circuit in the industry.

The main problem suffered by present day integrated CMOS in high frequency circuit is having a low-quality factor which caused energy loss and increasing in the noise figures of the device. Therefore, having a high resistivity substrate is crucial to eliminate the factors affecting the loss. Amongst the many commercialised substrate[1-3], silicon remains as the favourite[4, 5]. However, high resistivity silicon suffers from a phenomenon known as parasitic surface conduction (PSC) [6-9]. This effect is bias dependent, and is caused by the formation of charge carriers, via accumulation or inversion at oxide-silicon interface, creating a low resistivity region on the silicon surface. This low resistivity region translates into an increased in substrate loss in the microwave range application, defying the initially high resistivity nature of the bulk silicon substrate.

To suppress parasitic surface conduction, high density of traps are introduced at the surface of the silicon substrate [6, 10]. Consequently, the free carriers will be trapped, or

positioned far away from the oxide-silicon interface, preventing their formations and maintaining the high resistivity nature of the bulk substrate. Several methods have been proposed to suppress the effect such as deposition of addition layer [11-16] and amorphisation of the silicon surface using ion implantation [17-19]. In addition to this proposed solutions, deep level doping compensation also shows a potential in suppressing the effect [20]. Coplanar waveguide fabricated on high resistivity silicon substrates created through deep level doping compensation using gold has shown bias independent attenuation loss throughout the whole range of voltage measured where accumulation and inversion are said to occur [20]. This indicates potential of parasitic surface conduction suppression.

1.2 Problem Statement

The drawback of using high resistivity silicon substrate in monolithic microwave integrated circuit is the formation of free carrier charge due to the parasitic surface conduction at oxide-silicon interface. As mention previously, the deep level doping compensation using gold has shown a potential of providing high resistivity substrate and high volume of density of traps at the silicon surface to reduce the interface loss [20]. However, currently there is not any strong evident to support this method. Thus, it is essential to quantify the potentiality of Au-compensated high resistivity silicon substrate in suppressing the parasitic surface conduction. Since most of the characterization and comparison results obtained by the previous work [10, 12-14, 19] are significantly differ from one another, hence, for this project, a figure of merit known as effective resistivity is used to characterise and compare the effect of high resistivity silicon substrate [21]. The effect of fixed oxide charges, density of traps at the oxide-silicon interface, oxide thickness and line geometry are all quantified and discussed. The effective

resistivity of the substrate is obtained through the aid of coplanar waveguide transmission line model for this project.

1.3 Objectives of Research

The aim of this project is to analyse the potential of Au-Compensated Silicon substrate in suppressing the parasitic surface conduction effect.

The objectives of this project are

i. To evaluate attenuation loss using Coplanar Waveguides Transmission Line Model.
ii. To characterise the effective resistivity of Au-Compensated High Resistivity Silicon substrate using evaluated losses.
iii. To study the potential suppression of parasitic surface conduction using the substrate through effective resistivity characterization.

1.4 Scope of Research

This research project is mainly focusing on numerical analysis and most of the analysis are software oriented. Analysis approach for this project is divided into two parts. The first part focused on the numerical analysis for the attenuation losses using Coplanar Waveguide transmission line model. For the second part of this project, it focus on the effective resistivity characterization based on the classification figure of merit method research conducted by *Lederer* [21]. His research focus on the factors affecting the performance of a coplanar structure on a silicon substrate. Data extracted in the first part would be used for the numerical and graphical analysis in this part. MATLAB® software is used for numerical and graphical

analysis in this project. MATLAB® software is a commercially-available user-friendly software that allows matrix manipulation, plotting of graph functions, implementation of algorithms and other numerical computing. It is developed by MathWorks and able to be executed in Microsoft Windows© operating system.

This project began with the research on the figure of merit technique called effective resistivity analysis introduced by *Lederer,* continue by the numerical analysis for the attenuation losses using CPW transmission line and followed by analysis of the effective resistivity of the silicon substrate using both numerical and graphical analysis.

1.5 Thesis Outline

This thesis consists of five main parts comprising of introduction, literature review methodology, results and discussion and finally conclusion which describe the project in detail. The first chapter is the introduction of this project which describes the framework of this project. It is followed by problem statement, research aim and objectives, project scope and ended with the thesis outline.

Chapter 2 provides the literature review of the research information. This chapter illustrates the knowledge and information from previous research from other researcher and other fundamental information that are relevant to this project. With this knowledge, it would support the fundamental concepts and theory used in this project. Most of the fundamental theories related to this project is explained in this chapter.

As for Chapter 3, the methodology on the effective resistivity analysis on the Au-Compensated Silicon substrate are explained. This includes the method of analysing the

attenuation loss of the Coplanar Waveguide transmission line as well as the effective resistivity of the substrate using MATLAB® software.

Chapter 4 present the results and discussion of this project. This chapter discusses the overall outcome from the numerical analysis. The results for the CPW losses and the effective resistivity with be displayed through graphs, followed by the analysis of results. Comparison of performance between Float-zone silicon substrate and Au-compensated high resistivity silicon substrate have been made and discussed in this chapter.

Last but not least, Chapter 5 concluded the overall project. Summary of the research and the restatement of the results of the project are included. The recommendation for the future works will also be presented in this chapter to improve the overall of the project.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

Before implementing the analysis techniques proposed in this project, a comprehensive research need to be conducted for better perception. Thus, this chapter illustrates the summaries and reviews on the fundamental background and some past works that are relevant to the project research. The research areas studied include high resistivity silicon substrate in monolithic microwave integrated circuit (MMIC) and radio frequency (RF) application, parasitic surface conduction effect in bulk high resistivity silicon substrate, and Au-compensated high resistivity silicon substrate. In section 2.2, the basic idea of high resistivity silicon substrate in microwave application are discussed and investigated. As for section 2.3, the parasitic surface conduction is introduced and its effect towards MMIC is reviewed. This is followed by the fundamental concept of Au-compensated high resistivity silicon substrate in section 2.4. In section 2.5, the characterisation method using effective resistivity is introduced and discussed. Finally, this chapter end with the summary of the studies conducted in the last section.

2.2 High Resistivity Silicon substrate in RF Application.

The current integrated CMOS circuits for the use at high frequencies with active and passive components suffered from the deprivation of having low-quality factor. This low-quality factor would have influenced the generation of eddy current and undesirable capacitive coupling which would result in increase of noise figures [22]. One of the solution in

overcoming these problem is by using a semiconductor which has a specific resistivity as the substrate. One of the researcher proposed the usage of high resistivity substrate as the solution to suppress the substrate noise while increasing the quality factor of the passive components [23]. He states that the increasing in the substrate resistivity will not have any impact on the isolation and this can minimise the parasitic capacitance. He implemented 0.1 μm gate length RF CMOS on high resistivity substrates and this results in the improvement of capacitor performance and noise isolation. Graph below shows the effect of the resistivity of the substrate towards the quality factor of the capacitor. The quality factor increases as the substrate resistivity increase.

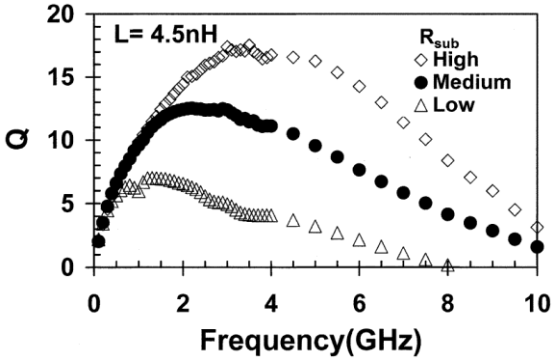


Figure 0.1: Graph function of quality factor versus frequency of 2.0pF MIM capacitor. The substrate with the highest resistivity has the highest quality factor in this graph. [23]

2.2.1 Silicon as Microwave Substrate

One of the problem in developing high frequency communication equipment is high cost material. Most of the material that provide great microwave performance are often expensive. Silicon is known to have numerous advantages as a system substrate material such as low production cost and mature technology. In one of the previous research, the loss of CPW transmission lines realized on silicon substrates are compared to loss obtained from CPW

realized on GaAs substrates [7]. The result shows that silicon with resistivity higher than 2000 Ω-cm produce losses comparable to GaAs with insulators. This proved that silicon substrate with high resistivity are capable to be used as microwave substrate. After an interval of two years, the same researcher had demonstrated that silicon substrate measured with resistivity in between 3 kΩ-cm to 7 kΩ-cm is able to produce CPW transmission line losses and quality-factor which are comparable with GaAs on a similar structure[24]. This result proves the feasibility and practical applicability of the usage of silicon as a microwave substrate. The use of CPW structure is one of the effective ways to reduce the loss of passive circuits on low resistivity silicon substrate. While the use of high resistivity silicon substrate has proven to effectively reduce the loss of on-chip passive circuits [4].

The two most common method used to produce monocrystalline silicon is Float zone (Fz-Si) and Czochralski (Cz-Si) crystal pulling process. The Czochralski technique [25] is a method of pulling a monocrystalline with the same crystallographic orientation of a small monocrystalline seed crystal out of melted silicon.

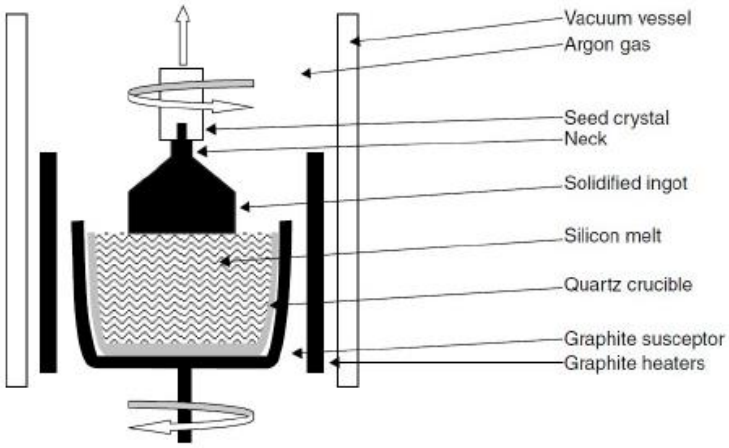


Figure 0.2: Czochralski silicon process.[25]

One of the disadvantages of this technique is the presence of parasitic carriers in the produced silicon ingots which arised from the unavoidable contamination during the Czochralski process [25]. The source of contaminations comes from the silica crucible that holds the melt. During high temperature treatment, the crucible dissolved slightly and releases 5 to 20 parts per millions atoms (ppma) of oxygen which then form silicon monoxide [26]. This problem can be solved by using the Float-zone method for silicon growing. Float-zone method is based on zone-melting principle of high purity crystal growth process. The process take place under vacuum or in an inert gaseous atmosphere.

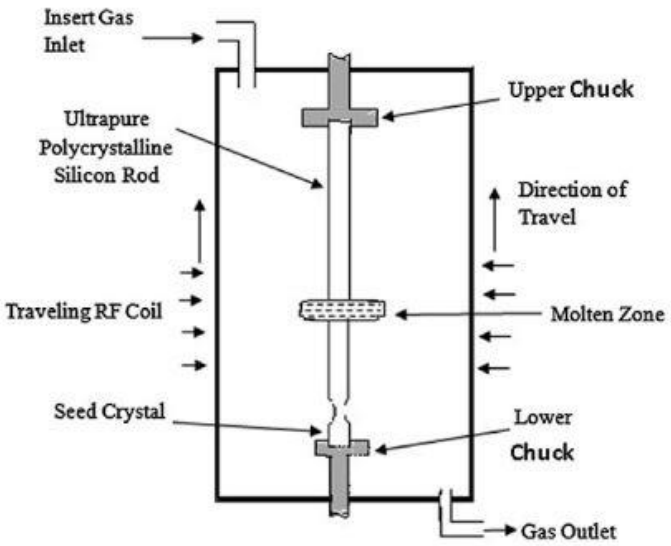


Figure 0.3: Arrangement of a typical float zone system. [27]

The Float-zone process shown in Figure 2.3 uses a rod of ultrapure polycrystalline silicon. The rod is statically maintained in vertical direction using two chunks and is confined in a chamber with inert atmosphere maintained by a flow of argon. An RF heater coil is then circled around the chamber. The single-crystal seed is clamped at the lower end where it

rotates around the axis during the growth process. The absence of a crucible in the Float-zone process eliminated the contamination from the walls of crucible in Czochralski process.

2.3 Parasitic Surface Conduction (PSC) in bulk High Resistivity Silicon substrate

As mention previously, to prevent leakage of energy in microwave devices, the resistivity of the bulk substrate need to be high. Two main factors affecting the resistivity of the silicon substrate are the resistivity of the bulk substrate itself and the parasitic surface conduction effect. Parasitic surface conduction which is also known as the oxide-silicon layer interface was first defined by *Reyes et al*. [7] where a sudden drop of resistivity in the silicon substrate was reported in his work for CPW transmission line realized on silicon substrates [7]. From the research he has conducted where CPW is realised on silicon substrates with oxides as the insulator, the effect distinctly shows that there is an increase in the attenuation losses. The effect of PSC is also investigated and the result shows that when the oxide layer is introduced, a strong inversion or accumulation layer of charges is formed at the surface of the silicon substrates [8]. Thus, leading to the increase of the attenuation loss.

2.3.1 An Introduction to Parasitic Surface Conduction

Usage of CPW structure on the silicon substrate had improved its potential to reduce the losses as the direct contact between the metal conductor layer with the high resistivity silicon substrate was reported having low microwave losses. However, this solution did not prevent the DC current from leaking into the substrate. To solve this problem, a layer of oxide was introduced between the metal layer of CPW and the high resistivity silicon substrate. In the research conducted by *Wu et al*. [9], it was demonstrated that there are about 10^{11} cm^{-2} positive oxide charges in the region of the oxide-silicon interface with zero biased voltage

condition [9]. The existence of the oxide layer induced the free carriers to the surface of the silicon substrate. This results in a region of low resistivity inversion layer on the surface as shown in Figure 2.4 below.

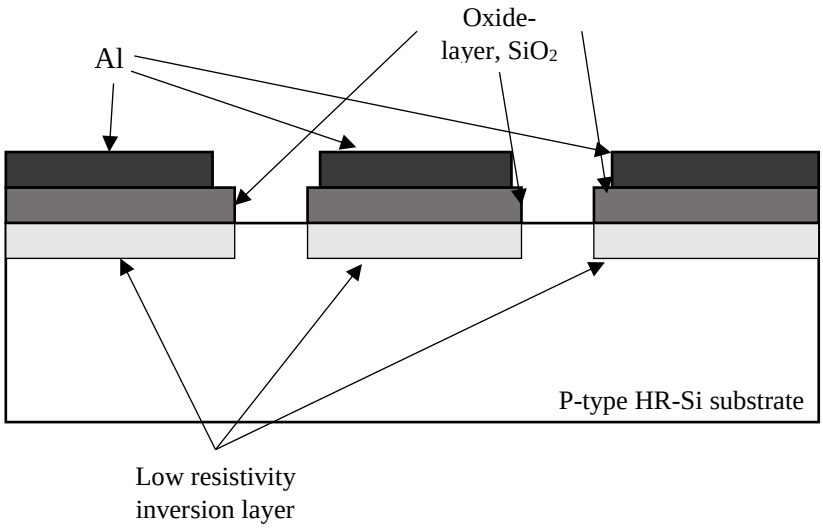


Figure 0.4: Formation of low resistivity region at the surface of the silicon substrate. [9]

On the other hand, the quality of the parasitic surface conduction (PSC) can firmly affect by the applied bias. It is clearly shown in a research, where the changes in the carrier static distribution at the surface of the substrate were observed and analysed. In their research, it shows that CPW attenuation losses were more affected by the existence of free carriers beneath the line metal. This reaction is mainly due to the localisation of electric field on the surface of the substrate in the CPW structures. This would then result in CPW attenuation losses that varied correspond to the applied DC bias. In one of their experiment on CPW losses with applied bias, about 20% increase of CPW losses using DC bias from 0 V to 3 V [6]. Hence, to solve these variations, the oxide-silicon interface is characterized by a high density of traps.

2.3.2 Method of suppressing Parasitic Surface Conduction Effect

Many research have been conducted to study and investigate the method in suppressing the PSC effect in the high resistivity silicon substrate. In one of the research, the author proposed a solution to solve the PSC problem by depositing a layer of low pressure chemical vapour deposition (LPCVD) polycrystalline silicon layer over the surface of a high resistivity silicon substrate as shown in Figure 2.5. In his research, he deposited a 0.6 μm layer of polycrystalline silicon at reduced pressure of 620 °C and covered by 0.1 μm silicon dioxide deposited by LPCVD at 720 °C. The thin surface layer of the LPCVD polycrystalline silicon acts as a stabilising layer that enables the surface of the substrate to be covered with an isolating layer to provide DC isolation while reduced the microwave transmission losses in the CPW structure. It also removes any dependency of CPW attenuation losses on DC bias level.

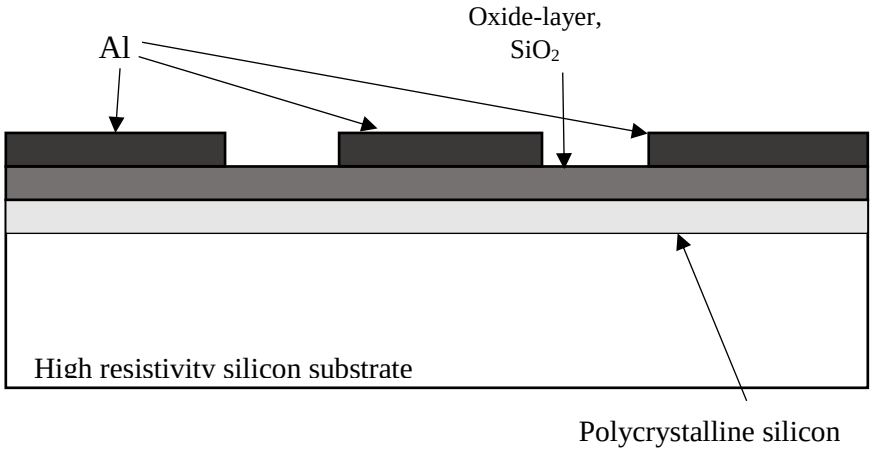


Figure 0.5: CPW structure on passivated polysilicon stabilized high resistivity substrate. [13]

On the other hand another researcher states that the use of 500nm layer of LPCVD polysilicon produces a large interface trap density which prevent the formation of free carrier

charges layer on the surface of the high resistivity silicon substrate [11]. A similar method is also proposed where he states that the thick polycrystalline silicon is used to as a trapping layer to trap the free carrier attracted to the oxide layer, thus reducing the attenuation loss. He integrated a 300 nm polysilicon layer under a 100 nm oxide layer to obtain an attenuation loss of 1.08 dB/cm at 30 GHz [14].

Depositing a thin layer of nanocrystalline silicon on the surface of the silicon substrate also have the same results in reducing the attenuation loss in the CPW structure. In the research by *Chen et al.* [12], he incorporated a 100 nm thick nanocrystalline silicon layer which is deposited by hot-wire chemical vapor (HWCVD) on the high resistivity silicon substrate. This method provided a surface passivation to the substrate and results in attenuation loss of 94.5 % lower than nonpassivated oxidized high resistivity silicon substrate at frequencies up to 20 GHz [12, 16]. This method was further justified in another research by another researcher which he demonstrated the effect of the thickness of the nanocrystalline silicon layer on the passivation effect of the silicon substrate. He was able to show that the thicker the nanocrystalline silicon layer, the better the passivation effect and the attenuation loss could be reduced to 0.69 dB/cm. In his research, he states that nanocrystalline silicon layer are able to provide good suppression effect of surface channels of high resistivity silicon substrate and thus decreasing the attenuation loss [16] .

Besides that, PSC effect can be suppressed by implantation of heavy ions to create traps at the oxide-silicon interface and reduced the free carrier charges. This method had proven to reduce the impact of accumulation charge towards the performance of the microwave applications. High dose of Argon implantation is used to produce a high-density trap region. It is produced through bombardment of Argon atoms into the silicon surface

which would form an amorphized layer in between the oxide and silicon substrate [18, 19]. The ions implantation reduced the effects of surface charges on high resistivity silicon substrates while maintaining its compatibility with the conventional silicon technology [17]. Graph of Attenuation Loss, α against Frequency, *f* is plotted based on the Table 2.1 in the Figure 2.6. Table 2.1 shows the summary of the method used to suppress the parasitic surface conduction effect from the previous work:

Table 0.1: Method of suppressing PSC and the result obtained by the previous work.

Reference	**Method of suppressing**	**Results (Attenuation loss)**
[13]	Deposition of LPCVD polycrystalline silicon layer	0.11 dB/mm at 30GHz
[14]	Deposition of thick polycrystalline on the silicon surface.	0.11 dB/mm at 30GHz
[17]	Ion implantation of marchand type baluns into the substrate	0.2 dB/mm up to 30GHz
[9]	Deposition of amorphous layer at the silicon surface	0.3 dB/mm at 30GHz
[19]	Deposition of this amorphous layer using Ar implantation technique.	0.15 dB/mm at 30GHz
[12]	Deposition of 100nm thick nanocrystalline silicon at the oxide-silicon interface.	0.11 dB/mm at 20GHZ
[20]	Using Au-compensated high resistivity silicon	0.2 dB/mm at 40GHz
[16]	Deposition of 400nm thick nanocrystalline silicon at the oxide-silicon interface.	0.07 dB/mm at 20GHz

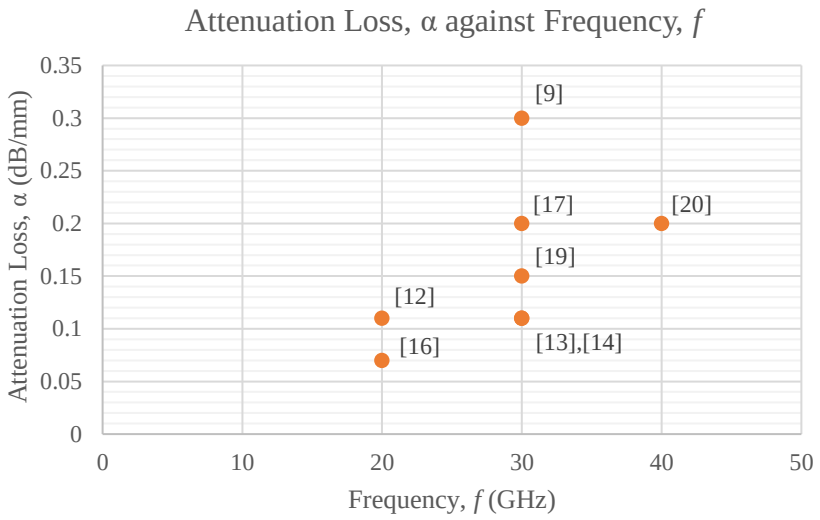


Figure 0.6: Attenuation Loss, α in unit dB/mm against Frequency, f in unit GHz.

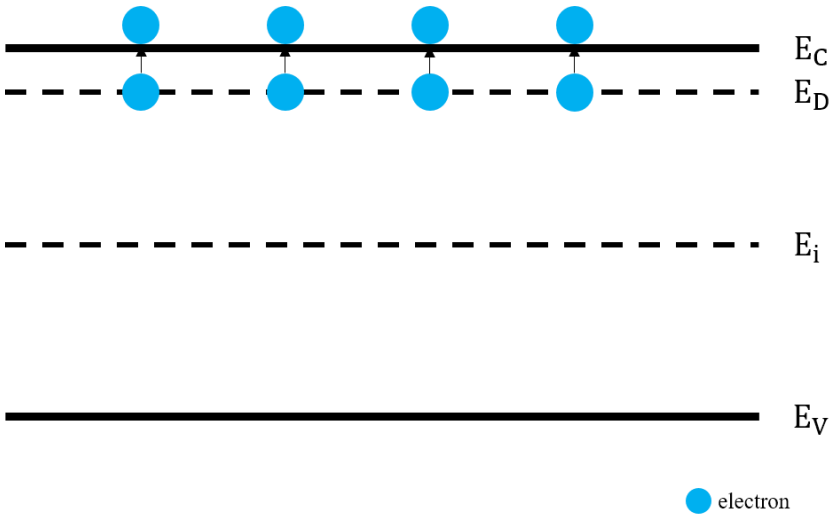
2.4 Au-Compensated High Resistivity Silicon

Deep-level doping compensation method is used to develop high resistivity silicon substrates for microwave applications. In this work, gold was used to compensate background carriers in low resistivity Czochralski silicon substrates through the creation of deep level traps and thus enhancing the resistivity of the substrates.

2.4.1 Deep level doping compensation of Au-compensated Silicon

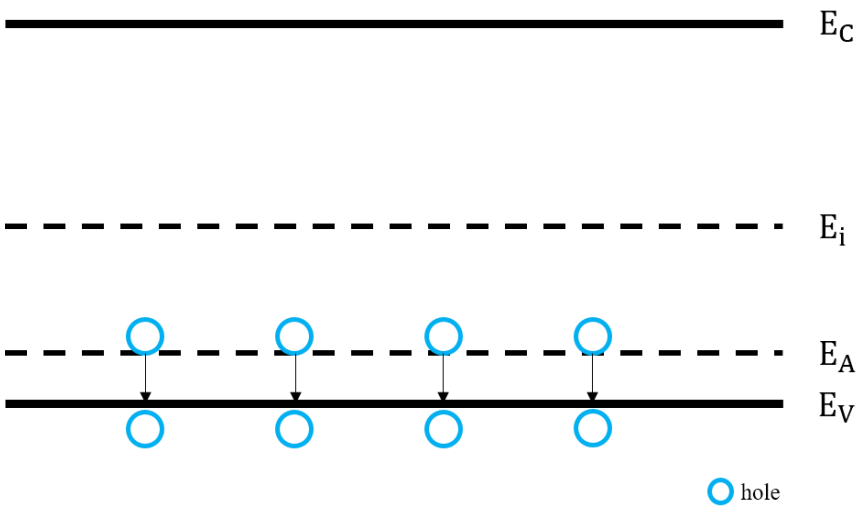
Ideally, intrinsic silicon contains no impurities and is insulating towards electrical field because of low number of electrons and holes in the silicon structure. However, in reality, it is unlikely to have pure silicon without any impurities as the possibility of contaminated environment during the growth of monocrystalline structure in silica crucible. As a result from the unwanted impurities, formation of free carrier charges occur in the silicon. There are two types of impurities which are shallow impurities and deep impurities. Shallow

impurities are correlated to the dopants from Group III or Group V elements where the dopants either become the acceptors of electrons or the donors of electrons during ionisation. During ionisation, shallows donors causes electrons to be promoted from donor levels, E_D to E_C, conduction band while shallow acceptors causes electron to be promoted from acceptor level, E_A to E_V, valence band as shown in Figure 2.7 below.



(a) N-type doping of shallow donors. [28]

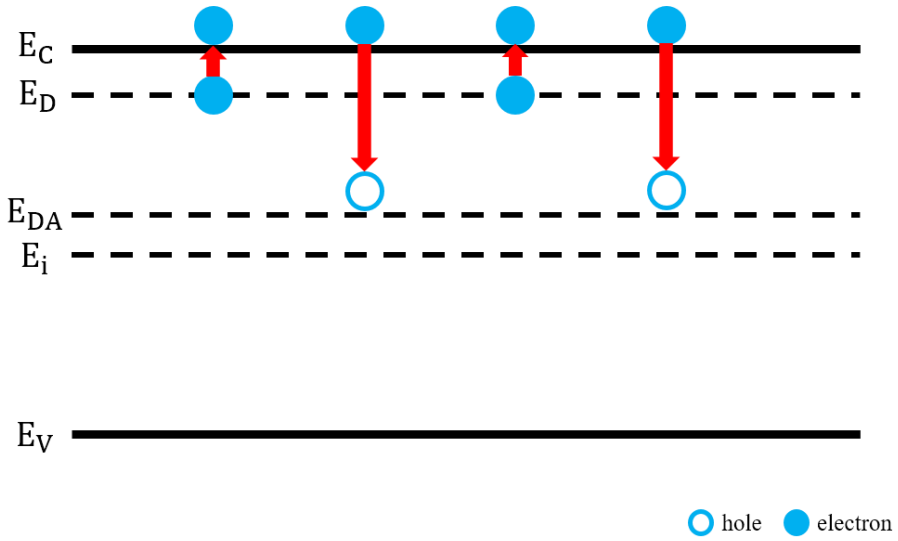
.



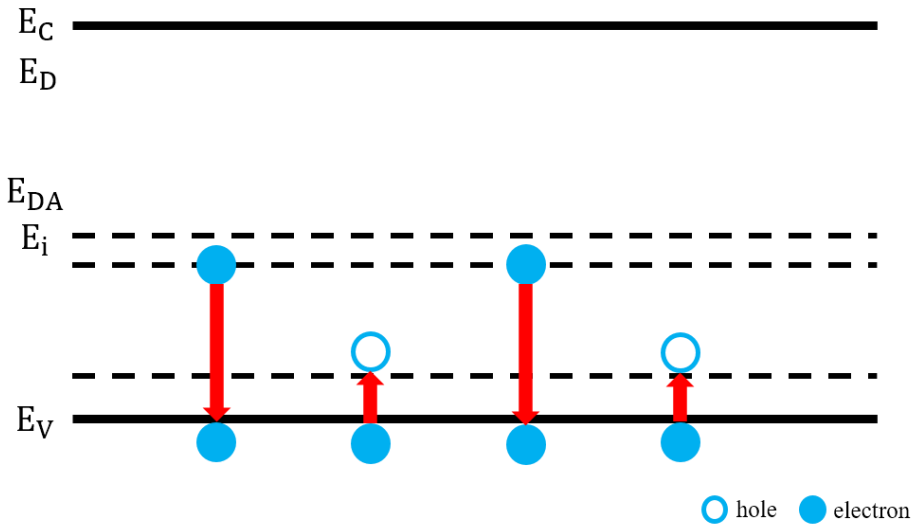
(b) P-type doping of shallow acceptors. [28]

Figure 0.7: Energy band diagram of silicon with dopant impurities.

When shallow donors and shallow acceptors co-exist inside the silicon, compensation doping occur. Compensation doping can occur in shallow impurities as well as in deep impurities where shallow donors are compensated by deep acceptors and shallow acceptors are compensated by deep donors. For shallow donors which are compensated with deep acceptor, the deep acceptors are negatively charged and attract the minority carrier holes to the E_{DA}- level. Then the electrons which were initially excited to the $E_{C,}$ fall to the holes. As for shallow acceptors which were compensated by deep donors, the positively charged deep donors attract and trap the minority carrier electrons into E_{DD}+ level, causing the trapped electrons to fall into the E_V and recombine with the holes which results in zero formation of free carrier charge as shown in Figure 2.8:



a) Shallow donors compensated by deep acceptors. [28]



b) Shallow acceptors compensated by deep donors. [28]

Figure 0.8: Compensation doping process between shallow impurities and deep impurities.

Reduction in formation of free carrier charges in silicon using the deep level doping compensation has become new development in producing high resistivity Czochralski silicon. In this project, gold is selected to be the deep element apart from other elements due to its minimal overcompensation effect and less need for tight control over dopant concentration. Au-doping was also proven to be capable of increasing the resistivity of silicon in [29, 30]. Some researchers had managed to produce gold-doped silicon wafer with resistivity of 180 kΩ-cm through deposition using E-beam or thermal evaporation and high temperature annealing indiffuse gold into the substrate [31]. This shows that Au is potential as deep level dopant as it provides a strong basis to produce high resistivity silicon for microwave application.

2.4.2 Suppression of PSC effect using Au-Si substrates

Deep level doping compensation is used to provide a high resistivity for the silicon substrate. By using Au-compensated silicon substrate, not only the background free carrier charges can be removed and thus increasing the resistivity of the substrate, deep level gold dopants are also capable of introducing high volume of trap densities that can suppressed bias dependant parasitic surface conduction effect which contributes to the attenuation losses of coplanar waveguide transmission. In the research conducted by *Hashim et al.*, the result shows that the attenuation loss for the devices on Au-compensated Cz-Si were lower compare to the value obtained from devices on Fz-Si at any given frequency [20]. In Figure 2.9, the attenuation of CPW on Au-compensated Cz-Si is 50% lower than Fz-Si is shown.

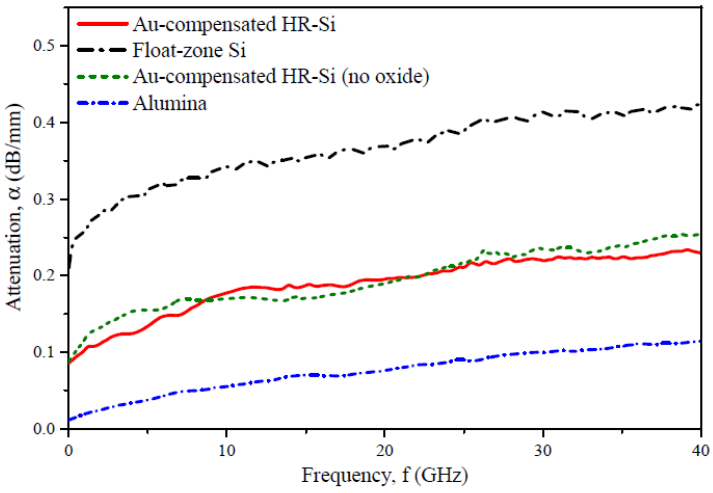


Figure 0.9: Frequency dependent attenuation loss for CPW transmission line. [20]

In the same work, bias-dependent measurements were conducted by back biasing the structure with constant DC voltage range of +6 V to -6 V and the result shows a constant attenuation of 0.2 dB/mm throughout the whole voltage range for CPW realized on Au-compensated Cz-Si at 40 GHz, as shown in Figure 2.10, eliminating the bias dependent oxide-silicon interface losses effect from parasitic surface conduction.

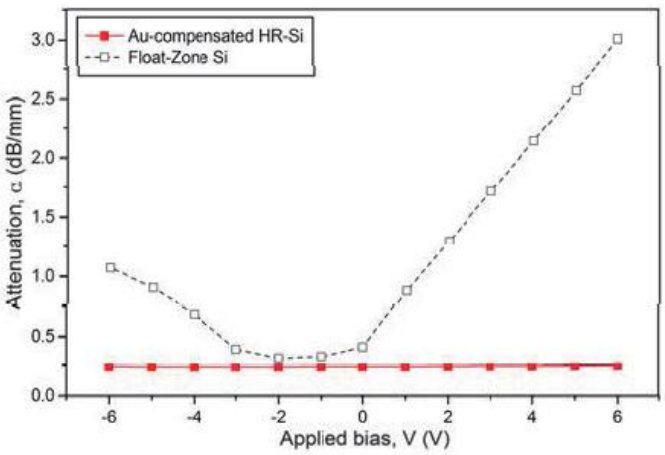


Figure 0.10: Bias-dependency of CPW attenuation loss on Au-compensated Si in comparison to Float-zone Si. [20]

2.5 Effective Resistivity Analysis

Effective resistivity (ρ_{eff}) characterization is a figure of merit technique introduced by *Lederer and Raskin* [21], which is used to characterize and analyse the substrate resistivity. Before the figure of merit technique of effective resistivity was introduced, there were few methods that were used to characterize the substrate resistivity such as insertion loss measurement method, attenuation loss measurement [32] and four-point probe measurement [33].

Effective resistivity characterization method was introduced due to the variation of depending factors in the attenuation loss which cannot be significantly represented by only the total radio frequency losses, which were reported in many mentioned works. These common methods only focused on measuring the bulk resistivity, but for effective resistivity characterization, it focused on analysing the surface resistivity as well. Effective resistivity (ρ_{eff}) analysis characterize the not only performance of the substrates, but the effect of bias (V_a), fixed oxide charges (Q_{ox}), density of traps at the oxide-silicon interface (D_{it}), oxide thickness (t_{ox}) and line geometry are all investigated [31]. Although this analysis is solely made in coplanar waveguides transmission line, however, this can be utilised in other coplanar devices.

The effective resistivity characterization method was derived from cross-sectional structure of CPW on inhomogeneous and homogeneous Si substrates analyzed in *Lederer and Raskin* work [21]. The cross-sectional structure of CPW on passivated silicon substrate and effective homogeneous substrate as shown on Figure 2.11 used for effective resistivity, ρ_{eff} modelling.

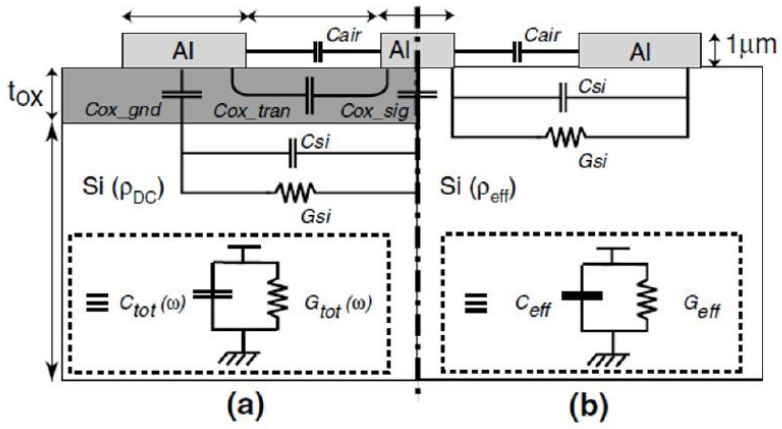


Figure 0.11: Cross-sectional CPW structure on (a) passivated inhomogeneous silicon substrate and (b) effective homogeneous substrate for effective resistivity modelling. [21]

Based on their work, to impartially and precisely studied the processed and biased silicon wafers, passivated and inhomogeneous silicon substrate is modelled with an effective homogeneous silicon substrate which had a uniform dielectric constant, $\epsilon_{r,Si}$ = 11.7 and uniform resistivity which are effective resistivity, ρ_{eff}. The RF losses for effective substrate need to be the same as the RF losses for inhomogeneous silicon substrate to produce the uniform effectivity resistivity, ρ_{eff} value. The effective resistivity for an inhomogeneous structure was derived based on the simplified model of the substrate shown in Figure 2.10. As mentioned previously, the RF losses for both substrate need to be identical, thus:

$$\alpha_{inh} = \alpha_{eff} \qquad (2.1)\ [21]$$

Since,

$$\propto_{inh} \approx \frac{G_{tot}}{2}\sqrt{\frac{L}{C_{tot}}}; \qquad \propto_{eff} \approx \frac{G_{eff}}{2}\sqrt{\frac{L}{C_{eff}}} \qquad (2.2)\ [21]$$

Assuming the lineic inductance (L) is same for both structures, and substituting Equation 2.2 into Equation 2.1, yields:

$$G_{eff} = G_{tot}\sqrt{\frac{C_{eff}}{C_{tot}}} \quad (2.3)\ [21]$$

where C_{eff} and G_{eff} are the parameter associated with the homogeneous structure, and given:

$$C_{eff} = \epsilon_{r,eff}C_0 = (1 + q(\epsilon_{r,Si} - 1))C_0 \quad (2.4)\ [21]$$

$$G_{eff} = q\frac{C_0}{\epsilon_0\rho_{eff}} = \left(\frac{\epsilon_{r,eff}-1}{\epsilon_{r,Si}-1}\right)\frac{C_0}{\epsilon_0\rho_{eff}} \quad (2.5)\ [21]$$

By combining the Equation 2.4 and 2.5 into Equation 2.3, the effective resistivity for an inhomogeneous structure as derived by *Lederer et al.*, is given by [21]:

$$\rho_{eff} = \frac{1}{\sqrt{\epsilon_{r,eff}}}\left(\frac{\epsilon_{r,eff}-1}{\epsilon_{r,Si}-1}\right)\frac{\sqrt{C_o}}{\epsilon_o}\frac{\sqrt{C_{tot}}}{G_{tot}} \quad (2.6)\ [21]$$

In which G_{tot} and C_{tot} are extracted from measurement of inhomogeneous studied structure [21]. This work also shows that higher effective resistivity can be achieved by having a thicker conductor on the oxide but did not prove it. As for density of traps, when a higher D_{it} levels enforced, larger value of effective resistivity (ρ_{eff}) obtained. This is because these traps absorb free carrier charges from the oxide-silicon interface.

Based on the previous work, the research experimentally demonstrated the distortion level of coplanar waveguide transmission line on silicon substrate by using the figure of merit mentioned above. They show the effective resistivity extracted from the simulated substrate

conductance, using the figure of merit method of effective resistivity characterization for different fixed charge densities in Figure 2.12. It can be seen in the graph that the effective resistivity of the substrate drop from the nominal resistivity of silicon, ρ_{Si} of 5 kΩ-cm to 75 Ω-cm due to the parasitic surface conduction effect. It is noticeable that for high resistivity silicon substrates without fixed charges, or extremely low fixed charges, the effective resistivity is more than twice the nominal resistivity value, ρ_{Si} [34].

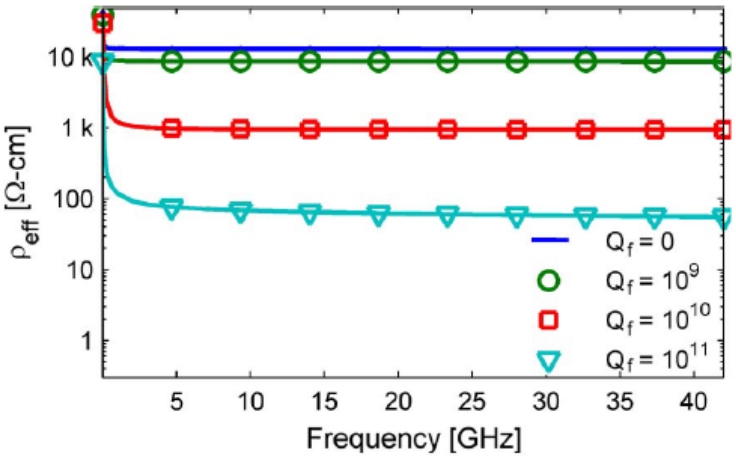


Figure 0.12: Effective resistivity for simulated CPW on n-type HR-Si. [34]

2.6 Summary

Based on the literature review that has been conducted, the factors that affecting the losses in the current monolithic microwave integrated circuit can be solve by using high resistivity silicon substrate. High resistivity silicon substrate, however, have a crucial drawback cause by parasitic surface conduction. This bias-dependent phenomenon is mainly due to the formation of free carrier charges at the oxide-silicon interface during the accumulation or inversion. Numerous methods have been conducted to suppress the parasitic surface conduction effect and one of the potential method is by using deep level doping compensation