DESIGN OF 0.13-µm CMOS LNA WITH FLAT GAIN FOR COGNITIVE RADIO APPLICATION

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by

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LIST OF ABBREVIATIONS

ADE	Analog Design Environment
AC	Alternating Current
CG	Common Gate
CMOS	Complementary Metal Oxide Semiconductor
CR	Cognitive Radio
CS	Common Source
dB	Decibel
DC	Direct Current
FCC	Federal Communication Commission
GHz	Giga Hertz
IIP3	Third Order Intercept Point
IP1dB	Input 1-dB Compression Point
LNA	Low Noise Amplifier
MHz	Mega Hertz
NF	Noise Figure
NMOS	N-Channel MOSFET
RF	Radio Frequency
SHF	Super High Frequency
SNR	Signal-to-Noise Ratio
SP	Scattering Parameters
UHF	Ultra High Frequency
UWB	Ultra wideband
WPAN	Wireless Personnel Area Network

LIST OF SYMBOLS

Ω	Ohm
$\overline{I_n^2}$	Thermal Noise
γ	Noise Factor
A_v	Voltage Gain
C_{gd}	Gate to Drain Intrinsic Capacitance
C_{gs}	Gate to Source Intrinsic Capacitance
C_{miller}	Miller Capacitance
K_f	Stability Factor
g_m	Transconductance
S_{11}	Input Reflection Coefficient
S_{12}	Reverse Isolation
S_{21}	Power Gain
S_{22}	Output Reflection Coefficient
Z_{IN}	Input Impedance
Z_L	Load Impedance
Z_0	Output Impedance
Z_S	Source Impedance

Reka bentuk 0.13-um CMOS LNA dengan Gandaan Kuasa Rata yang Tinggi Bagi Aplikasi Radio Kognitif

ABSTRAK

Penguat hingar yang rendah (LNA) adalah salah satu komponen yang sangat penting dalam penerima CR yang berfungsi untuk menguatkan isyarat yang berkuasa rendah dan dan mengurangkan bunyi tambahan yang terhasil daripada isyarat yang diterima. Cabaran terbesar dalam merekabentuk LNA bagi aplikasi ultra-jalur lebar (UWB) ialah untuk mencapai gandaan kuasa rata yang tinggi sepanjang jalur lebar yang luas. Tesis ini adalah mengenai reka bentuk penguat hingar rendah (LNA) yang mampu menghasilkan gandaan kuasa rata yang tinggi bagi aplikasi ultra-jalur lebar (UWB) dalam linkungan 300 MHz hingga 10 GHz spektrum frekuensi. Bagi membolehkan LNA untuk diadaptasi dalam aplikasi CR, ianya harus mempunyai keupayaan untuk beroperasi pada operasi jalur lebar yang luas dengan gandaan kuasa rata yang tinggi. Di samping menumpukan focus untuk mencapai target pada gandaan kuasa rata yang tinggi sepanjang jalur lebar yang luas, metric prestasi yang lain juga perlu dioptimumkan untuk mencapai sasaran spesifikasi reka bentuk yang telah ditetapkan. Reka bentuk LNA yang telah diusulkan adalah penguat cascode bersama tindak balas rintangan secara shunt, ditentukan berdasarkan kelebihannya untuk memenuhi kriteria projek ini. LNA ini telah direka bentuk dalam proses teknologi CMOS 0.13-µm daripada Silterra dan simulasi pasca bentangan telah dilaksanakan dengan menggunakan Cadence SpectreRF. Nilai gandaan kuasa rata yang diperoleh adalah 18.56 dB hingga 21.31 dB dengan kadar variasi sebanyak $\pm 2.75\ dB (15\%)$. Angka hingar (NF) adalah antara nilai 4.41 dB hingga 5 dB, nilai S_{12} < -49.43 dB dan nilai K_f > 1 telah dicapai sepanjang nilai jalur lebar yang terlibat. Reka bentuk ini juga mencapai nilai -7.97 dB bagi IIP3 manakala nilai bagi IP1dB adalah - 18.4377 dB pada 4 GHz berdasarkan simulasi pasca bentangan yang telah dijalankan. Kadar penggunaan kuasa bagi reka bentuk ini ialah 34.8 mW pada 1.2V. Berdasarkan keputusan yang telah diperoleh, reka bentuk in telah berjaya memenuhi sasaran objektif yang telah ditetapkan.

Design of 0.13-um CMOS LNA with Flat Gain for Cognitive Radio Application

ABSTRACT

A low noise amplifier (LNA) is one of the important component in a CR receiver that amplifies a very low-power signal and minimized additional noise from the received signal. The biggest challenge in designing an LNA for ultra-wideband (UWB) application as required in CR, is to obtain high flat gain throughout wide bandwidth. This thesis presents the design of CMOS LNA with high flat gain for ultra-wideband (UWB) application between 300 MHz to 10 GHz frequency spectrum. In order to implement the LNA in CR application, the LNA must be able to provide wide bandwidth operation at high flat gain. Besides focusing on the targeted high flat gain throughout the wide bandwidth, other performance metrics must be optimized to fulfill the design target specification. The proposed LNA design is a cascode amplifier with resistive shunt feedback, determined based on its merits that can fulfill the design requirement of this work. The LNA was designed in Silterra's 0.13-µm CMOS process technology and the pre-layout simulation was executed by using Cadence SpectreRF. The achieved gain is within 18.56 dB to 21.31 dB with a variation of 2.75 dB ($i.e.$ 15%). The noise figure (NF) is between 4.41 dB – 5 dB, S_{12} < -49.43 and K_f > 1 were achieved within the operating bandwidth. This design is able to achieve IIP3 value of -7.97 dB while the value of IP1dB is -18.4377 dB at 4 GHz in pre-layout simulation. The power consumption is 34.8 mW at 1.2V. The performances indicated that the design is able to achieved all the set objective.

CHAPTER 1

INTRODUCTION

1.1 Background Overview

Over the last few years, an exponential growth in wireless communication makes the wireless standard exist in various frequency bands. One of the attempts is to extend the bandwidth of operating frequency and the ultra-wideband technology (UWB) was introduced. In February 2002, the Federal Communication Commission (FCC), an independent agency of United State government introduced the 3.1 GHz to 10.6 GHz frequency spectrum for ultra-wideband (UWB) applications (Kshetrimayum, 2009). The research and development activities towards its application in data communications has massively increased because UWB system in data communication can provide high data rate, low cost and low power technology (Kshetrimayum, 2009). The possible applications of UWB technology can be applied in imaging systems, sensor networks, wireless personnel area network (WPAN) and so on. In particular, it is envisioned to replace almost all cable networks at home or in an office with a wireless connection that features hundreds of megabits of data per second.

For this project, a CMOS low noise amplifier (LNA) with flat gain for cognitive radio application is to be designed. UWB has an inherent potential to fulfill some of the important Cognitive Radio requirement (Sahin et al., 2007). Thus, there is a strong match between what is the requirement of CR and what UWB could offered. CR is the solution to the inefficient frequency management in traditional communication systems as its transmitter and receiver can intelligently detect which communication channels are available in wireless spectrum and instantly move into vacant channels while avoiding occupied ones. This will optimize the use of available radio-frequency (RF) spectrum while minimizing interference to other users.

LNA is the first stage in RF receiver architecture. Since LNA is the first stage in the RF receiver architecture, we must ensure that it must be able to amplify the signal with adequate gain and least noise as possible to the signal. This indicates that an LNA performance is very influential on the gain and noise factor of the overall receiver.

There are many LNA design produced and the main target is to obtain a flat gain more than 15 dB for large bandwidth around 300 MHz to 10 GHz. However, to design an LNA with flat gain over a wide bandwidth is very challenging. In order to satisfy all of the performance metrics according to the design specification, some trade-offs need to be made. With these two parameters (gain and the bandwidth) designed for their best performance, the other performance metrics can be at the value just meeting the design specification.

1.2 Motivation of Thesis

There are many researches conducted on LNA as it is one of the most influential component that can determine the performance of RF communication receiver. Due to massive frequency spectrum usage, the development of LNA keeps increasing and become more important. Moreover, many advanced applications are being introduced from time to time which lead to continuous research to improve the topologies for UWB LNA.

In cognitive radio (CR) application, there are 3 important characteristics that must be considered for the LNA which make it superior compared to the other type of amplifiers. Firstly, the gain flatness to avoid any signal distortion over such a wide bandwidth. Secondly, the LNA should be able to generate high power gain using low power consumption. The third characteristic is the wideband impedance matching for both maximum power transfer and optimum noise characteristic. Minimal reflections between pre-sequent and subsequent stage can be achieved by using an appropriate matching network. However, to achieve good performance in all three metrics simultaneously is a huge challenge as one performance may improve at the expense of the deterioration of another.

There are various design topologies of UWB LNA. However, each one of the topology has their own merits and demerits. It is important to choose the most suitable topology for UWB LNA. Thus, analysis of different topologies and the comparison is made between them to identify the best topology for UWB LNA. In addition, popular broadband LNA topology that employs noise cancellation technique is able to achieve a low noise figure (NF) but may face difficulties if the bandwidth is extended as the NF escalates especially at higher frequency.

The most challenging part in designing the UWB LNA is to achieve a flat gain over a wide bandwidth that covers the range from hundreds MHz to tenth GHz. Based on the LNA design from previous student, the topology is able to achieve very high gain throughout the bandwidth. However, the gain is not flat enough and the low end frequency is not low enough.

1.3 Problem Statements

As known, LNA is the first building block in the RF receiver which means it has a significant impact on the overall performance of the receiver. In designing the LNA, there are some compromise need to be made to achieve design specifications due to the trade-off between performance metrics which cannot be avoided. Since CRs utilize any occupied channel in a wide range of frequencies from several megahertz up-to several gigahertzes, the main concern amongst all the performance metrics associated with LNA is its bandwidth. There are many designs available for UWB LNA such as (Zhang and Kinget, 2006), (Pozar, 2011), (Pourjafarian and Mafinezhad, 2015), (Ragheb *et al.*, 2012) and (Razavi, 2010).

Based on the work by Zulhilmi (2016), the CG stage cascade with CS stage is implemented which provide good input and output matching as the design can be easily match with 50 Ω. The design is being able to achieve high flat gain for more than 18 dB from 4.71 GHz to 12.46 GHz and the NF value is lower than 5.8 within the bandwidth. It is important to obtain such a high flat gain at high bandwidth. However, within the bandwidth from 2.464 GHz to 3.026 GHz, the gain is lower than 15 dB and was not flat.

Thus, this design can only be utilized by only a few of the existing frequency bands such as UHF, SHF and EHF (Cheong 2013). It is a huge advantage to design an LNA that could achieve a high flat gain at the bandwidth that covers most of the frequency bands available so that these frequency band could also utilize the features that UWB can provided.

1.4 Objective

Based on the issue mentioned previously, the following objective are set.

- To identify the best suited topology for ultra-wide band LNA.
- To design an LNA for cognitive radio application which provides wide bandwidth operation at high flat gain.
- To optimize the noise figure, linearity and power consumption of the LNA to fulfil the design specification.

1.5 Project Scope

In this project, the focus is to design a UWB LNA that operates from 300 MHz to 10 GHz with flat gain. The schematic design is to be conducted using Silterra's 0.13 um CMOS Process Technology and simulated using Cadence Spectre RF. The gain should be more than 15 dB as flat as possible. This project will not cover the post-layout simulation because the only concern is up to pre-layout simulation due to cost and time constraints. The performance of proposed LNA topology will be compared with similar work by others.

1.6 Thesis Outline

This thesis consists of five chapters and is starts with an introduction in Chapter 1. In this chapter, the project's background and overview, problem statements, the objectives, project scope and organization of thesis are presented.

Subsequently, in Chapter 2, it is mainly about the theories and equations related to the design and analysis of LNA. The design topologies and techniques by others are compared in side and discussed in this chapter. Based on the related literature review conducted, the target specification for this project are determined.

In Chapter 3, the research methodology of designing a wideband LNA is given. Generally, this chapter presents the overall process sequence related to the design of the LNA including the chosen topology to be employed in this project. Work implementation flow and circuit analysis are presented in this chapter and also the optimization technique used to obtain best performance for each performance metric.

The simulation result for the schematic design are analyzed in Chapter 4. Discussion for the result obtained from pre-layout simulation are elaborated with the help of figures and tables. The performance of this work is then compared with the work by others. Finally, Chapter 5 demonstrates the conclusion for the whole project. Each of the objective stated in Chapter 1 is evaluated in terms of its achievement. Limitations and the recommendation for future development of the project are included at the end of this chapter.

CHAPTER 2

BACKGROUND AND LITERATURE REVIEW

2.1 Background

This chapter will discuss about the overview of an LNA and the highlighted point of performance metrics in designing an LNA. The theory about Scattering Parameter which is commonly used in RF and microwave analysis is also included in this section.

2.1.1 Overview of LNA

The performance of a receiver's design is measured in multiple dimensions such as receiver sensitivity, selectivity, and proclivity to reception errors. All receivers require an LNA with sufficient sensitivity to discern the residual signal from the surrounding noise and interference in order to reliably extract the embedded information. There are characteristics of LNA design needed to be control as they can affect the sensitivity of the RF receiver such as noise figure, gain, bandwidth, linearity, frequency, power consumption and dynamic range. However, controlling these characteristics requires an understanding of the active device and impedance matching to create an amplifier that achieves optimal performance with the fewest trade−offs.

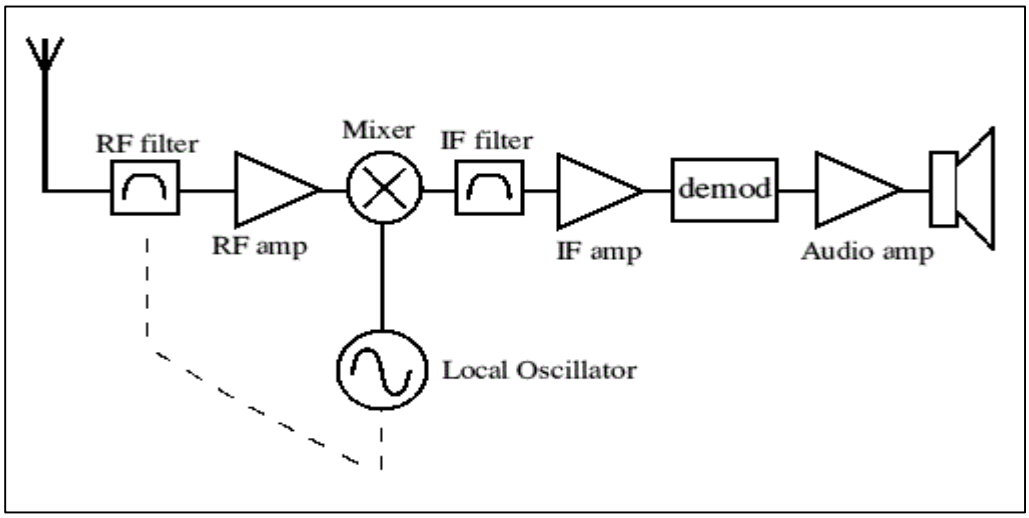

Figure 2.1 Block Diagram of RF Receiver (https://www.quora.com)

2.1.2 LNA Performance Metric

The performance metrics involved in designing the UWB LNA are elaborated in Table 2.1 below

Table 2.1 Description of each performance metric of the LNA

Performance Metric	Description
Gain	The gain value should be high and stay flat at the same time.
Frequency	A wide range of frequencies (large bandwidth) is required in LNA design for Cognitive Radio application.
Noise Figure (NF)	It is important to have low NF to ensure the LNA is resilient to noise as it dominates the overall noise of receiver.
Linearity	LNA with higher linearity can maintain a linear operation which reduced the intermodulation distortion.
Power Consumption	The power consumption of LNA should be low so that excessive energy wastage can be prevented. This is also to ensure sustainability.

2.1.3 Scattering Parameter

S-parameter is commonly used in RF and microwave analysis (Matthews, 1955). S-parameter can be used to represent incident, reflected and transmitted waves that provides a complete description of the network seen at the *N* ports system. This representation can help to relate between the incident voltage to the port and the reflected wave from the port. For some components and circuits, network analysis techniques can be used to calculate the scattering parameters (Pozar, 2011). A representation of two-port network LNA to describe the measurement of S-parameters is shown in Figure 2.2.

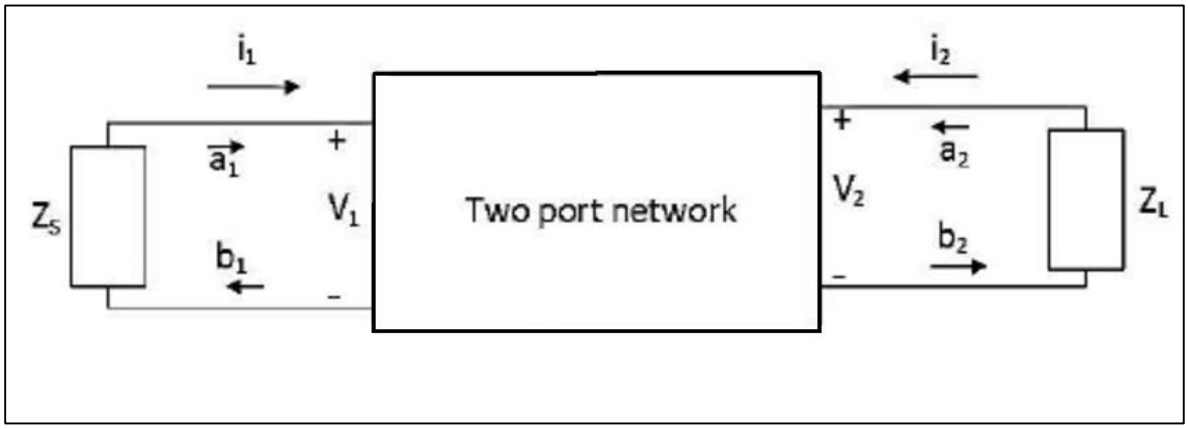

Figure 2.2: Two-port network (Azizan and Zainol Murad, 2015)

As shown in Figure 2.2, a_1 and b_1 can be related to the port voltage of v_1 and v_2 and the current of i_1 and i_2 as follows:

$$a_i = \frac{v_i^+}{\sqrt{Z_0}} \tag{2.1a}$$

$$b_i = \frac{v_i^-}{\sqrt{Z_0}} \tag{2.1b}$$

Where a_i represents an incident wave and b_i represents a reflected wave from the port (Pozar, 2011). The overall voltage and current at the *i*-th port can be written as in Equation (2.2).

$$v_i = v_i^+ + v_i^- \tag{2.2a}$$

$$i_i = i_i^+ + i_i^- = \frac{1}{Z_0}(v_i^+ - v_i^-) \tag{2.2b}$$

Substituting Equation (2.2a) and (2.2b) into Equation (2.1a) and (2.1b) yields Equation (2.3).

$$v_i = v_i^+ + v_i^- = \sqrt{Z_0}(a_1 + b_1) \tag{2.3a}$$

$$i_i = \frac{1}{Z_0}(v_i^+ - v_i^-) = \sqrt{\frac{1}{Z_0}}(a_1 - b_1) \tag{2.3b}$$

From Equation (2.3a) and Equation (2.3b), the $a_1$and b_1 can be expressed as

$$a_i = \frac{v_i^+}{\sqrt{Z_0}} - b_1 \tag{2.3c}$$

$$b_i = a_i - i_i\sqrt{Z_0} \tag{2.3d}$$

Substituting the Equation (2.3c) into the Equation (2.3d), yields Equation (2.3e).

$$2a_i = \frac{v_i + Z_0}{\sqrt{Z_0}} \tag{2.3e}$$

Equation (2.3e) also yield the Equation (2.4a) and (2.4b).

$$a_i = \frac{v_i + i_i Z_0}{2\sqrt{Z_0}} \tag{2.4a}$$

$$b_i = \frac{v_i - i_i Z_0}{2\sqrt{Z_0}} \tag{2.4b}$$

Where the value of *i* is corresponding to the port number, Z_0 is known as characteristic impedance which is purely resistive and has a standardized impedance value of 50 Ω in most of the RF circuit design. The matrix form also can be used to symbolize the two port relation as in Equation (2.5a). Equation (2.5b) and Equation (2.5c) are obtained from the given matrix.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{2.5a}$$

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.5b}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.5c}$$

Each equation gives the relationship between the reflected and incident power waves at each of the network ports, 1 and 2, in terms of the network's individual S-parameters. In order for load impedance Z_L to be equal to Z_0 ($Z_L = Z_0$), input port driven together with the output port should be terminated by Z_0. Meanwhile a_2 is set equal to zero. This enables the value for S_{11} and S_{21} to be obtained, i.e. (Adhyaru, 2007) as shown in Equation (2.6a) and Equation (2.6b) respectively.

$$b_1|a_{2=0} = S_{11}a_1$$

$$S_{11} = \frac{b_1}{a_1} \tag{2.6a}$$

$$b_2|a_{2=0} = S_{21}a_1$$

$$S_{21} = \frac{b_2}{a_1} \tag{2.6b}$$

The same method can be used to obtain $Z_S = Z_0$, where the output port is driven together with the input port ad being terminated by Z_0. At the same time, the value of a_1 is set to zero (a_1=0) in order to determine the value of S_{12} and S_{22} as shown in Equation (2.6c) and Equation (2.6d) respectively.

$$b_2|a_{1=0} = S_{12} \tag{2.6c}$$

$$S_{12} = \frac{b_2}{a_2}$$

$$b_2|a_{1=0} = S_{22}a_2$$

$$S_{22} = \frac{b_2}{a_2} \tag{2.6d}$$

Based on the statements mentioned, it is clear that for the input and output port to be matched, the value of a_1 and a_2 should be equivalent and this only happens when $Z_S = Z_0$ and $Z_L = Z_0$. The S-parameters are defined in Equation (2.7).

$S_{11} = \frac{b_1}{a_1}|a_{2=0}$ = input reflection coefficient with matched output port (2.7a)

$S_{21} = \frac{b_2}{a_1}|a_{2=0}$ = forward transmission gain with matched output port (2.7b)

$S_{12} = \frac{b_1}{a_2}|a_{1=0}$ = reverse transmission gain with matched output port (2.7c)

$S_{22} = \frac{b_2}{a_2}|a_{1=0}$ = output reflection coefficient with matched output port (2.7d)

S_{11} is the input return loss which is defined as the ratio of the reflected voltage wave to the incident voltage at the input port with load impedance matched to Z_0. S_{21} is known as forward transducer power gain as it is the ratio of the reflected voltage wave at the output port to the incident voltage applied at the input port, provided the output port termination in Z_0.

S_{12} is known as reverse isolation as it is the ratio of the reflected wave at the input port to the incident voltage wave at the output port, provided the input port termination in Z_0. S_{22} is the output return loss that is described as the ratio of the reflected voltage wave to the incident voltage wave at the output port, with the source impedance, Z_S matched to Z_0. S-parameters are commonly expressed in the unit decibel (dB) as shown by Equation (2.8).

$$S_i(dB) = 20\log_{10} S_i \tag{2.8}$$

Where *i* represent by 11,12,21, and 22. The typical value of S-parameters for LNA are S_{11} and S_{22} <-10 dB, S_{21} > 10 dB and S_{12} < -40 dB (Molavi, 2005), which may vary according to the application. Having a magnitude of 10 dB for S_{11} and S_{22} in most RF design is considered to be sufficient. Based on performance characteristic of RF and microwave transistor in (Pozar, 2011), the typical gain value for CMOS transistor is 10 dB to 20 dB. A good amplifier should possess a large S_{21} to achieve high gain, small S_{11} and S_{22} to possess good input and output matching, and small value of S_{12} to ensure stability and reverse isolation.

2.1.4 Noise Figure (NF)

Noise can be passed into a microwave system from external source, or self-generated within the system. To achieve the best performance of RF receiver, it is important to minimize the noise level. NF is defined as the ratio of the total output noise power to the output noise due to the input source (Swamy, 2013). There are various types of noise as mentioned in (Pozar, 2011), namely thermal noise, shot noise, flicker noise, plasma noise and quantum noise.

According to (Lee, 2004), shot noise essentially caused by the hopping of electric charges over a potential barrier and is specific to nonlinear devices such as transistor and diode. According to (Leach, 1994), flicker noise occurs due to the trapping of charges in the impurities and defects of the channel region in MOS devices. As a general rule, the designer assume that the larger MOS device experience less flicker noise than the smaller MOS device. The flicker noise can be ignored since the amount of flicker noise is inversely proportional to the frequency of operation. Meanwhile, thermal noise is a noise that is generated when thermal energy causes free electron to move randomly in a resistive material. MOS transistors also exhibit thermal noise and the most significant source is the noise generated in the channel. The expression for thermal noise in MOSFET can be defined as in Equation (2.9) (Razavi, 2017).

$$\overline{I_n^2} = 4kT\,\gamma\,gm \tag{2.9}$$

The noise performance of an LNA is measured by its noise factor (F) or noise figure (NF). Noise factor (F) is measured for the degradation of the signal-to-noise (SNR) caused by the component in a RF signal chain. NF can be defined as in Equation (2.10a) (Razavi, 1998) and is expressed in decibel (dB) whereas noise factor is defined as in Equation (2.10b).

$$F = \frac{SNR_{in}}{SNR_{out}} \tag{2.10a}$$

$$NF = 10\log_{10} F \ \ (dB) \tag{2.10b}$$

2.1.5 Linearity

Linearity is one of the crucial performance metric in designing an LNA. The most commonly used are the 1-dB compression point (P1dB) and third order intercept point (IIP3) (Pozar, 2011).

2.1.5.1 1-dB Compression Point

The input P1dB is usually defined as the amplitude of the input signal at which small signal gain drops 1-dB below its nominal value. Based on Figure 2.3, the actual gain of the amplifier is equal to the slope of the line in the linear region. The gain starts to decrease as the input power increases. The amplifier goes into compression region when there is no increment in output with respect to the input. The flat gain at the compression region indicates that the amplifier become saturated, and the response become non-linear resulting in signal distortion.

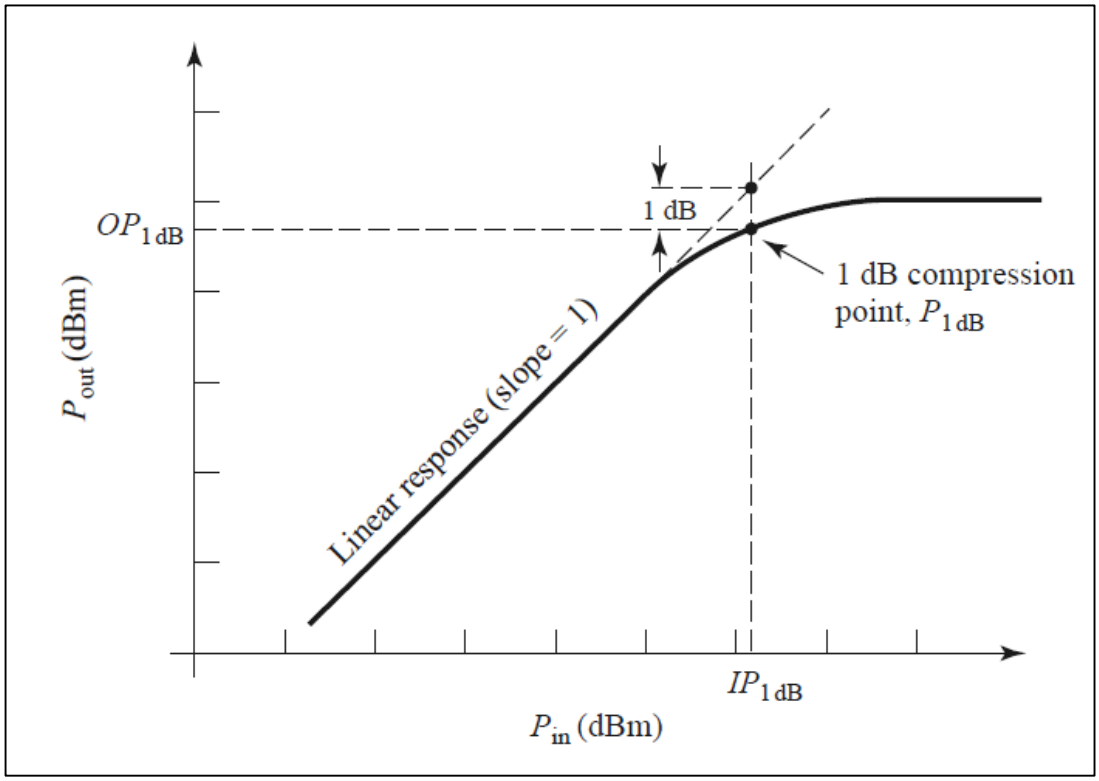

Figure 2.3: 1-dB compression point (Pozar, 2011)

2.1.5.2 Third-Order Intercept Point

An LNA with good linear properties should have a high value of input third-order intercept point (IIP3). Figure 2.4 shows the IIP3-at which the third-order distortion signal amplitudes equal to the power of the first order output. The IP3 value indicates how large a signal that the amplifier can process before intermodulation distortion (IMD) occurs. Output referred (OIP3) represents the maximum output power that can be produced by an LNA before signal degradation.

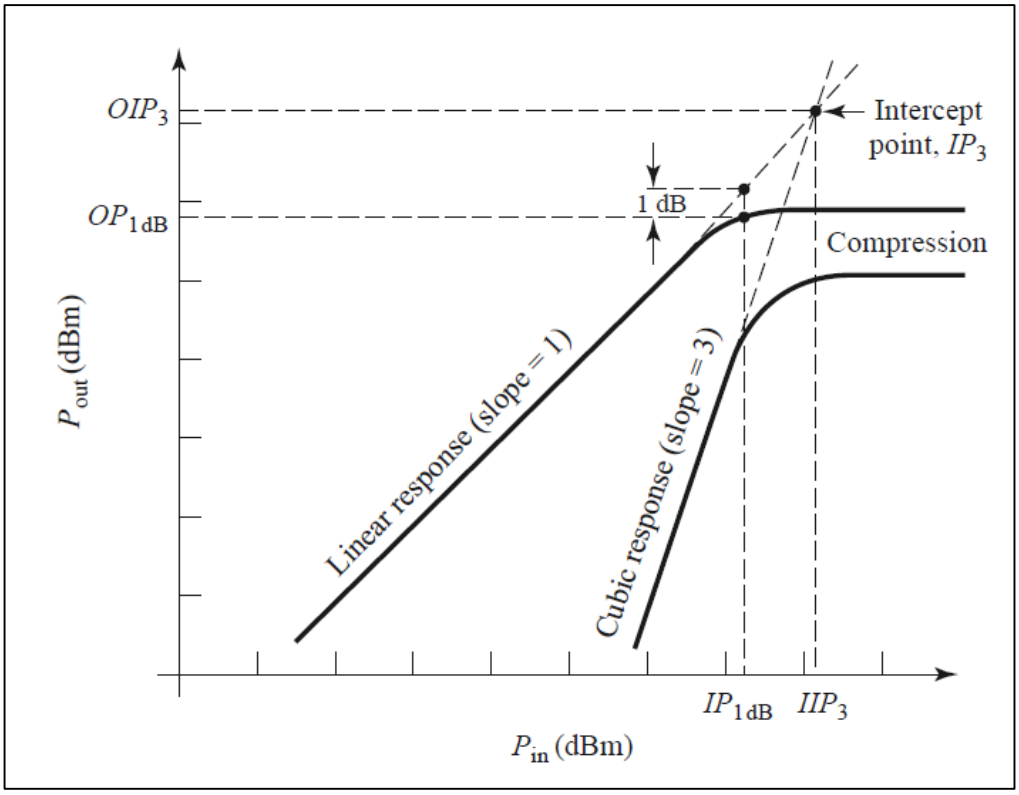

Figure 2.4: Third-Order Intercept (Pozar, 2011)

2.1.6 Nonlinear Effect (Miller Effect)

There is an important element that we need to be considered when dealing with amplifier which is Miller Effect. It is a must to overcome the imperfection from this effect on amplifier due to high frequency amplification design. C_{gd} in MOSFET can be defined as input by $1+A_v$ which is an amplifier gain. Meanwhile at the input, the input capacitance by $C_{miller} = C_{gd} = 1+A_v$ which caused the bandwidth become narrower. Figure 2.5 shows an example of Miller Capacitance.

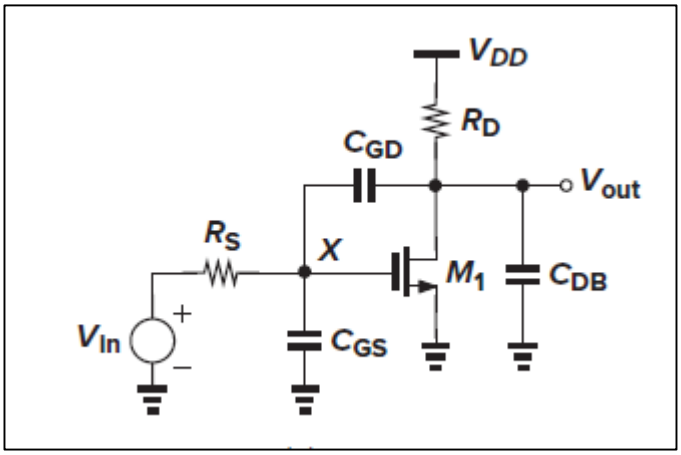

Figure 2.5: Example of Miller Capacitance of CS amplifier (Razavi, 2017)

Several techniques can be applied to reduce the effect of C_{gd}. For example, by reducing the overlapping area between the drain and gate pins. The voltage gain, A_v, common source (CS) amplifier need to be reduced to value 1 by adding a common gate (CG) amplifier, at which the output is isolated from the input by AC grounding the gate by a bypass capacitor. This is also known as cascade network based on (Miller, 1919) in (Razavi, 2017).

2.2 Literature Review

There are abundance LNA designs available today. With the rapid development in the field of technology, the research and enhancement has been developed throughout these past decades to improve the LNA design.

2.2.1 Comparison of LNAs' performances from previous works

Designs from 4 different authors are selected and compared with respect to the performance metrics of their LNA design. The work that had been selected are Ragheb et al. (2012), Lin et al. (2007), Shim et al. (2013), and Pokharel et al (2008). Table 2.2 summarizes the comparison of LNA performance from each work by the authors.

Table 2.2: Comparison on LNA performance from previous works.

Performance Metrics	(Ragheb *et al.*, 2012)	(Mirvakili and Yavari, 2009)	(Shim *et al.*, 2013)	(Pokharel *et al.*, 2008)
Topology	2-stage CS using Current Reuse Technique	Noise Cancelling LNA	Noise-cancelling LNA	Cascode Amplifier with Resistive shunt-feedback
Bandwidth (GHz)	3-11.	4.7-11.7	3.1-9.8	3.1-10.2
S_{11}	< -10.61	<-8	<-11.9	<-13.43
S_{21}	14.44-15.76	12.4	10.4–12.6	18.1-20
S_{12}	< -40	-	<-23	<-40
Power (mW)	8.65	13.5	15.2	24
NF (dB)	2.70-3.38	2.88-3	2.9-5.4	3.5
IIP3 (dBm)	3.0	-3	-4.6	-9
CMOS Technology (um)	0.18	0.13	0.18	0.18

Each topology provides different value of power gain. So, it is important to choose the topology that provides the best value of power gain. Based on the Table 2.2, it can be seen that both Ragheb et al.'s (2012) and Pokharel et al.'s (2008) provide higher gain value than Shim et al.'s (2013) and Mirvakili et al.'s (2009). This is because the value of gain is higher if the design is using the CG cascade with CS topology which is being applied in current reuse technique than the gain achieved by the noise cancelling techniques. Pokharel et al.'s (2008) provides the highest value of gain. This is because Pokharel et al.'s (2008) using CS with shunt inductive peaking being applied at the third stage of the circuit to achieve high gain at high frequency and resistive shunt feedback to flatten the gain. What is more important, the power consumption of Pokharel's design is the highest amongst the four and this contributes to the highest gain. It is always a trade-off between having a high gain or low power consumption.

When comparing the NF value, there is a trend that can be hypothesized. When the higher power consumption is being used in the design, the value of NF will decrease. Comparing the work from Pokharel et al.'s (2008) and Shim et al. (2013), the power consumption for Pokharel et al.'s (2008) is higher than Shim et al. (2013). Hence, the NF value of Pokharel et al.'s (2008) is generally lower than Shim et al. (2013). Thus, there is a trade-off in the power consumption and the NF. However, it is a different case with Ragheb et al.'s (2012) which uses current reuse technique and is able to achieve low the power consumption as well as low NF simultaneously.

The decreasing size of CMOS technology will result in better NF for the LNA. This can be seen when we compare the NF value between Mirvakili et al. (2009) and Shim et al. (2013). Both of them using the same Noise cancelling topology, however the NF value of Mirvakili et al. (2009) is lower than Shim et al. (2013) which is 2.88-3 dB and 2.9-5.4 dB respectively. However, the better noise performance can also be contributed by the higher power consumption by Mirvakili. Considering a 0.13-µm process has lower V_{DD} than a 0.18-µm process, the current consumed by Mirvakili's design is much higher than that by Shim.

Yet, the main focus of designing a UWB LNA is generally the bandwidth. The bandwidth from the works of Ragheb et al.'s (2012) and Pokharel et al. (2008) are wider than that of Mirvakili et al. (2009) and Shim et al. (2013). Amongst the compared work in Table 2.2, Ragheb et al. (2012) exhibits the largest bandwidth. The work from Pokharel et al. (2008) is selected as the most suitable topology to be employed in this project considering the ability of the topology to provides wide bandwidth operation at high flat gain. Thus, the objectives of this project could be fulfilled.

2.2.2 LNA Circuit Topologies

The two well-known LNA topologies found are the common source (CS) and common gate topologies (CG) (Klumperink, Bruccoleri and Nauta, 2001). There are various other topologies as well which ~~is~~ are discussed here in detail along with the aforementioned popular configurations.

2.2.2.1 Common Gate Topology

The wideband input impedance matching was first introduced by (Bode, 1945) and (Fano, 1950) as discussed in (Pozar, 2011) which was to improve the bandwidth of the antenna. Common gate structure is a well-known method to provide a wideband input matching. Figure 2.6 shows the conventional CG-LNA where the inductor resonates with the parasitic capacitance of the impedance-matching device and the input pad.

The input-matching network of the CG LNA is a parallel resonance as opposed to the series resonance of the inductor-degenerated LNA. Hence, a low Q (quality factor) of the input matching network results in a wider bandwidth. The CG-LNA is more robust to process, voltage, and temperature (PVT) variations (Kim, 2011). The power gain of CG LNA is relatively low due to the impedance-matching constraint.

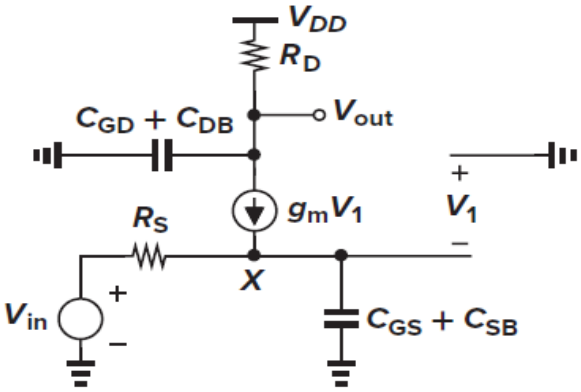

Figure 2.6: CG LNA (Razavi, 2010)

2.2.2.2 Noise Cancellation Technique

This circuit consists of two stages which are the CG topology at the first stage and the CS as the second stage. The CG topology at the first stage provides high gain and a wideband input matching. However, the NF produced at this stage is also high. Thus, the implementation of CS as the second stage is used to cancel the noise. Figure 2.7 shows the LNA topology with the implementation of both CG and CS.

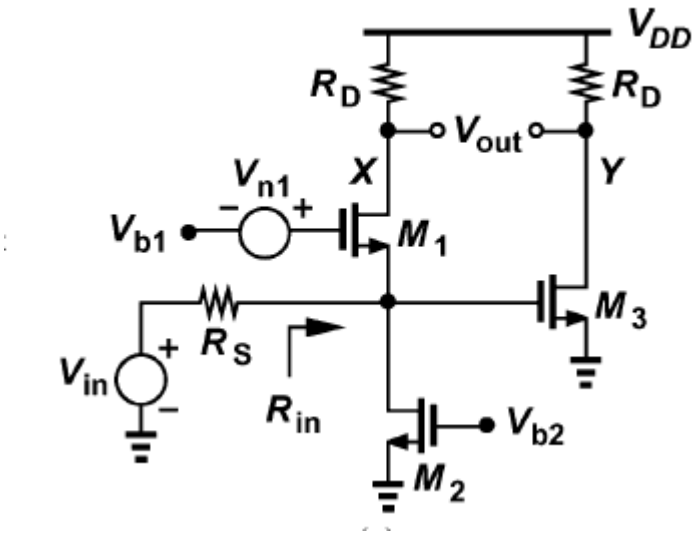

Figure 2.7: Noise Cancelling LNA (Razavi, 2010)

Based on the Figure 2.7, the noise exists at the output nodes X and Y. Thus, by the use of the structure as shown above, the noise can be cancelled (Razavi, 2010).

2.2.2.3 Current Reuse Technique

The typical schematic of current-reused LNA is shown in the Figure 2.8. The current reuse technique can reduce the power consumption of LNA while preserving high-gain. However, since the second stage of the traditional current-reused LNA topology requires a DC bias as well as resistor, an extra noise and signal leakage will be produced (Wu and Lin, 2010).

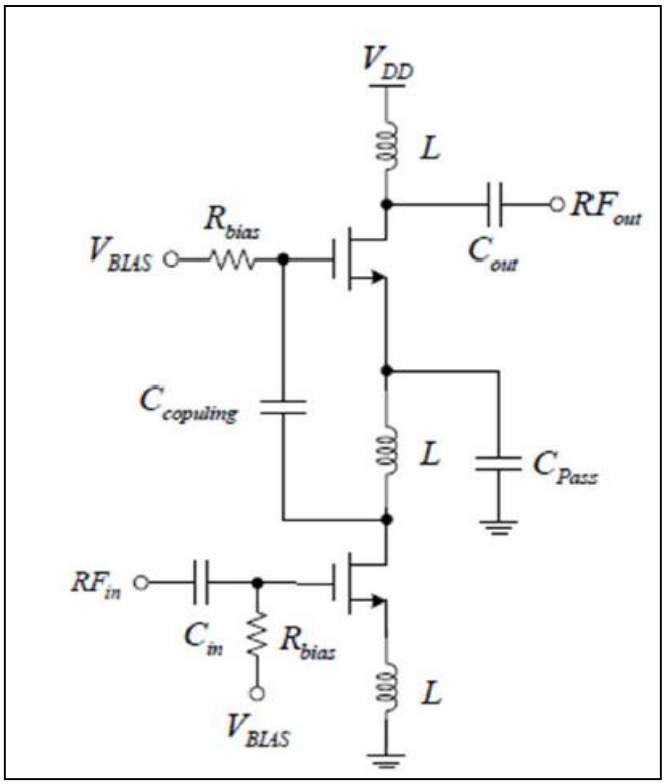

Figure 2.8: Conventional current reuse configuration (Wu and Lin, 2010)

By using the current-reused technique, the power consumption, noise and the IIP3 can be improved. A major drawback of this design is its high input and output impedances, thus requiring external impedance matching networks. This prevents the use of this LNA in fully integrated applications. Due to the high gain property, the strong Miller effect reduces the reverse isolation of this LNA.

2.2.2.3 Resistive Feedback Technique

Feedback offers numerous benefits for broadband amplification, including gain, stability over processing and supply variations, lower distortion, and the ability to tailor port impedances for noise and impedance matching (Reiha and Long, 2007). The typical schematic of resistive feedback LNA is shown in Figure 2.9.

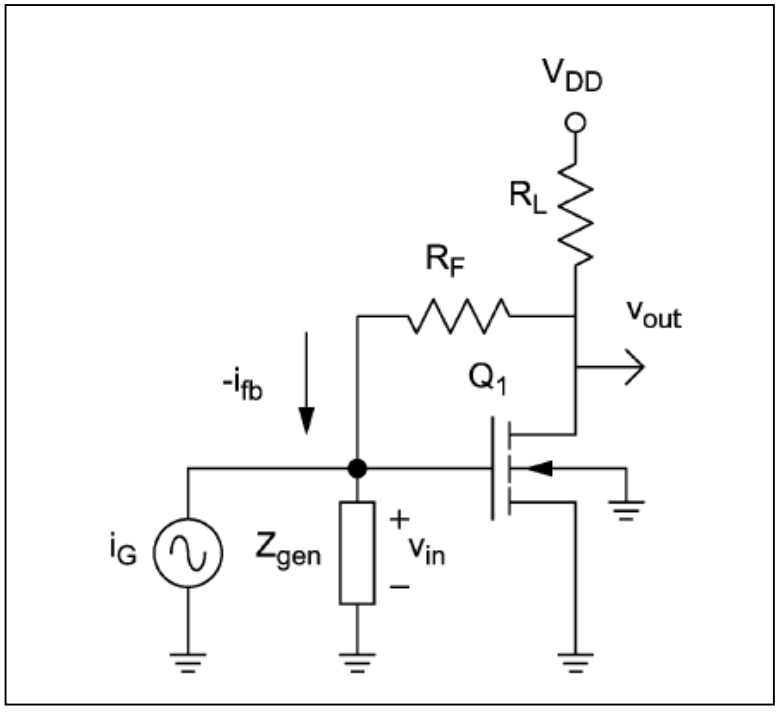

Figure 2.9: Resistive feedback LNA (Reiha and Long, 2007)

Resistive shunt feedback is a widely known technique in wideband amplifiers. A broadband input match can be achieve by increasing the feedback resistor, R_f. This also improves the noise figure, NF.

CHAPTER 3

METHODOLOGY

3.1 Introduction

It is well known that LNA is one of the most crucial part and has a significant impact on the overall performance of the RF receiver. UWB LNA has the ability to support wide range of applications. To manage the ultra-wide spectrum and operate at a low power at the same time poses severe challenges in the design of a UWB LNA.

This work is a preliminary attempt to construct a CMOS LNA with gain more than 15 dB with wide range of frequencies from 300 MHz to 10 GHz. To design an LNA for CR application, it is essential for the LNA to provide the wide bandwidth, moderate but flat gain over entire bandwidth, low NF, good linearity and lower power consumption. Yet the design of an LNA is constrained by the maximum power transfer.

The overall process began with circuit analysis to understand how the circuit works. At this point, an optimization should be made to improve the circuit performance to meet the design specification as well as the objectives of this work. In addition, it is necessary to be familiar with the software that is related to this work, Cadence SpectreRF, to obtain the simulation data for design verification and further analysis.

3.2 Project Implementation Flow

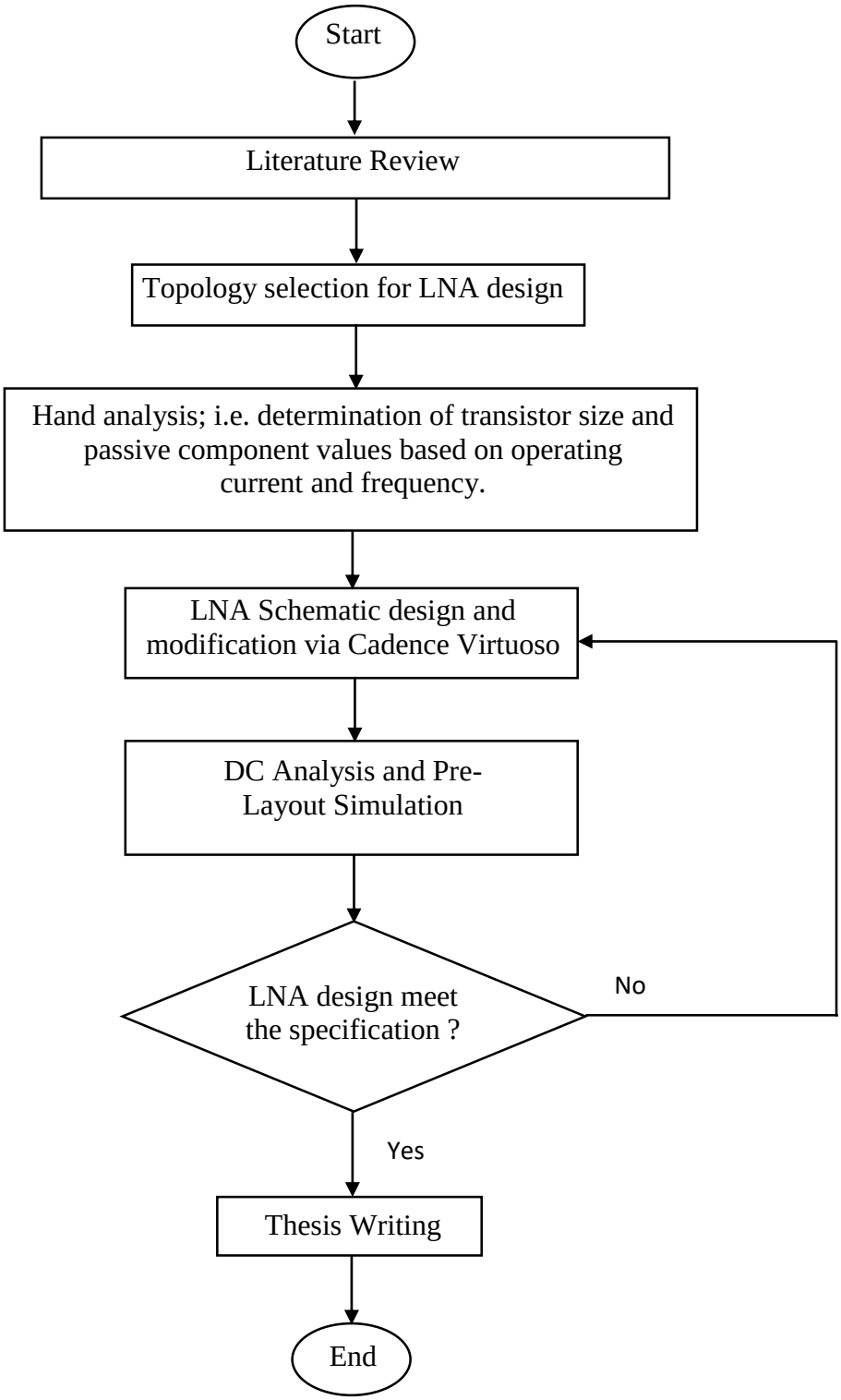

Figure 3.1: Project and Design Implementation Flow