DESIGN AND SIMULATION OF HIGH Q INDUCTORS ON AU-COMPENSATED HIGH RESISTIVITY SILICON

YAP CHEE SEONG

UNIVERSITI SAINS MALAYSIA

2017

DESIGN AND SIMULATION OF HIGH Q INDUCTORS ON AU-COMPENSATED HIGH RESISTIVITY SILICON

By

YAP CHEE SEONG

Thesis submitted in partial fulfilment of the

requirements for the degree of

Bachelor of Engineering (Electronic Engineering)

JUNE 2017

ACKNOWLEDGEMENTS

First and foremost, I must thank Dr. Nur Zatil ‘Ismah Hashim, my research supervisor, for seeing the promise of this thesis and achieving research conducted under her watchful eyes. Her guidance and patience throughout the tumultuous time of conducting scientific investigations related to this project are much appreciated. Besides, her invaluable support and insightful suggestions, not to mention all the hardwork and extra time poured in has resulted in the completion of this project, with the achievement of few publications under her belt.

Because science and engineering is not a collection of knowledge, I would like to thank Dr. Mohd Tafir Bin Mustaffa f, my project examiner, for his positive feedback and suggestions in providing a deeper understanding.

Last but not least, applauds and appreciations are dedicated to my loving parents and other friends for their inputs, supports.

Table of Contents

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

Au	Gold
BOX	Buried oxide layer
CBCPW	Conductor-backed coplanar waveguide
CZ	Czochralski Silicon
FZ	Float-zone
GaAs	Gallium arsenide
IC	Integrated circuit
IPDs	Integrated passive devices
MMIC	Monolithic Microwave Integrated Circuit
PSC	Parasitic surface conduction
Q-factor	Quality factor
RF	Radio Frequency
Si	Silicon
SiO_2	Silicon dioxide
SOI	Silicon-on-insulator
TSVs	Through-Silicon-Vias

REKA BENTUK DAN SIMULASI INDUKTOR Q TINGGI PADA SILIKON PAMPASAN-AU KERINTANGAN TINGGI

ABSTRAK

Potensi silikon kerintangan tinggi pampasan-Au sebagai substrat mikro gelombang disiasat memandangkan substrat semikonduktor kerintangan yang tinggi memainkan peranan yang penting dalam penurunan kehilangan dan keupayaan peranti MMIC berprestasi tinggi. Substrat kerintangan yang tinggi adalah penting untuk mengekalkan nisbah isyarat-kepada-hingar pada tahap yang boleh diterima dan menyediakan kecekapan penghantaran kuasa tinggi dalam permohonan mikro gelombang. Kerintangan tinggi pampasan-Au boleh digunakan sebagai substrat asas yang dapat dimasukkan ke dalam teknologi RF-MMIC seperti integrasi IPD, TSVs dan oksida dikebumikan. Integrasi IPD menjadi pertimbangan dalam kerja ini dan ‘meander’ dipilih sebagai peranti pasif kerana ciri satah dimiliki. Dalam kerja ini, tiga ‘meander’ dengan pelbagai segmen telah direka dan disimulasi dengan menggunakan substrat pampasan-Au kerintangan tinggi. Di samping itu, kearuhan bagi pengaruh ‘meander’ dikira dan pengiraan adalah berdasarkan Greenhouse 1974 dan Grover 1954. Berdasarkan keputusan simulasi, faktor Q bagi pengaruh ‘meander’ berkurangan apabila bilangan segmen panjangnya bertambah. Selain itu, faktor Q bertambah apabila penurunan kearuhan berlaku, yang bermakna perlunya keseimbangan antara faktor Q bagi pengaruh Meander dan nilai kearuhan.

DESIGN AND SIMULATION OF HIGH Q INDUCTORS ON AU-COMPENSATED HIGH RESISTIVITY SILICON

ABSTRACT

The potential of the Au-compensated high resistivity silicon as a microwave substrate was investigated as the high resistivity semiconductor substrates play a crucial role in low loss and high performance MMIC devices. High resistivity substrates are essential to keep the signal-to-noise ratio at acceptable levels and provide high power transmission efficiency in microwave application. The Au-compensated high resistivity can be used as a base substrate which able to be incorporated into the RF-MMIC technology such as integration of IPDs, TSVs and buried oxide. The integration of the IPD was the concern in this work and the meander inductor was chosen as the passive device due to its truly planar characteristic. In this work, three meander inductors with different number of segments of the greatest length was designed and simulated by using the Au-compensated high resistivity substrate. In addition, the inductance for the meander inductors was calculated and the calculation was based on Greenhouse 1974 and Grover 1954. Based on the simulation result, the Q factor of the meander inductor decreases as the number of segments of the greatest length increases. Besides, the Q factor of the meander inductor increases as its inductance decreases which means there is a trade-off between the Q factor of the meander inductor and its inductance value.

CHAPTER 1

INTRODUCTION

1.1 Research Background

Monolithic Microwave Integrated Circuit (MMIC) is a type of integrated circuit (IC) device that able operates in microwave frequency range which from 300MHz to 300GHz. As the operating frequency of MMIC device increases, high resistivity semiconductor substrates play a crucial role in low loss and high performance MMIC device such as microwave mixing, low-noise amplification, power amplifier and high frequency switching. The high resistivity substrates are essential to keep the signal-to-noise ratios at acceptable levels as well as provide high power transmission efficiency in microwave application. The devices that benefit from the high resistivity substrates include transmitters and receivers, high-Q inductors and capacitors, super high frequency mixers, coplanar waveguides and low-loss microstrip lines.

The most common high resistivity semiconductor substrates have always been associated with III-V semiconductor materials such as GaAs which produced by introducing deep-level traps during crystal growth. The reason that these materials was chosen to produce high resistivity substrates is its wide band-gap nature of the compound substrates and such substrates have resistivity in the 10^8 ohm-cm range. However, being GaAs, the fabrication cost was undesirable due to its complexity in creating compound semiconductors. Silicon (Si), on the other hand, has the less complexity and lower fabrication and manufacturing cost. Nevertheless, the resistivity of Silicon is relatively low compared to GaAs which its highest resistivity is about 10^5 ohm-cm. Although multiple Float-zone (FZ) passes can produce high resistivity Silicon which about 10,000 ohm-cm due to FZ has low oxygen concentration, the wafer diameter is limited. Czochralski (CZ) Silicon, is another method which able growing larger diameter ingots than FZ. However, CZ no only contain relatively higher oxygen concentrations compared to FZ but also introduces higher level of contamination lead to the increment of background free carriers which further decrease the resistivity of silicon. The solution to solve the issue is by introduced the silicon-on-insulator (SOI) technologies which have

the advantages in reduced source and drain capacitances, higher transconductance and dielectric isolation. The combination with SOI technologies make the low cost, low loss and high performance MMIC devices become possible.

The parasitic surface conduction effect underneath the buried oxide layer (BOX) lead to degrades its effective true resistivity. The parasitic surface conduction effect has been proven in [1] and [2] by using coplanar waveguides, the transverse electric field through the SiO_2/Si interface induces a highly conductive surface carrier channel (accumulation or inversion). In addition, this parasitic surface conduction increases the substrate RF losses and crosstalk [3] and reduce the effective resistivity of the high resistivity silicon wafer by more than one order of magnitude [4] as well as the high resistivity silicon substrates also become more non-linear.

This parasitic surface conduction can be effectively minimizing by increasing the trap density near the insulating oxide to freeze the attracted free carriers, recover the nominal resistivity values of the high resistivity silicon and stabilize the whole wafer surface. The techniques such as ion implantation in [5], deposition of amorphous silicon [6], and polycrystalline silicon layer [7] between the high resistivity silicon handle substrate and the oxide can use to achieve the reduction of the parasitic surface conduction effect. Deep level doping compensation was chosen throughout the work to provide a high resistivity silicon substrate and high volume of trap densities at silicon surface. This deep level doping compensation effectively reduced the substrate and interface losses as well as it's a one of the flexible alternative for bulk RF silicon substrate. In [8] and [9], the gold-compensated Czochralski-silicon (Cz-Si) has successfully reduced the background free carrier concentration and increasing the resistivity of Cz-Si by three order of magnitude.

1.2 Problem Statement

In paper [10], it illustrates that the material that used for the integrated passive device (IPD) substrate is polysilicon. It has been used in integrated circuit technology many years as the technology of polysilicon is well known and well developed in terms of properties and thin film deposition techniques. Whereas in paper [11], it states that

GalliumiArsenide (GaAs) substrates are the one of the common platforms for fabricating RF passive devices. In fact, the common high resistivity semiconductor substrates nowadays are semi-insulating GaAs which produced by introducing deep-level traps. For example, metal-semiconductor FETs are fabricated based on semi-insulating GaAs substrates. In short, there is no mature research about the incorporation of gold-compensated high resistivity silicon into RF-MMIC technology such as integrated passive devices (IPDs) and 3D-integration using Through-Silicon-Vias (TSVs).

1.3 Objective of Research

The objectives of this research are:

1. To provide a conclusive study on the potential of integration of planar meander inductor on Au-compensated high resistivity silicon substrate
2. To design and simulate meander inductor topology on Au-compensated high resistivity silicon substrate
3. To calculate the inductance value for the meander inductor using Greenhouse 1974 and Grover methods
4. To observe the Q factor performance of the meander inductor

1.4 Scope of Research

The Conductor-backed coplanar waveguide (CBCPW) structure is designed and simulated using CST. Besides, the inductance of the high-Q meander inductor is calculated using MATLAB whilst the structure of meander inductor is designed and simulated using CST.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Compensation doping is used to control the properties of the semiconductor through doping both shallow donors and shallow acceptors in semiconductor. The type of Si is determined by the resultant concentration of shallow donors and shallow acceptors. If acceptor concentration, N_A is much higher than the donor concentration, N_D, the substrates becomes p-type and vice versa. Full compensation occurs when the N_D is equal to the N_A yielding no free carriers in Si. Figure 2.1 show the compensation doping process which adding both donor and acceptor impurities in the same region.

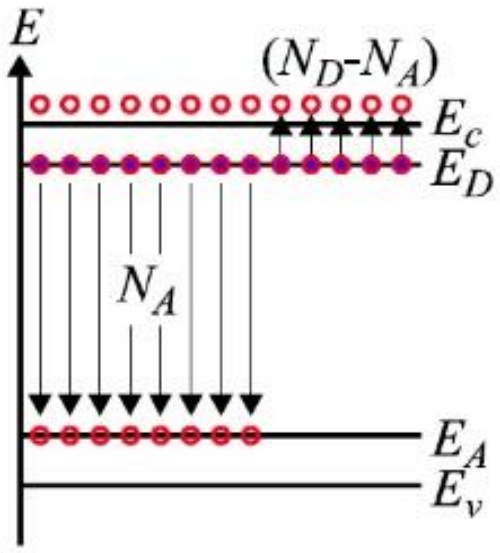
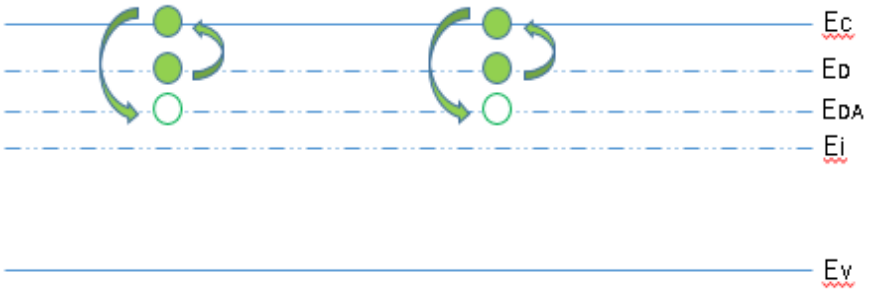


Figure 2.1: compensation doping

The compensation doping process can happen between shallow impurities and deep impurities. The shallow acceptors are being compensated by deep donors, N_{DD} whilst the shallow donors are being compensated by deep acceptors, N_{DA}. Figure 2.2 show the compensated doping process between shallow impurities and deep impurities.

The majority carrier electrons from E_D are initially excited to conduction band, E_C then fall to E_{DA} level and recombined with minority carrier holes at this energy level. This process called compensation of shallow donors by deep acceptors, N_{DA} which the negatively charged are trapping minority carrier holes at E_{DA} level. On the other hand, the positively charged N_{DD} are trapping minority carriers electrons at E_{DD} level are called shallow acceptors compensated by deep donors. The majority carrier holes fall into valence band, E_V whilst trapping electrons at E_{DD} level and then recombined with minority carrier electrons which fall from the E_{DD} level. There is no generation of free carriers occurs in both situation.



(a) Shallow donors are compensated by deep acceptors, N_{DA}

(a) Shallow acceptors are compensated by deep donors, N_{DD}

Figure 2.2: Compensated doping process between shallow impurities and deep impurities

This show that deep level doping compensation can effectively reduce the generation of free carriers. Meanwhile, deep level doping has become the basic of developing new method in producing high resistivity Czochralski silicon. In short, the effect pin the Fermi

level near the middle of the Si bandgap and the ability of trap carriers inside Si lattice leading to the high resistivity Si substrate can be achieved.

The deep level doping element was Au throughout the work because it need less tight control over dopant concentration and minimal overcompensation effect. The experiment done in papers [12-13] were proved that Au-doping can increase the resistivity of silicon successfully.

2.2 Implementation of Au-compensated HR-Si in microwave technology

Czochralski silicon is an excellent material for fabrication of integrated circuits [14]. Although it is previous suffers from the problem that CzSi technology lacks very high resistivity semi-insulating substrates, the problem was solved by using Au-compensated high resistivity silicon. In [15] and [16], gold (Au) had been used successfully to increase the resistivity of Si by introducing deep donor and acceptor states at E_C -0.78eV and E_V +0.56eV respectively [17]. However, the high diffusivity of Au in Si ($3.5 \times 10^{-6} cm^2 s^{-1}$ at 800^oC) gold atoms [18] is detrimental for silicon wafer-processing as it can diffuse to active regions of the devices during high temperature device process step, and may degrading the performance of device. Thus, the application of Au-compensated HR-Si substrates are only focussing on specific RF-MMIC technology such as integrated passive devices (IPDs) [19,20], 3D-integration using Through-Si vias (TSV) [21], and the realisation of SOI devices with buried oxide (BOX) as diffusion barrier in between handle and active Si wafers [22,23]. All the technology that included Au-compensated HR-Si was based on one principle which is to have active devices as far as possible from the substrate to prevent it from ruin those devices.

2.3 Meander Inductor

Planar inductor has been chosen due to it is one of simplest integrated passive device. There are two types of planar inductor which are meander inductor and spiral inductor. However, meander inductor is specifically chosen for design IPD on top surface of Au-compensated high resistivity silicon for two reasons. First, it requires only one layer of material to be implemented, i.e. it is truly planar, so it providing way to avoid more levels

of photolithograph. Secondly, in published paper [24] was shown that meander topology yields the higher coupling coefficient out of several planar variations. The meander inductor gives weaker performances compared to spiral inductor. Although meander inductor not only providing weaker inductance per equal chip surface but also has weaker quality factor (Q-factor) for the equal inductance due to the longer conductor which generate greater DC resistance, it was still chosen for this project because of its' simple process of production and less coupling with the rest of the circuit.

In [25], the spiral and the meander type inductors were fabricated and the measurement results were compared and analysed. Based on the results in [25] as shown in figure 2.3, the inductance of the spiral inductor is 600nH, which is about eight times higher than that of the meander inductance. In addition, the resonance frequency of the spiral and the meander inductor were 100MHz and 300MHz respectively. The inductance of the meander inductor is lower than the that of spiral inductor with the identical of current adjacent coils because the mutual inductance of the meander inductor is negative due to the opposite of current adjacent coils. Figure 2.4 show the Q factor of the spiral and the meander inductor. The Q factor of the spiral inductor is higher than that of the meander inductor due to that the inductance increment is large and the resistance increment is small. Table 2.1 show the summary of comparison between the spiral and meander inductor.

Table 2.1: Summary of comparison between spiral and meander inductor

	Spiral	Meander
Inductance	~600 nH	~75 nH
Resonant frequency	~100 MHz	~300 MHz
Peak Q factor	~5	~1

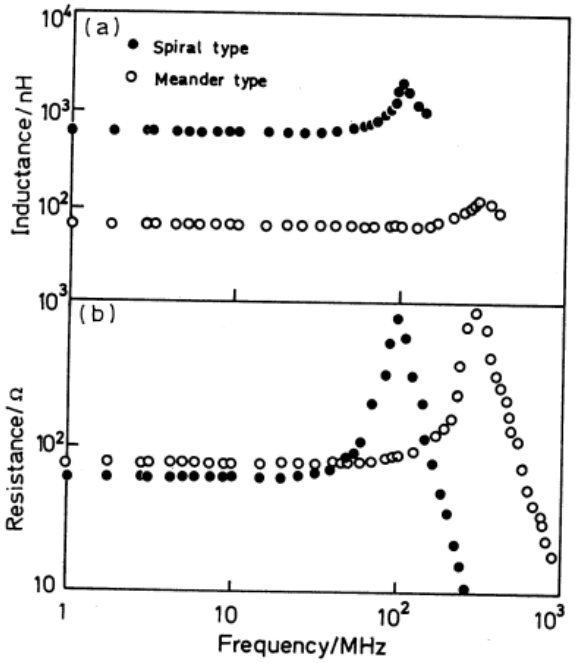


Figure 2.3: frequency characteristic of inductance and resistance in the inductors

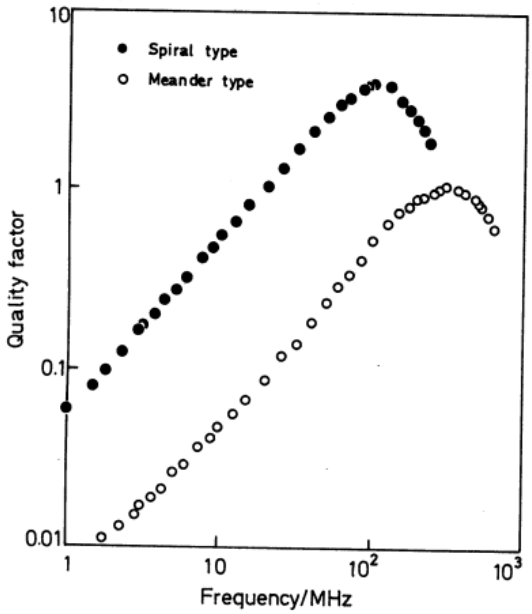


Figure 2.4:frequency characteristic of quality factor in the inductors

2.4 Inductance Calculation in Meander Topology

The total inductance of meander inductance can be determined by calculating the summation of self-inductance and mutual inductance. The layout of meander inductor is shown in Figure 2.5 whereas the figure 2.6 show that the cross-section of one conductive segment of a meander inductor.

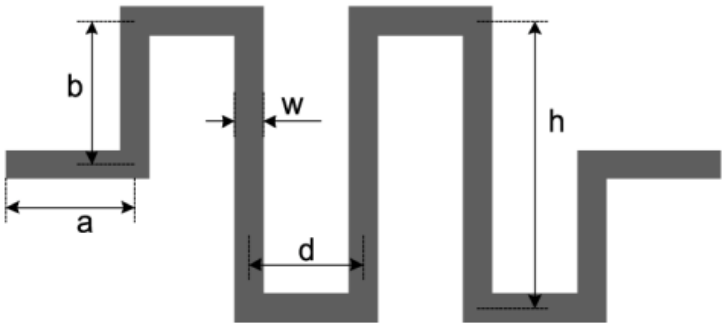


Figure 2.5:meander inductor with characteristic dimensions

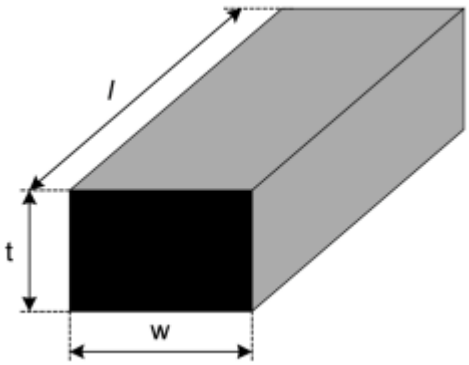


Figure 2.6:cross-section of one conductive segment of a meander inductor

The starting point for the calculation of inductance of meander inductor is Greenhouse 1974 theory. Greenhouse decomposed inductor into its constituent segments which means that the meander inductor is basically divided into straight conductive segments. The self-inductance of individual straight segment can be calculating by using equation (2.1) which based on Greenhouse 1974 theory.

$$L = 0.002l\left[\ln\left(\frac{2l}{w+t}\right) + 0.50049 + \left(\frac{w+t}{3l}\right)\right] \quad (2.1)$$

The parameters for the equation (2.1) are L = inductance in microhenries, l = length of conductive segment in centimetres, w = width of the rectangular cross section and t = thickness of the rectangular of the cross section.

The total self-inductance $L_{selftot}$ is calculated by using equation (2.2) as a sum of self-inductances of all individual line segments which form meander inductor. Figure 2.7 show characteristic geometrical dimensions of the meander inductor with N=6.

$$L_{selftot} = 2L_a + 2L_b + NL_h + (N+1)L_d \quad (2.2)$$

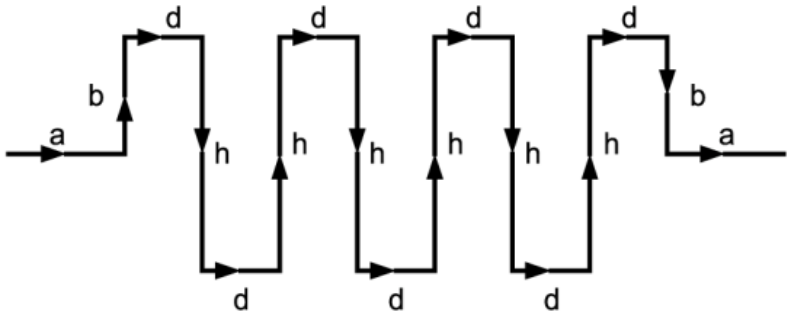


Figure 2.7: characteristic geometrical dimensions of meander inductor

This is a generalized equation where $L_{a,b,h,d}$ are self-inductances of segments where the length is l = a, b, h, d respectively and N represents a number of segments of the greatest length h. The self-inductances for each individual line segments are calculated by using the equation (2.1).

In addition to Greenhouse's, Grover (1954) also contributed extremely to the inductance calculation. Grover has considered the concept of partial inductance which the contribution of individual segments to the overall inductance. The equation (2.3) which taken from the book of Grover (1954) calculates the mutual inductance, M_c of the segments with equal length l, at distance r and are place opposite one to another as shown in Figure 2.8.

$$M_c(l,r) = \pm\frac{\mu_o}{2\pi} l\left[ln\left(\frac{l}{r}+\sqrt{1+\left(\frac{l}{r}\right)^2}\right)-\sqrt{1+\left(\frac{r}{l}\right)^2}+\frac{r}{l}\right] \quad (2.3)$$

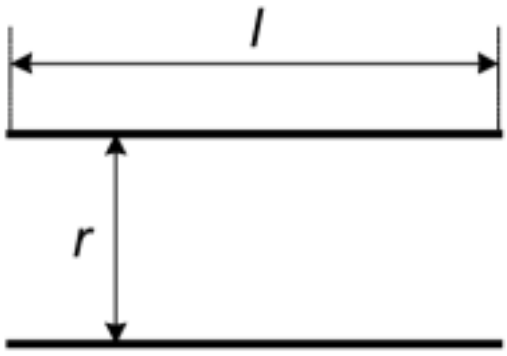


Figure 2.8: two equal parallel straight filaments

Furthermore, the two cases of the inductor which with even and odd number of the longest segments, h need to be considered in order to calculate the total mutual inductance. Figure 2.9 show some characteristic situations of the position of two segments that can appear in meander inductors. The equation (2.4) to (2.7) expressed the mutual inductance for the segment positions by linear combinations of the equation (2.3).

$$M_{a1}(l_1,l_2,r,s) = 0.5[\, M_c(l_1+l_2+s,r)+M_c(s,r)-M_c(l_1+s,r)- M_c(l_2+s,r)\,] \quad (2.4)$$

$$M_{a2}(l_1, l_2, r) = 0.5[\, M_c(l_1, r) + M_c(l_2, r) - M_c(l_1 - l_2, r)\,] \tag{2.5}$$

$$M_{a3}(l_1, l_2, r) = 0.5[\, M_c(l_1 + l_2, r) - M_c(l_1, r) - M_c(l_2, r)\,] \tag{2.6}$$

$$M_b(l_1, l_2, s) = \frac{\mu_o}{4\pi}[(l_1 + l_2 + s)\ln(l_1 + l_2 + s) - (l_1 + s)\ln(l_1 + s) - (l_2 + s)\ln(l_2 + s) + s\ln(s)\,] \tag{2.7}$$

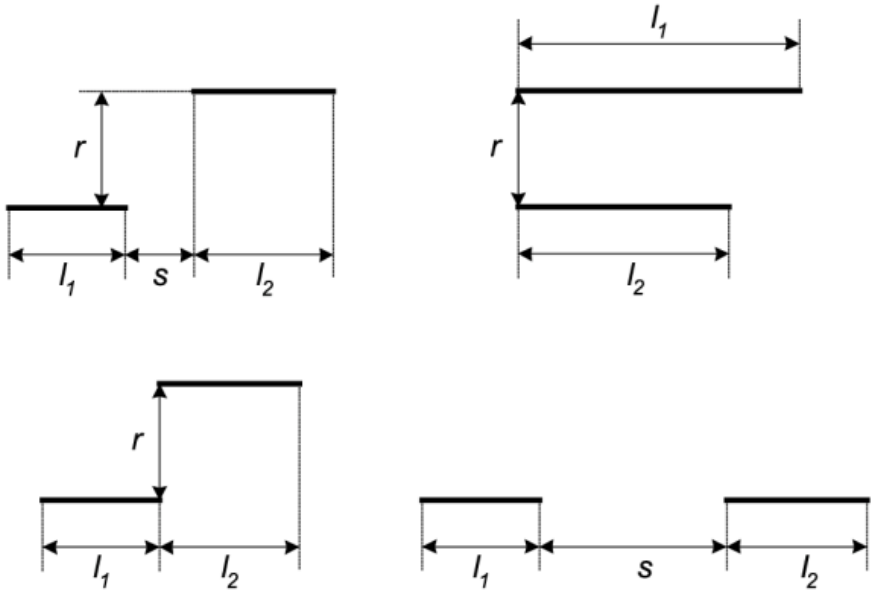
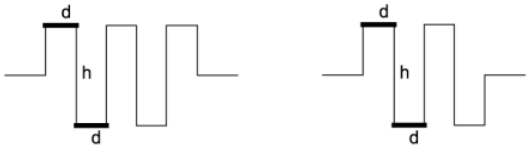
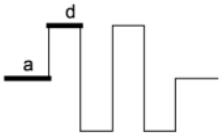
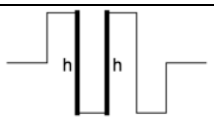


Figure 2.9: 4 typical segment combinations in meander inductor (a) combination 1 (top left) (b) combination 2 (top right) (c) combination 3 (bottom left) (d) combination 4 (bottom right)

The segment combinations of unequal parallel filaments as shown in figure 2.9(a) was expressed by equation (2.4) whilst the situation of filaments have their ends in common perpendicular as shown in figure 2.9(b) was expressed by equation (2.5). The situation of appearing only in case when N-odd for the couple of filaments with length b as shown in figure 2.9(c) was expressed by equation (2.6). The situation of the two segments are in the same axis at the corresponding distance between each other was expressed by equation (2.7).

Figure 2.10 show characteristic situations of all obtained expressions for calculation of the total inductance. The advantage of make a closed form of the expression for inductance of the meander is the designer can get the information on how the geometrical parameters of the inductor influence upon the self-inductance, positive or negative mutual inductance.

$L = 0.002l\left[\ln\left(\frac{2l}{w+t}\right) + 0.50049 + \left(\frac{w+t}{3l}\right)\right]$
$L_{selftot} = 2L_a + 2L_b + NL_h + (N+1)L_d$
$M_1 = \sum_{i=1}^{\frac{N}{2}} (2N+4-4i)\cdot M_{a1}(d,d,h,(2i-2)d)$, for N even  $M_1 = \sum_{i=1}^{\frac{N+1}{2}} (2N+4-4i)\cdot M_{a1}(d,d,h,(2i-2)d)$, for N odd
$M_2 = \sum_{i=1}^{\frac{N}{2}} (2N+2-4i)\cdot M_b(d,d,(2i-1)d)$, for N even  $M_2 = \sum_{i=1}^{\frac{N-1}{2}} (2N+2-4i)\cdot M_b(d,d,(2i-1)d)$, for N odd
$M_3 = 2\cdot M_b(a,a,(N+1)d)$ 
$M_4 = \sum_{i=0}^{N} 4\cdot M_{a1}(a,d,b,id)$ 
$M_5 = \sum_{i=1}^{N-1} (-1)^i \cdot 2\cdot(N-i)\cdot M_c(h,id)$ 

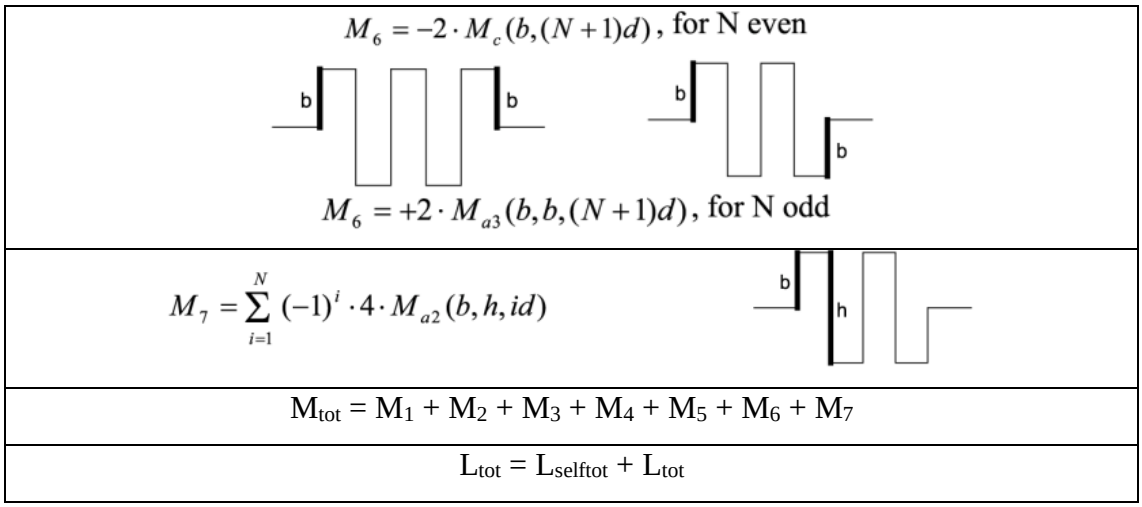


Figure 2.10: presentation of all expression for calculation of total inductance for N-even and N-odd

The inductances of meander inductors can be calculating accurately by using the equations of the self-inductance and mutual inductance as shown in figure 3.6. However, in [26], there already exist expressions in a simple monomial form for the square and octagonal planar inductors which is equation (2.8). This equation for calculation of inductance is very suitable for application in the optimization procedure of the inductor by means of the geometric programming method. The five variables in the equation were represented by the five characteristic geometrical dimensions that determine inductance of the inductor itself. In this case, the a = x_1, h = x_2, N = x_3, d = x_4 and w = x_5.

$$L = \beta \cdot x_1^{a1} \cdot x_2^{a2} \cdot x_3^{a3} \cdot x_4^{a4} \cdot x_5^{a5} \qquad (2.8)$$

In [26], the equation (2.8) has been obtained for spiral inductors by fitting to the measured inductance of a great number of inductors. Meanwhile, in [9], the equation (2.8) has been obtained for meander inductors and the fitting was using the method of the least squares finds parameters of the equation that minimize the sum of squares of the error between accurate data and fitted equation. Hence, the equation (2.9) was the monomial equation for the total inductance, L_{tot} of the meander inductor that gave the least relative error which maximally up to 12 percent.

$$L_{mom} = 0.00266 \cdot a^{0.0603} \cdot h^{0.4429} \cdot N^{0.954} \cdot d^{0.606} \cdot w^{-0.173} \quad (2.9)$$

In equation (2.9), the parameters a, h, N, d and w are in μm and L_{mom} is in nH. The advantage of this equation is simplicity and relatively good accuracy but the disadvantages are the physical sense of the equation is being lost as well as it is no possible to get information on self-inductance or of the mutual inductance of the meander inductor.

2.5 Q Factor

To study the potential of the integration of passive devices on Au-compensated high resistivity silicon substrate, the performance of the meander inductor by using this substrate was evaluated through a parameter called quality factor, Q factor. The Q factor is a dimensionless parameter that indicates the energy loss relative to the amount of energy stored within the system. Thus, the Q factor can be used in defining the performance of an inductor, a capacitor or tuned circuit. Since the basic Q factor formula is based upon the energy losses within the inductor, capacitor or other form of component, the Q factor can be mathematically expressed as formula 2.10 below.

$$Q = \frac{E_{stored}}{E_{lost\ per\ cycle}} \quad (2.10)$$

To calculate the Q factor for an inductor, an inductor is necessary be considered in term of its equivalent circuit. The real-world inductors have significant series resistance and parallel capacitance in term of its equivalent circuit which limiting their lower and upper frequencies respectively. In additional, the series resistance has a strong influence on the performance of the inductor at all frequencies. Thus, the Q factor of the inductor can be defined as the ratio of the reactive part of the impedance Z to the resistive part as formula 2.11 below.

$$Q = \frac{Im\{Z\}}{Re\{Z\}} \quad (2.11)$$

The peak inductor Q factors for early RF integrated circuits (RFICs) had ranged from less than 10 up to 30 or higher in some silicon-on-insulator processes. The even higher Q factors i.e. up to 100 or higher are possible if microelectromechanical (MEMs) techniques are employed or other techniques such as hybrid approaches are adopted were implemented.

2.6 Coplanar Waveguide

Conductor-backed coplanar waveguide (CBCPW) is a one of the common transmission line medium for monolithic microwave integrated circuit (MMIC) applications. CBCPW structure not only can be integrated with high frequency IC circuits easily but also of its simple measurement work. This technology provides a convenient thin-film structure which requiring the coating of only one side of the structure. This have been simplifying the fabrication processing and assembly. In addition, the s-parameter measurement process can be simplified due to the CBCW structure can easily interface with probe station. Figure 3.1 show the cross-section view of CBCPW, a centre signal strip with width, W and two upper grounds which on each side of the signal strip with a signal-to-ground spacing, g.

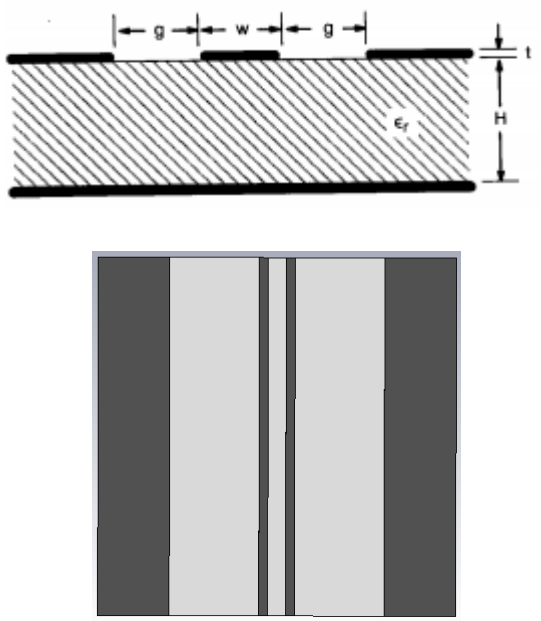


Figure 2.9: (a)cross-section view (top) (b) top view (bottom) of CBCPW structure

2.7 Summary

The high resistivity silicon was obtained by using the deep level doping method and the gold was chosen as the deep level doping element because it need less tight control over dopant concentration and minimal overcompensation effect. In addition, the meander inductor was chosen in this work for the several advantages and its inductance calculation in meander topology which based on Greenhouse 1974 and Grover 1954 was studied in this chapter.

CHAPTER 3

METHODOLOGY

3.1 Introduction

In order to study the potential of integration of meander inductor on Au-compensated high resistivity silicon, the design of meander inductor in coplanar waveguide transition by using this substrate was simulated and analysed. In addition, the inductance calculation for the meander inductor which based on the Greenhouse 1974 and Grover 1954 was verified in this chapter. This inductance calculation method was then used to calculate the inductance value of the meander inductor designed in coplanar waveguide transition. Lastly, the Q factor and inductance of the meander inductors were obtained from the simulation result in order to analyse the performance of the meander inductors.

3.2 Project Implementation Flow

Figure 3.1 show the project implementation flow in design and simulation the meander inductor on gold compensated high resistivity silicon substrate. First, the project has been initialised to design and simulation of high Q inductors on Au-compensated high resistivity silicon substrate. The second step was doing the background research and reading such as studying the conference papers, journal papers or even websites which related to this project. In this stage, the meander inductor topology has been chosen in this project. Next, the inductance calculation in meander topology has been studied in order to make sure it's able to calculate the inductance value even though the parameters of the meander inductor change. The following step was incorporated the coplanar waveguide transition into the meander inductor design as it benefits the design of meander inductor in microwave frequency range. There were three main meander inductors was designed and studied as well as all of them were taken from [27]. Next, the effect of tapering, effect of meander shaped and effect of conformed ground to the Q factor were investigated. From the simulation results, the Q factor of the meander inductors was determined as well as the performance of the inductors also can be evaluated as the Q factor is directly related to its performance. Lastly, the simulation results were the comparison and analysed as well as come out some conclusive discussion.

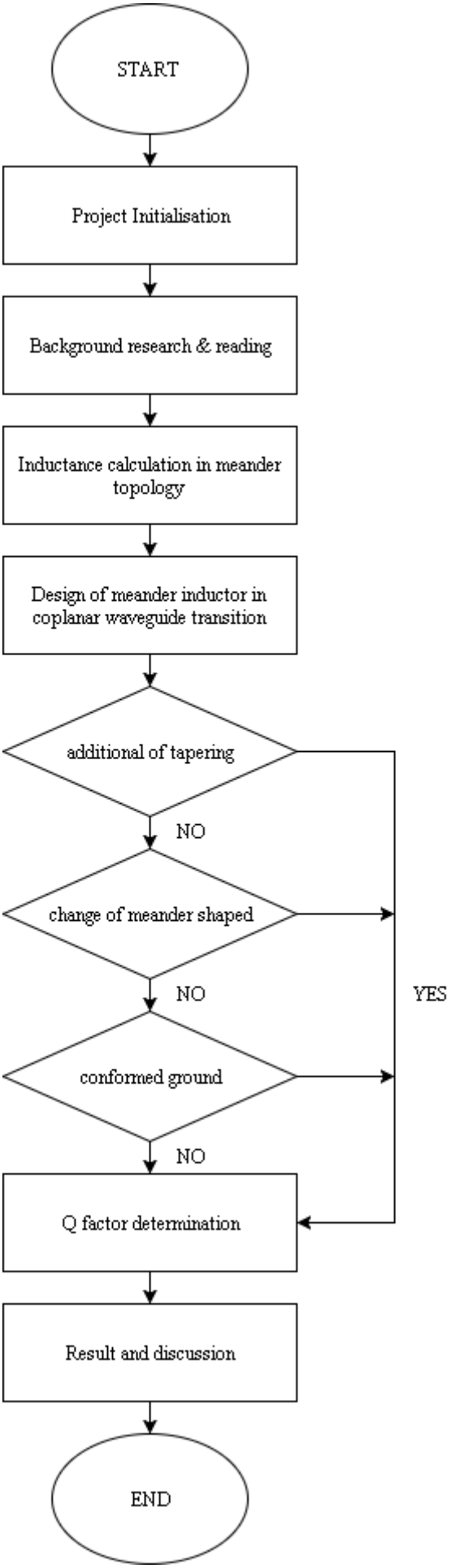


Figure 3.1: project implementation flow

3.3 Inductance Value Calculation

The inductance value of three inductors with N=5, N=8 and N=11 which taken from [26] were calculated in order to demonstrate the validity of results of the developed MATHLAB code by comparing the calculated results and the experimental results taken from [26]. Table 3.1 show the geometrical parameters and measured inductance for the three meander inductors.

Table 3.1: Dimensions of three types of meander inductors and their measured inductances

Name	a (µm)	h (µm)	N	d (µm)	w (µm)	L_{meas} (nH)
Ind No.1	140.0	320	5	80	40	1.5
Ind No.2	162.0	336	8	48	24	2.0
Ind No.3	158.5	343	11	34	17	2.5

These dimensions are used in the calculation of the self-inductance and the mutual inductance. The calculation was done by using the formula (2.1) and formula (2.2) as mentioned in section 2 as well as these formulae in figure 2.10.

$$L = 0.002l\left[\ln\left(\frac{2l}{w+t}\right) + 0.50049 + \left(\frac{w+t}{3l}\right)\right] \quad (2.1)$$

$$L_{selftot} = 2L_a + 2L_b + NL_h + (N+1)L_d \quad (2.2)$$

The formulae (2.1) and (2.2) were used to calculate the total self inductance of the meander inductor whereas the formula in figure 2.10 were used to calculate the mutual inductance of the meander inductor. The calculation results were compared with the measurement results in [26] to verified the validation of the developed program.

Figure 3.2 show the meander inductors with N=5,8 and 11 by using the three dimensions in table 3.1.

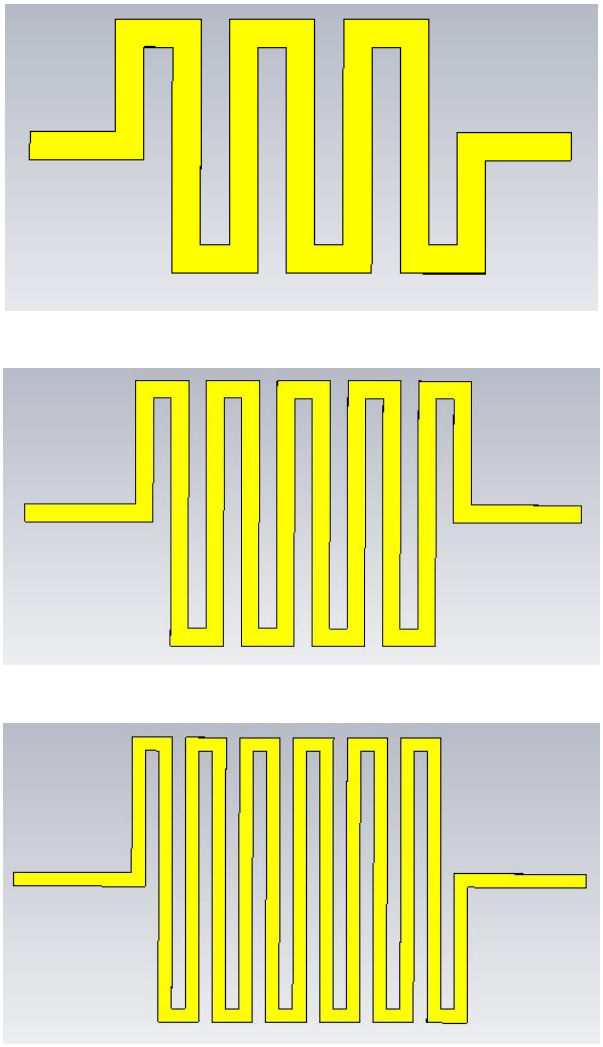


Figure 3.2:meander inductors with (a) N=5 (top) (b) N=8 (middle) (c) N=11 (bottom)

The program used to calculate the self-inductance and mutual inductance was written in the program language MATLAB and the inductance simulated results for the three types of the meanders are given in table 3.2.

Table 3.2: calculation results of the meander inductor

Name	$L_{selftot}$ (nH)	L_{tot} (nH)	Monomial expression (nH)	Measured inductance (nH)
Ind No.1	1.48091	1.50914	1.609747	1.5
Ind No.2	2.46285	1.95493	2.082738	2.0
Ind No.3	3.45115	2.37379	2.449753	2.5

The inductance calculation results by using MATLAB was in good agreement with the measured inductance values. The percentage error of the three meander inductors were 0.61%, 2.25% and 5.05% respectively. This justify that this program can been used to calculate the inductance of the meander inductor.

3.4 Coplanar Waveguide

Since the fifth step of the project implementation flow was designing the meander inductor in coplanar waveguide transition, the CPW structure was designed and simulated in order to study its characteristics. In [28], the width of the centre signal strip was 50 µm since the difficulty of the line-probing increases significantly if the value less than it. Meanwhile, the W_g was chosen to be 250 µm as it is large enough to provide sufficient space for probes of different pitch to be used during experimental measurement. In addition, the signal-to-ground spacing was 25 µm as it is in the logical intermediate range of $20 < g < 30$ µm which based on the experimental results in [28]. Furthermore, the length of the CPW was 1000 µm which is large enough to design the meander inductor in CPW transition and the table 3.3 show all the parameters of the CPW.

Table 3.3: CPW parameters

Parameter	Value (um)
Ground strip width	250
Signal strip width	50
GSG strip separation	25
Au-compensated HR-Si thickness	675
SiO_2 thickness	0.02
Aluminium thickness	1

The CPW was then simulated using CST STUDIO SUIT and the structure of the CPW was shown in figure 3.3.

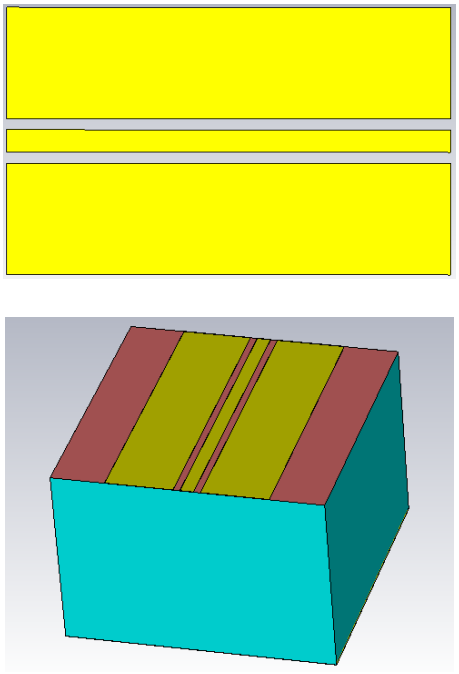


Figure 3.3: (a) top view (top) (b) side view (bottom) of the structure of the CPW

The simulation of the CPW was performed up to 40GHz. Figure 3.4 shows the S_{11} of the CPW whereas figure 3.5 shows the S_{21} of the CBCPW. From the simulation results, the return loss and insertion loss of the CPW was low over the range of the 40GHz. The S_{11} of the CPW was -38.037955 at 20GHz whereas the S_{21} of the CPW was -0.085343481dB at 20GHz. This justify that there is no much negative impact as incorporation of the CPW transition into the design of the meander inductor.

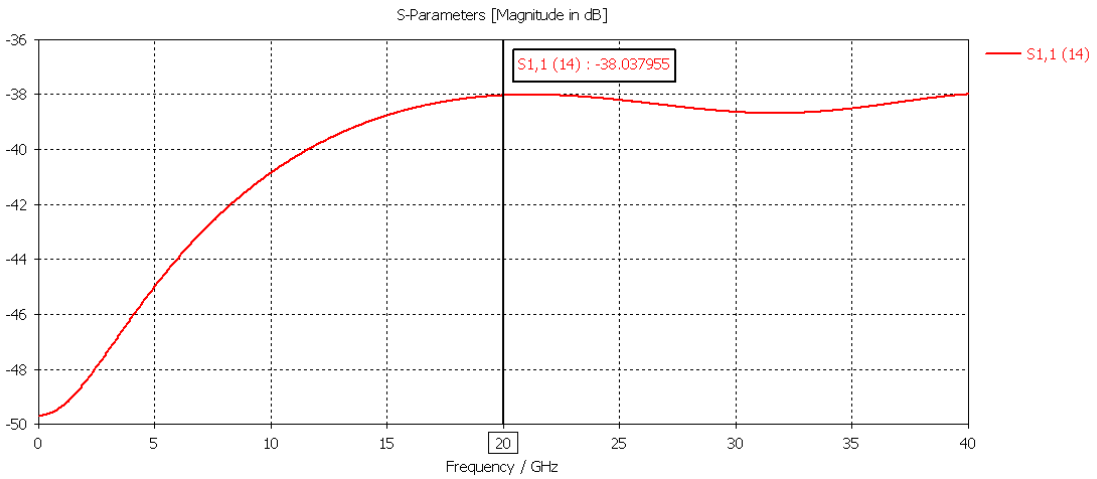


Figure 3.4: S11 of the CBCPW

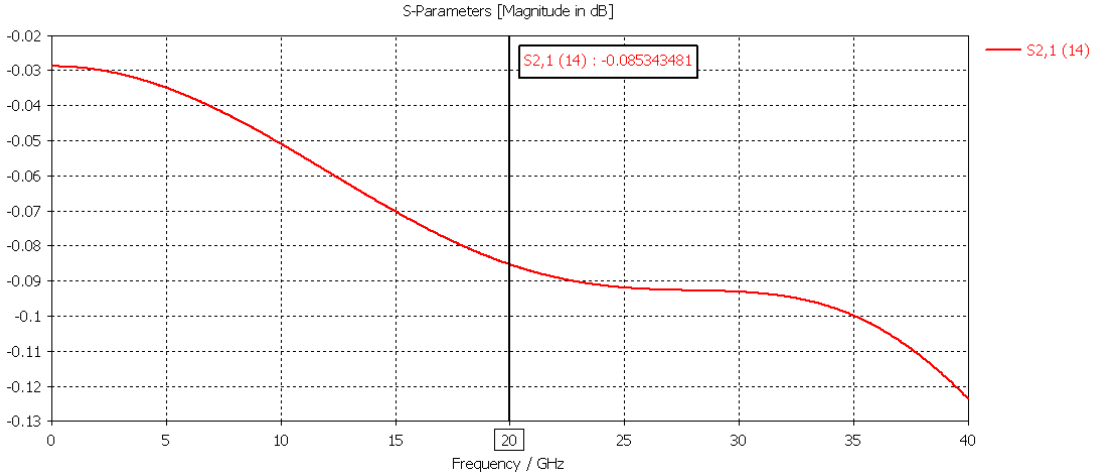


Figure 3.5: S21 of the CBCPW

3.5 Simulation

Figure 3.6,3.7 and 3.8 show the design of the meander inductor with N=5, 8 and 11 in coplanar waveguide transition respectively. The three meander inductors were simulated using CST STUDIO SUIT, the Q factor and inductance of the meander inductors were then analysed and compared.