A STUDY OF CAPACITANCE-VOLTAGE CHARACTERISTICS FOR METAL-OXIDE-SEMICONDUCTOR STRUCTURE ON GOLD-COMPENSATED HIGH RESISTIVITY SILICON

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by

TAN JIA YIING

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LIST OF SYMBOLS

C_{FB}	MOS flatband capacitance
C_{HF}	High frequency capacitance
C_{LF}	Low frequency capacitance
C_{MOS}	Total capacitance for high resistivity silicon
C_{ox}	Oxide capacitance
$C_{s,DD}$	Deep-depletion capacitance of the semiconductor
$C_{s,HF}$	High frequency capacitance of the semiconductor
$C_{s,LF}$	Low frequency capacitance of the semiconductor
E_g	Intrinsic band gap energy
G_{MOS}	Total conductance for high resistivity silicon
K_{ox}	Relative permittivity of silicon dioxide
K_s	Relative permittivity of silicon
L_D	Extrinsic Debye length
L_{Di}	Intrinsic Debye length
N_d, N_a	Concentration of doping density
N_{ss}	Interfacial density of singly oxide charge
Q_f	Fixed oxide charge
Q_{inv}	Inversion layer charge
Q_{it}	Interface trapped charge
Q_m	Mobile ionic charge
Q_{ot}	Oxide trapped charge
U_s, U_F	Normalized potentials
V_{FB}	Flat-band voltage
V_G	Gate voltage
V_T	Threshold voltage
V_t	Thermal voltage
n_i	Concentration of intrinsic silicon density

t_{ox}	Thickness of silicon dioxide
x_d	Depletion width
ε_0	Permittivity of vacuum
ε_{ox}	Permittivity of silicon dioxide
$\varepsilon_{s,dd}(\phi_s)$	Relationship between the potential at the surface and the field under deep depletion
$\varepsilon_{s,eq}(\phi_s)$	Relationship between the potential at the surface and the field under thermal equilibrium
ε_s	Permittivity of silicon
τ_D	Response time of majority carrier
ϕ_f	Bulk fermi potential
ϕ_m	Work function of aluminium
ϕ_s	Work function of semiconductor
$F(U_s, U_F)$	Dimensionless semiconductor surface electric field
$F(v_s, u_B)$	Dimensionless electric field
T	Temperature
Y	Admittance for high resistivity silicon
k	Boltzmann constant
q	Electric charge
μ	Electron mobility
ρ	Resistivity of a silicon substrate
χ	Electron affinity
ω	Angular frequency

LIST OF ABBREVIATIONS

BST	Barium Strontium Titanate
CPW	Coplanar Waveguide
C-V	Capacitance-Voltage
Cz-Si	Czochralski-Silicon
Fz-Si	Float-Zone Silicon
HRS	High Resistivity Silicon
HWCVD	Hot-Wire Chemical Vapour Deposition
LPCVD	Low-Pressure Chemical Vapour Deposition
LRS	Low Resistivity Silicon
MMIC	Monolithic Microwave Integrated Circuit
MOS	Metal-Oxide-Semiconductor
Nc-Si SPL	Nanocrystalline Silicon Surface Passivation Layer
nMOS	n-type Metal-Oxide-Semiconductor
pMOS	p-type Metal-Oxide-Semiconductor
PSC	Parasitic Surface Conduction
SHF	Super High Frequency
Si-SiO_2	Silicon-silicon dioxide
SOA	Silicon-on-Anything
SOI	Silicon-on-Insulator

KAJIAAN CIRI KAPASITANS-VOLTAGE BAGI STRUKTUR SEMIKONDUKTOR LOGAM-OKSIDA TERHADAP EMAS-KOMPENSASI SILICON KERINTANGAN TINGGI

ABSTRAK

Matlamat untuk mencapai mikrogelombang kehilangan pengecilan rendah dalam sistem komunikasi tanpa wayar berkelajuan tinggi adalah penting dalam kemajuan evolusi teknologi. Pembawa bebas elektron dan pengaliran permukaan parasit menghalang kemajuan dalam bidang perhubungan wayarles. Kebelakangan ini, satu kaedah baru yang menggunakan pengedopan berperingkat dengan unsur emas supaya menghasilkan substrat silikon kerintangan tinggi untuk aplikasi gelombang mikro telah berjaya. Kini, tidak ada model litar setara dan persamaan matematik untuk mengelakan ciri kapasitans-voltan bagi struktur semikonduktor logam-oksida pada emas-kompensasi substrat silikon kerintangan tinggi. Siasatan terhadap ciri-ciri kapasitans-voltan untuk struktur semikonduktor logam-oksida pada kerintangan rendah, kerintangan tinggi dan emas-terkompensasi substrat silikon telah dijalankan. Persamaan matematik yang sesuai untuk mewakili keluk kapasitans-voltan silikon kerintangan rendah telah dinilai. Model litar setara silikon kerintangan tinggi untuk frekuensi rendah dan tinggi telah ditentukan dengan MATLAB dan disahkan melalui SILVACO. Model litar setara dan persamaan silikon kerintangan tinggi telah ditentukan dengan berjaya. Data eksperimen emas-kompensasi silikon kerintangan tinggi dibandingkan dengan data teori silikon kerintangan tinggi. Berdasarkan hasil perbandingan keluk kapasitans-voltan, model litar setara bagi emas-terkompensasi kerintangan tinggi silikon didapati berbeza daripada silikon kerintangan tinggi.

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ABSTRACT

The goal to achieve low microwave attenuation loss in a high-speed wireless communication system is crucial for the advancement of technology evolution. Background carrier and parasitic surface conduction hinder the progression of a wireless system to perform better. Recently, a new method using deep-level doping compensation with the gold element to create high resistivity silicon substrate for microwave application is successful. Currently, there is no existing equivalent circuit model and mathematical equations to classify capacitance-voltage characteristic for a metal-oxide structure on gold-compensated high resistivity silicon substrate. An investigation of capacitance-voltage characteristics for the metal-oxide-semiconductor structure on low resistivity, high resistivity and gold-compensated silicon substrates are carried out. The suitable mathematical equations to represent capacitance-voltage curves of low resistivity silicon is evaluated. High resistivity silicon equivalent circuit models for low and high frequencies are determined in MATLAB and verified in SILVACO. The equivalent circuit models and equations of high resistivity silicon are determined successfully. Experimental data of Au-compensated high resistivity silicon is compared and analysed with theoretical high resistivity silicon data. Based on the comparison result of both C-V curves, the equivalent circuit of gold-compensated high resistivity silicon is not same as the high resistivity silicon.

CHAPTER 1

INTRODUCTION

1.1 Research Background

In the blooming era of wireless technology, the demand for the high-speed wireless communication system for data transmission is noticeably increasing. A suitable and reliable high resistivity substrate is crucial in manufacturing high frequency application's chips typically in monolithic microwave integrated circuits (MMICs). MMIC is a microwave circuit that consists of active and passive components fabricated on a semiconductor substrate. The application of MMIC is widely seen in cellular, radio and satellite systems, ranging between 300MHz to 300GHz [1]–[3].

The existence of MMICs can be related to transmit-receive (TR) module design, which is based on a government-funded program for an aircraft phased-array antenna in 1964 [4]. The poor performance of silicon as microwave substrate was replaced by III-V material, which is the gallium arsenide to solve the lossy substrate issue. Typical III-V materials found these days are the aforementioned gallium arsenide (GaAs), gallium nitride (GaN) and indium nitride (InN) [5]–[7]. It is well known that III-V materials have wider energy bandgap compare to silicon. Moreover, it shows intrinsic concentration property with a low concentration of carriers [8]. The benefits of using III-V materials include suppression of electrical current conduction, which consequently reduces the parasitic effect [9].

Although III-V materials naturally possess semi-insulating properties, these materials are not free of defects. The lattice mismatch problem causes the decrease in material quality, and high fabrication cost is perceived as an undesirable factor. Since the

general industrial requirement is to minimise development time, yield high volume and cheaper wireless products to the market, silicon is still an excellent choice for it mature development technology and capability of high volume production [9], [10]. Besides, silicon possesses high thermal conductivity and frequency-independent permittivity that suitable for usage in microwave substrate [11].

During the production of monocrystalline silicon, unavoidable contamination can occur which yield decrease in substrate quality. The originate of background carriers causes significant current conduction paths in microwave application that subsequently lead to substrate losses. Technologies of silicon-on-anything (SOA) and silicon-on-insulator (SOI) are introduced to solve the background carrier issue, but the thermal breakdown is a problem that required complex solution [9]. High resistivity silicon (HRS) is an alternative solution to reduce background carrier concentration in the substrate [12].

HRS with a resistivity at least $3\mathrm{k}\,\Omega\cdot\mathrm{cm}$ can be used in a wireless system operating at high frequency due to its properties of low-loss, high thermal conductivity and permittivity when passivated [13], [14]. The existence of background free carriers in a silicon substrate is not the only issue causing an increase in attenuation loss under high frequency environment with bias application. The surface resistivity of silicon will decrease due to the formation of charges/ charge carriers in the accumulation/ inversion regime under coplanar waveguide (CPW). At high frequency environment, this effect is known as parasitic surface conduction (PSC), where it will cause CPW attenuation losses at the silicon-oxide interface. This additional microwave loss is due to the formation of charges at the mentioned regimes, and it is bias-dependent [9].

Recently, Hashim *et al.* [15] managed to tackle both issues by using a method called deep-level doping compensation with elemental gold (Au). In her work, Au is

introduced via ion-implantation and activated through subsequent annealing procedure. As a result, a substrate resistivity of $70k\Omega \cdot cm$ was achieved using a nominal $50\Omega \cdot cm$ silicon substrate [15]. CPW fabricated on the compensated substrate showed a bias-independent attenuation loss, with a constant value of 0.2 dB/mm at 40GHz for bias voltage ranging between -6V to +6V, where inversion and accumulation were said to occur [16]. Therefore, Au-compensated HRS substrate is a potential material to be used for MMICs production in the future as a microwave substrate.

1.2 Problem Statement

There are a few well-known materials such as III-V materials, SOA and SOI are commonly used in MMICs' fabrication. Even though all these materials seem promising, but still allow rooms for improvement. HRS substrate is an alternative material used as a microwave substrate [12][17]. It can decrease attenuation loss by suppressing background carrier concentration, but the substrate still suffers from PSC effect due to CPW under bias-condition [13][18].

The existence of background carrier and PSC issues in silicon substrate has hindered the development process. Recently, by deep-level doping compensation with Au into silicon substrate has successfully yielded a new material called Au-compensated HRS [16]. Since it is a new material, there is no any existing equivalent circuit model and mathematical equations to classify it theoretically. Therefore, in this project, a study is carried out to compare between HRS with Au-compensated HRS by using Metal-Oxide-Semiconductor (MOS) structure. The capacitance-voltage (C-V) characterization of capacitors on both HRS and Au-compensated HRS will be investigated.

Currently, almost all the circuit models and equations available today are related to low resistivity silicon (LRS). Besides, the requirement to represent C-V for HRS in an equivalent circuit model and equations are crucial before proceed to study the C-V characterization of HRS. Furthermore, once the equivalent circuit model and equations of MOS structure C-V for HRS are determined, it can be used to investigate the C-V characteristic of Au-compensated HRS.

1.3 Objectives of Research

The objectives of this project are listed below:

1. To study the C-V behaviour of MOS structure on low resistivity silicon substrate.
2. To study the C-V behaviour of MOS structure on high resistivity silicon substrate.
3. To provide a comparative study of the theoretical C-V curve of HRS and experimental C-V curve of the Au-compensated silicon substrate based on MOS structure.

1.4 Scope of Research

This research is a purely software based project with only considering the simulation of C-V characterization for MOS structure. Fabrication of MOS capacitor is not covered in this study due to the lack of equipment and technology in the school laboratory. The simulation tools used in this project are MATLAB and SILVACO. In this project, a p-type MOS C-V characterization is simulated according to mathematical equations defined by researchers. The conditions such as low frequency, high frequency, the effect of various phosphorous doping concentration and different equivalent circuit models of LRS and HRS MOS capacitor are included in the C-V characterization consideration. Lastly, an experimental C-V curve of Au-compensated HRS is compared

with a theoretical C-V curve of HRS. The experimental data (fabrication C-V suppression data) for this project is obtained from Dr Nur Zatil Ismah Hashim, at the Southampton Nanofabrication Centre in 2015.

1.5 Thesis Outline

This thesis is organised into five chapters, in Chapter 1, this thesis begins with an introduction of this project with some research background. In this chapter, problem statement, objectives, scope and thesis outline are also included. In Chapter 2, a literature review is presented with the study on MMICs, HRS, Au-compensated HRS and MOS C-V characterization. For Chapter 3, a methodology of this project is explained in detail in this part by using flow charts and equations. Next, the C-V simulation results are analysed and described in depth in Chapter 4. Last but not least, in Chapter 5, which is the final chapter, a summary of this research finding from the beginning till the end is concluded. The limitations and suggestion for future works are also included in the project.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, the literature review including sources from the various thesis, journals, conference papers, books and websites. Firstly, a short review is done on the development of silicon substrate in wireless technology and issues present at microwave frequency. Secondly, methods used to suppress PSC effect are summarised. Next, fundamental MOS capacitor theory is explained briefly, which include mode of operation, charges associated with MOS system and C-V techniques.

The natural phenomena of background free carriers present in the semiconductor are unavoidable during monocrystalline Si growth in the Czochralski process. It is very problematic for super high frequency (SHF) application. A few methods have been proposed to fabricate HRS, such as Float-zone silicon (Fz-Si), silicon-on-anything (SOA), silicon-on-insulator (SOI) and proton implantation [9]. Although resistivity of the semiconductor has increased by using these methods, the existence of PSC effect causes the effective resistivity of substrate degraded. This issue is due to the formation of charges under CPW structure such as spiral inductors on a silicon substrate at high frequency application [19], [20].

Transition element impurities such as Ag, Au, Mn and V can be used to produce HRS by deep-level doping explained by Mallik *et al.* [21]. By suppressing background free carrier and PSC effect, deep-level doping compensation technique can use to compensate charge formation in low resistivity Czochralski silicon (Cz-Si) substrates. It acts as trapping platform in bulk Si substrate by introducing high density of traps at silicon

surface proved by Hashim *et al.* [16]. Besides, Au-compensated HRS able to accomplish high-quality factor Q material [22]. In addition, uniform HRS can be easily achieved without specific control over the partitioning of Au compensating deep impurity concentration [21] [23]. Therefore, deep-level doping with Au is useful to increase the resistivity of silicon.

2.2 Parasitic Surface Conduction Effect

The effective resistivity of HRS is lower at high frequency due to CPW attenuation loss [20]. This microwave attenuation loss of HRS is related to parasitic surface conduction (PSC) effect at microwave frequency range. Reyes *et al.* [24] claimed that when insulator such as SiO_2 was subjected to time varying signal, attenuation loss is caused by internal polarisation of the material. One year later, in 1995, Reyes *et al.* [14] confirmed that presence of accumulation or inversion caused coplanar waveguide (CPW) attenuation loss to increase.

After four years, in 1999, Wu *et al.* [25] demonstrated Reyes's hypothesis regarding the low resistivity region at Si-SO_2 interface was due to an accumulation or inversion region. Wu *et al.* proposed to replace a continuous layer of SiO_2 with a non-continuous oxide pattern right below the CPW in Figure 2.1. The proposed structure successfully reduced the loss from 18 to 3 dB/cm at 30 GHz. In the same year, Gamble *et al.* [26] suggested another method by introduced a high density of traps in between continuous Si-SiO_2 interface layer with an LPCVD polycrystalline silicon layer in Figure 2.2. By using this approach, the attenuation loss was successfully reduced to 1.08 dB/cm at 30 GHz. In 2002, after Gamble's work, Lue *et al.* [27] deposited BST thin films on HRS, and low insertion loss was obtained.

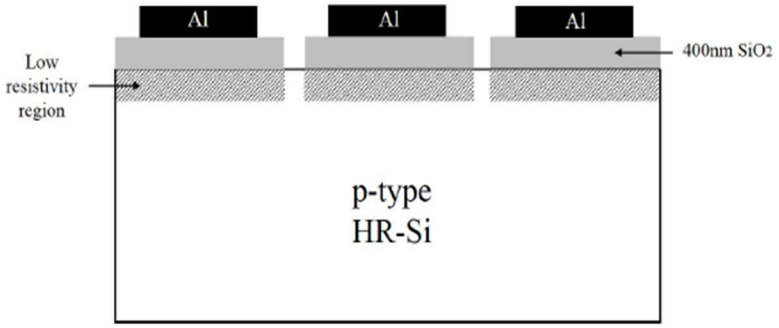

Figure 2.1 Non-continuous SiO_2 layer [25].

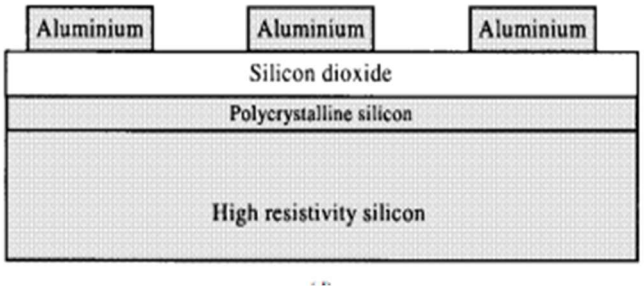

Figure 2.2 Polycrystalline silicon layer in between Si-SiO_2 interface [26].

In addition, in 2003, according to Jansman *et al.* [28], a high density trap region can be introduced into a silicon substrate by bombardment of Argon (Ar) atoms to suppress PSC. This technique will have a formation of an amorphous Si layer in between Si-SiO_2 interface layer. It caused mobility of charge carriers to decrease heavily and increase the effective substrate resistivity. Follow by CPW configured baluns by using implantation dose of 10^{15} cm^{-2} mentioned by Jansman, an attenuation value of 0.2 dB/mm was obtained at 30 GHz [29]. After two years, in 2005, Spirito *et al.* [11] demonstrated an attenuation loss of 0.15 dB/mm at 30 GHz by using the same dose for Ar-implantation in DIMES-04.

Apart from Ar-implantation technique, in 2008, Li *et al.* [30] suggested nanocrystalline silicon surface passivation layer (nc-Si SPL) by using hot-wire chemical vapour deposition (HWCVD). Then, in 2011, Chen *et al.* [31] and Wang *et al.* [32]

respectively shown that by using HWCVD technique to form a 100 nm and 400 nm thick nc-Si SPL obtained an attenuation loss less than 1.05 dB/cm and 0.69 dB/cm at frequency 20 GHz respectively. The result showed lower attenuation loss due to thicker nc-Si SPL thickness.

Until now, techniques mentioned above focus on introducing high density of traps by inserting polysilicon, Ar-implantation and nanocrystalline silicon in between Si-SiO_2 interface. Although the attenuation loss was reduced as the time passes, the current thermal stability issues still connected with amorphous silicon. Recently, in 2014, Hashim *et al.* [16] demonstrated using deep-level doping compensation with Au to suppress PSC effect. The result obtained with an attenuation value of 0.2 dB/mm at 40 GHz. The benefits of this method were the reduction of complexity and low fabrication costs.

The methods to suppress PSC effect at high frequency application as mentioned previously are summarised in Table 2.1. Based on the table, lowest attenuation is achieved by Spirito *et al.* but not at the highest frequency. By comparison, the best approach is by deep-level doping compensation with Au with low attenuation loss at highest microwave frequency value. This method is simpler compared to the rest and lower cost of implementation.

Table 2.1 Summary of comparison between methods reviewed to suppress PSC effect at microwave range frequencies.

Author	Method Review	Attenuation loss (dB/mm)	Frequency (GHz)
Yunhong Wu, H.S. Gamble, B. M. Armstrong, V.F. Fusco, J.A.C. Stewart [25]	Implement noncontinuous SiO2 layer	30	30
H.S. Gamble, B.M. Armstrong, S.J.N. Mitchell, Y. Wu, V.F. Fusco, J.A.C. Stewart [26]	Continuous oxide as passivation layer and a high density of traps in between Si-SiO2 interface with LPCVD polycrystalline silicon layer	10.8	30
Hang-Ting Lue, Tseung-Yuen Tseng, Guo-Wei Huang [27]	Depositing 300-nm thick polysilicon film below a 100-nm thick SiO2 layer	Not stated	Not stated
E. Valletta, J. Van Beek, A. Den Dekker, N. Pulsford, H.F.F. Jos, L.C.N. de Vreede, L.K. Nanver, J.N. Burghartz [29]	Introduce a high density trap region by Ar-implantation	0.2	30
M. Spirito, F. De Paola, L. Nanver, E. Valletta, B. Rong, B. Rejaei, L. de Vreede, J. Burghartz [11]	Fabricate coplanar lines on HRS along with DIMES-04 and produced a thin amorphous layer with Ar-implantation technique	0.15	30
C.-J. Chen, R.-L. Wang, Y.-K. Su, T.-J. Hsueh [31]	Deposition of nanocrystalline silicon layer using hot-wire chemical vapour deposition with thickness 100 nm	10.5	20
R.-L. Wang, Y.-K. Su, C.-J. Chen, T.-J. Hsueh [32]	Increased thickness of nanocrystalline silicon layer to 400 nm	6.9	20
Nur Z. I. Hashim, Ahmed Abuelgasim, Cornelis H. de Groot [16]	Deep-level doping compensation with Au	0.2	40

2.3 Au-compensated High Resistivity Silicon

Attenuation loss due to background carriers can be suppressed by using HRS, but an additional microwave loss due to CPW attenuation degrade the overall substrate's resistivity. These issues are tackled by deep-level doping compensation method to enhance the performance of silicon substrate. Deep-level traps are introduced into silicon band gap by using this compensation method, through ion implantation and subsequent annealing process [15]. In 2013, Hashim *et al.* [16] showed that resistivity of Au-compensated HRS was increased up to $70\text{k}\Omega \cdot \text{cm}$ by using a nominal $50\Omega \cdot \text{cm}$ silicon substrate. Later in 2014, by using Au-compensated HRS as microwave substrate, it can achieve an attenuation loss of 0.2dB/mm at 40GHz. This method has shown that deep-level doping compensation with gold element method can suppress bias-dependent PSC at the silicon-silicon dioxide ($Si\text{-}SiO_2$) interface.

According to Hashim *et al.* [16], the CPW attenuation is bias-dependent for Float-zone silicon whereas it is bias-independent for Au-compensated HRS as shown in Figure 2.3. Based on the figure, the CPW attenuation is the higher at accumulation and inversion regions compare to depletion region. The higher loss in both accumulation and inversion regions is due to the formation of surface conduction layer at the silicon-silicon dioxide interface whereas depletion of charges in depletion region causes the lowest loss. The lower mobility of holes compares to electron causes attenuation in inversion lower compares to accumulation. CPW attenuation for Au-compensated HRS is maintained at constant value regarding the bias voltage from -6V to +6V. Furthermore, it attenuation loss is the lowest compared to Float-zone silicon. The result shows that Au-compensated HRS is a bias-independent potential microwave substrate material.

Hashim *et al.* [16] suggested C-V measurement for Au-compensated HRS and Float-zone silicon can be used to analyse the attenuation measurement result in Figure 2.3. Based on Figure 2.4, the C-V measurement is done in high frequency condition with frequency at 1MHz. The shape of Float-zone C-V curve exhibits typical high frequency C-V behaviour with minimum inversion capacitance and maximum accumulation capacitance for the pMOS capacitor structure. Moreover, the present of fixed oxide and interface trapped charges in silicon-silicon dioxide interface layer cause C-V curve for Float-zone silicon shifted to the left and stretched out. Besides, for Au-compensated HRS C-V curve show non-responsive C-V with a horizontal line. The extremely high resistivity property of Au-compensated HRS able to prevent a reduced amount of free carriers in response which leads to unusual C-V behaviour in high frequency.

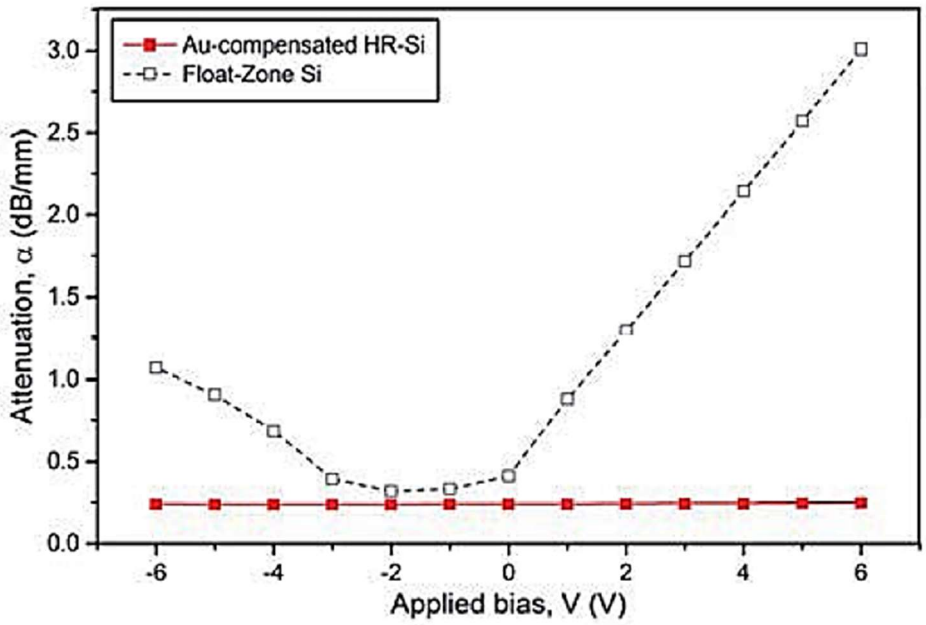

Figure 2.3 Comparison of CPW attenuation losses for Au-compensated HRS and Float-zone silicon [16].

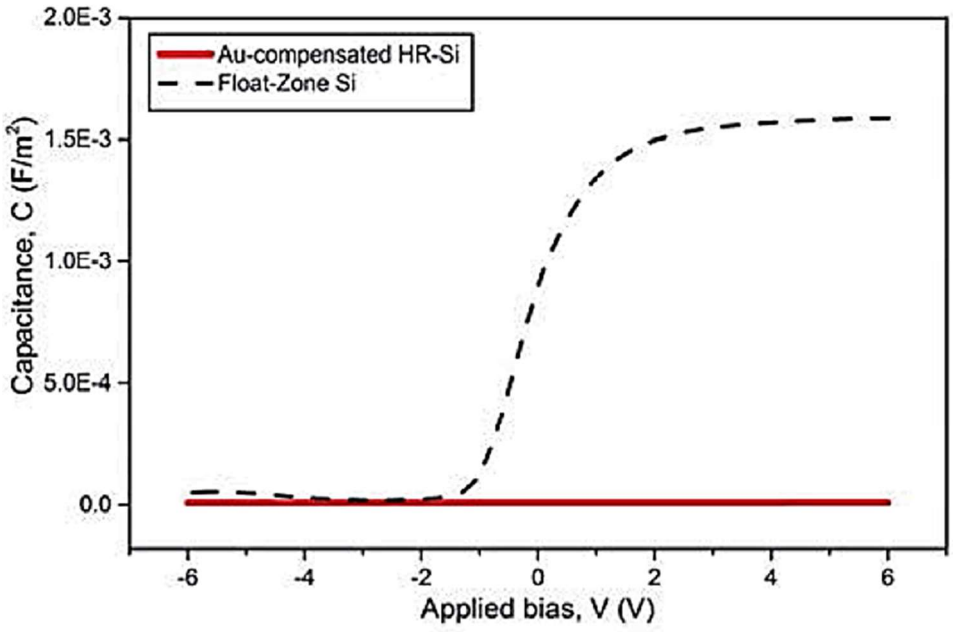

Figure 2.4 Comparison of Au-compensated HRS and Float-zone silicon C-V curves at 1MHz [16].

2.4 MOS Capacitor Structure

Metal-oxide-semiconductor (MOS) capacitor is an effective test structure to characterise devices and extract information [33]. It is composed of a metal electrode (gate), an insulator film (SiO_2) and a semiconductor substrate [34]. An additional metal layer can be formed below the substrate to have an Ohmic contact as shown in Figure 2.5. The benefit of this simple structure can be used to analyse elements in the integrated circuit of greater complicated components.

There are two types of MOS capacitors, such as pMOS and nMOS. The pMOS capacitor substrate is doped with donors (Group V elements: Phosphorus, Arsenic, Antimony) whereas nMOS capacitor substrate is doped with acceptors (Group III elements: Boron, Aluminium, Gallium) [35]. The majority and minority carriers in both MOS capacitors can be categorised as shown in Table 2.2.

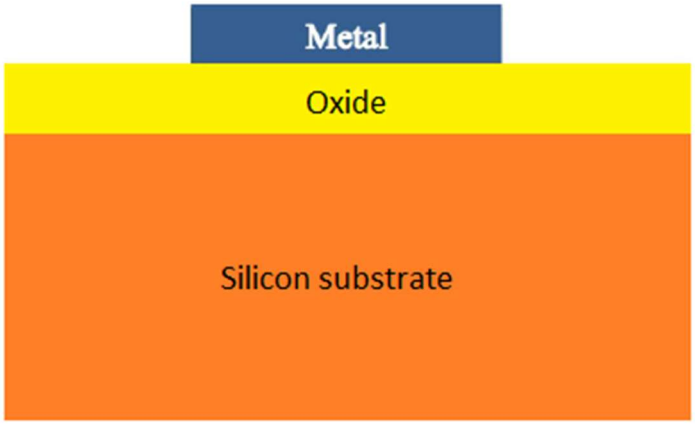

Figure 2.5 MOS Capacitor cross-sectional view [9].

Table 2.2 Minority and majority carriers in MOS capacitor

	Majority carriers	**Minority carriers**
pMOS (n-type doped substrate)	Electrons	Holes
nMOS (p-type doped substrate)	Holes	Electrons

2.5 MOS Capacitor Operational Region

When a voltage is applied to the gate terminal of nMOS or pMOS capacitors, three basic operating regions such as accumulation, depletion and inversion can be observed from MOS capacitor at different bias voltages [36]. Accumulation occurs when large negative gate voltage, V_G is applied to the metal contact of p-type substrate (nMOS). Majority carrier (holes) will be attracted to the Si-SiO_2 interface [36]. The exact range for accumulation to occurs when applied V_G is less than flatband voltage, V_{FB}. Whereas for n-type substrate (pMOS), accumulation happens in positive V_G where it is large than V_{FB}. This is due to different dopants is used in nMOS and pMOS [36].

In the case of nMOS, depletion occurs when V_G is changed from negative to slightly positive, holes will be pushed away from the Si-SiO_2 interface into the substrate [36]. When V_G is same as V_{FB}, now the semiconductor is depleted of mobile carriers at

the interface and a layer of ionised acceptor ions is formed in the space charge region [36]. The exact range for depletion to occur is between flatband voltage and threshold voltage. For both nMOS and pMOS, depletion happens in the same voltage range [36].

Furthermore, inversion occurs as the positive V_G is increased beyond threshold voltage, V_T, minority carriers will be attracted to the interface, which forms a negatively charged inversion layer and depletion-layer in nMOS [36]. Whereas for pMOS, as the negative V_G is increased beyond V_T, minority carrier of positively charged will be attracted to the interface, and a positively charged inversion layer is formed [36]. Table 2.3 shows the summary of operational regions according to the applied gate voltage for both nMOS and pMOS.

Table 2.3 MOS capacitor operation regions when the gate voltage is applied.

nMOS capacitor region	**Conditions for both MOS**		**pMOS capacitor region**
Accumulation	$V_G < V_{FB}$	$V_G > V_{FB}$	Accumulation
Depletion	$V_{FB} < V_G < V_T$	$V_{FB} > V_G > V_T$	Depletion
Inversion	$V_G > V_T$	$V_G < V_T$	Inversion

2.6 Ideal Capacitance of MOS structure

Energy band diagram provides a good understanding of MOS capacitor. Each bias condition of a pMOS capacitor as shown in Table 2.3 and illustrate with Figure 2.6, can be understood based on the silicon bands bending effect in energy band diagram shown in Figure 2.7.

During accumulation, a positive bias voltage is applied to the metal contact. This positive bias voltage attracts majority carriers to the surface meanwhile the conduction band, E_C bends downward to Fermi level, E_F [9]. As the positive bias voltage decreases to zero potential, the flatband condition is reached. Flatband is a condition where the energy band is flat as shown in Figure 2.8. In this condition, it is indicating that the metal

work function, ϕ_m is equal to semiconductor work function, ϕ_s with no energy difference. When a slight negative bias voltage is applied, depletion occurs and the silicon bands bend slightly upward. As the negative bias voltage is increased beyond the threshold voltage, inversion occurs and the silicon bands bend significantly upward which causes the intrinsic level, E_i crosses over E_F[9].

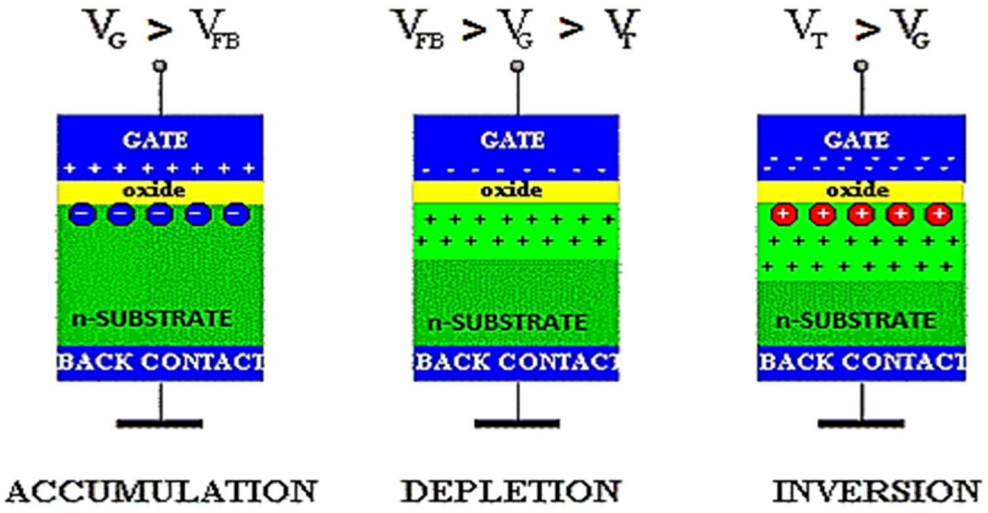

Figure 2.6 The operation regimes of a pMOS capacitor at different bias voltage [36].

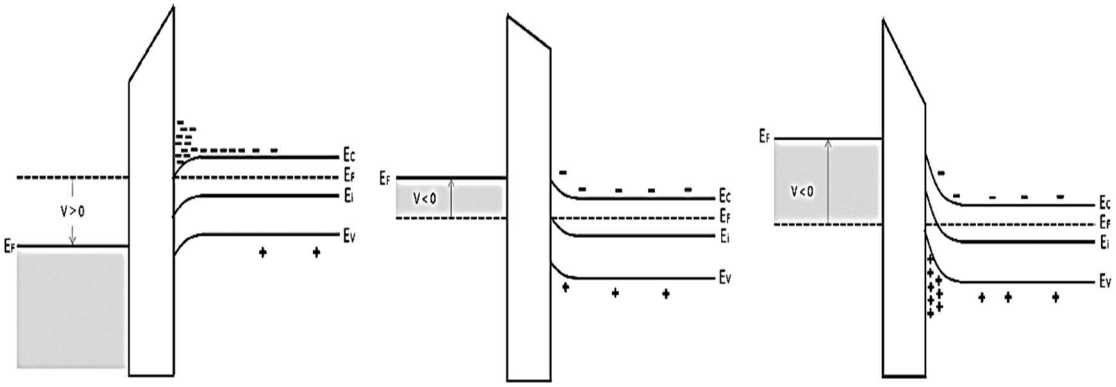

Figure 2.7 Energy band diagram of accumulation, depletion and inversion regimes of MOS capacitor [9].

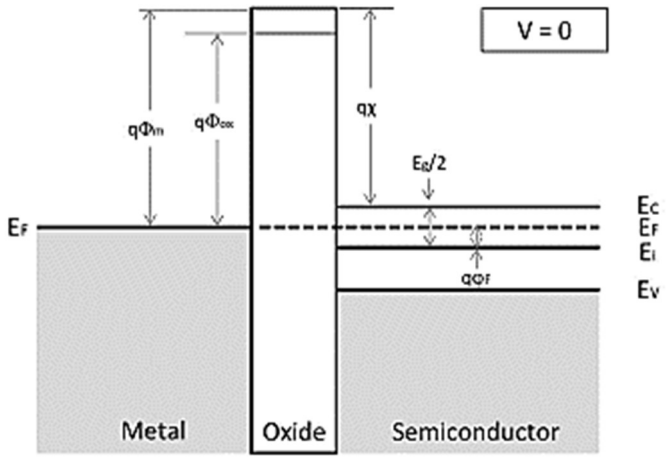

Figure 2.8 Energy band diagram of an ideal pMOS structure in flatband condition [9].

The theoretical equations of a pMOS capacitor to define the parameters in energy band diagram are shown in below. The equations for semiconductor work function, ϕ_s and bulk Fermi potential are [9]

$$\phi_s = \chi + \frac{E_g}{2q} - \phi_F \tag{2.1}$$

$$|\phi_F| = \frac{kT}{q} ln \frac{N_d}{n_i} \tag{2.2}$$

where

χ : Electron affinity

E_g : Intrinsic band gap energy

q : Electric charge

ϕ_F : Bulk Fermi potential

k : Boltzmann constant

T : Temperature

n_i : Intrinsic carrier concentration of silicon

N_d : Phosphorous doping concentration

The depletion width of the silicon substrate is given as in Eq.(2.3) where ε_s is the permittivity of silicon. When $\phi_S = 2\phi_F$, it is known as threshold condition, where the maximum depletion width is reached. At this point, the capacitance value is at the lowest value. [9]

$$x_d = \sqrt{\frac{2\varepsilon_s(|\phi_S|)}{qN_d}} \tag{2.3}$$

The flatband voltage is defined as the difference between ϕ_M and ϕ_S. At here, the flatband, gate and threshold voltages can be expressed as [9]

$$\begin{aligned} V_{FB} &= \phi_M - \phi_S \\ &= \phi_M - (\chi + \frac{E_g}{2q} - \frac{kT}{q} ln \frac{N_d}{n_i}) \end{aligned} \tag{2.4}$$

$$V_G = V_{FB} + \phi_s - \frac{\sqrt{2\varepsilon_s \phi_s q N_d}}{C_{ox}} - \frac{Q_{inv}}{C_{ox}} \tag{2.5}$$

$$V_T = V_{FB} - 2|\phi_s| - \frac{\sqrt{4\varepsilon_s \phi_s q N_d |\phi_F|}}{C_{ox}} \tag{2.6}$$

According to Zeghbroeck [36], based on all the equations from this part, an ideal C-V curve of MOS capacitor can be plotted at low and high frequencies conditions. These ideal mathematical equations to represent C-V curve of MOS capacitor are not used in this research due to its simplicity and rough approximation to exact C-V curve. The expected capacitance based on this method is shown in Table 2.4.

Table 2.4 Ideal capacitance value of MOS capacitor at each regime in low and high frequencies condition.

Regions	Low Frequency	High Frequency
Accumulation	$C_{MOS} = C_{OX}$	$C_{MOS} = C_{OX}$
Depletion	$C_{MOS} = C_{OX} \| \| C_d$	$C_{MOS} = \frac{1}{\frac{1}{\text{Cox}} + \sqrt{\frac{2\emptyset_s}{q(N_A - N_D)\varepsilon_s}}}$
Inversion	$C_{MOS} = C_{OX}$	$C_{MOS} = \frac{1}{\frac{1}{\text{Cox}} + \sqrt{\frac{4\emptyset_F}{q(N_A - N_D)\varepsilon_s}}}$

2.7 Exact Capacitance of MOS Structure

In 1982, Nicollian and Brews [37] mentioned that the C-V curve of MOS capacitor can be represented by an equivalent circuit and the capacitances are expressed in mathematical equations as a function of gate bias at low and high frequencies. The equations are based on steady state condition and p-type substrate of the MOS capacitor.

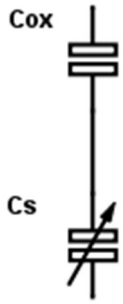

Figure 2.9 A simple equivalent circuit to represent MOS capacitor.

a. Low Frequency Capacitance

In order to plot low frequency C-V curve of MOS capacitor, the equations that are related, such as the total capacitance (C_{MOS}), silicon surface charge density (Q_s), silicon capacitance (C_s) and applied gate bias (V_G) as shown in below:

$$C_{MOS} = \frac{1}{\frac{1}{C_s(v_s)} + \frac{1}{C_{ox}}} \tag{2.7}$$

$$Q_s = Sign(-v_s)\frac{\varepsilon_s}{L_{Di}}(\frac{kT}{q})F(v_s, u_B) \tag{2.8}$$

$$C_s(v_s) = \frac{C_{FBS}}{\sqrt{2}} \frac{\exp(v_s) - \left(\frac{n_i}{N_d}\right)^2 \exp(-v_s) - 1}{\sqrt{[-(v_s + 1) + \exp(v_s) + \left(\frac{n_i}{N_d}\right)^2 \exp(-v_s)]}} \tag{2.9}$$

$$V_G = -\frac{Q_s(v_s)}{C_{ox}} + v_s \tag{2.10}$$

where

C_{ox} : Oxide capacitance

v_s : Total band bending

ε_s : Permittivity of silicon

L_{Di} : Intrinsic Debye length

$F(v_s, u_B)$: Dimensionless electric field in the silicon

C_{FBS} : Flatband capacitance

b. <u>High Frequency Capacitance</u>

The equations for a C-V curve of MOS capacitor at high frequency is different compared to low frequency. This is due to the carrier response of majority and minority carriers react differently in low and high frequencies condition. The different of the equation is in the silicon capacitance part, which require integration and Δ is a fraction that considers the spatial redistribution and inversion charge layer. The rest of the equations are same with low frequency equation.

$$C_s = 2C_{FB}\left[1 - \exp(-v_{s0}) + \left(\frac{n_i}{N_d}\right)^2 (\exp(v_{s0}) - 1)\frac{\Delta}{1+\Delta} + 1\right][F(v_{s0}, u_B)]^{-1} \quad (2.11)$$

$$\Delta = \frac{F(v_{s0}, u_B)}{\exp(v_{s0}) - 1}\left\{\int_0^{v_{s0}} \left(\frac{\exp(v_s) - \exp(-v_s) - 2v_s}{F(v_s, u_B)^3}\right) dv_s - 1\right\} \quad (2.12)$$

2.8 Charges Associated with The MOS System

Based on Deal, MOS transistors were invented in between 1963-1964. For the past 15 years, after it was introduced to the world, there are no standard symbols to represent four types of charges. This has caused misunderstanding during meetings and publications of semiconductor passivation. Finally, in May 1979, a final terminology to represent those charges were acknowledged [38].

In reality, the exact MOS structure is included four types of oxide charges that are not mentioned previously. Those charges that can be found in the Si-SiO_2 interface are fixed oxide charge, mobile ionic charge, interface trapped charge and oxide trapped charge in Figure 2.10. These charges can be sorted into two groups, which are oxide charge and interface trapped charge [39].

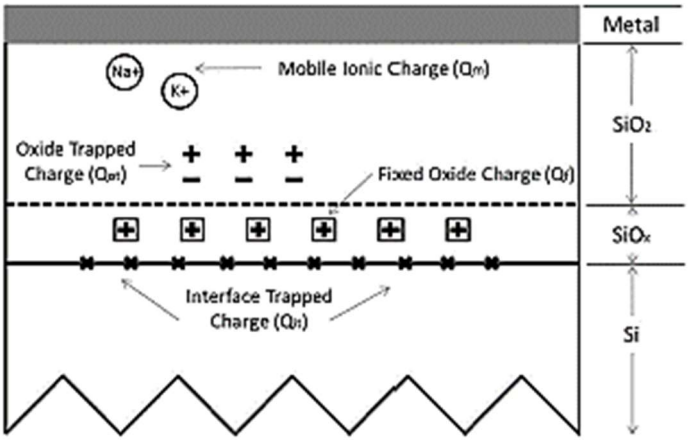

Figure 2.10 Charges associated with the MOS system at Si-SiO_2 interface [38].

2.8.1 Oxide Charges

Fixed oxide charge, Q_f is a layer of less than 2.5nm positive charges form in Si-SiO_2 interface whereby it is due to structural defects in the oxide layer related to oxidation process [38]. Q_f is typically positively charged, but it can be negative charges as well. The present of Q_f causes flatband voltage, V_{fb} shifting effect in C-V curve [40]. The direction of the shift depends on the type of charges, positive Q_f causes a left voltage shift, and negative Q_f causes a right voltage shift as shown in Figure 2.11 [9].

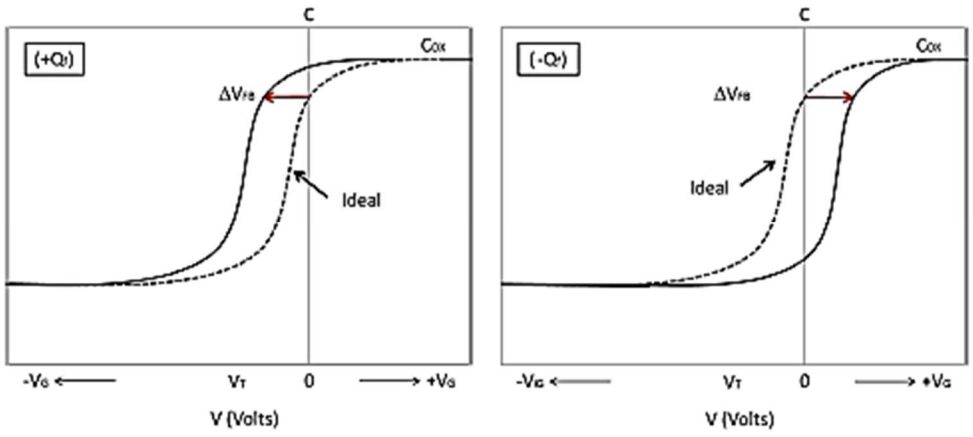

Figure 2.11 The C-V curve shift to the left ($+Q_f$) and right ($-Q_f$) for n-type semiconductor [9].

Mobile ionic charges, Q_m is known as ionic impurities such as positive/negative ions and heavy metals [38]. Lastly, oxide trapped charge, Q_{ot} is either positive/negative due to holes/electrons trapped in the bulk of the oxide from ionising radiation [38]. In addition, these two charges are related to C-V curve shift as well. The total voltage shift:

$$\Delta V = \frac{Q_f + Q_m + Q_{ot}}{C_i} = \Delta V_f + \Delta V_m + \Delta V_{ot} \qquad (2.3)$$

where C_i is the SiO_2 capacitance [34].

2.8.2 Interface Trapped Charge

Interface trapped charge, Q_{it} is either positive/negative charges located at Si-SiO_2 interface. The trapped charges are due to the defects caused by structural, oxidation-induced, metal impurities and radiation or any similar bond breaking processes. The difference between Q_f and Q_{it} can be view in term of electrical property, oxide charges are not electrically active, but interface trapped charge is electrically active. Q_{it} affects the characteristic of C-V by stretching out the curve as shown in Figure 2.12 [38].

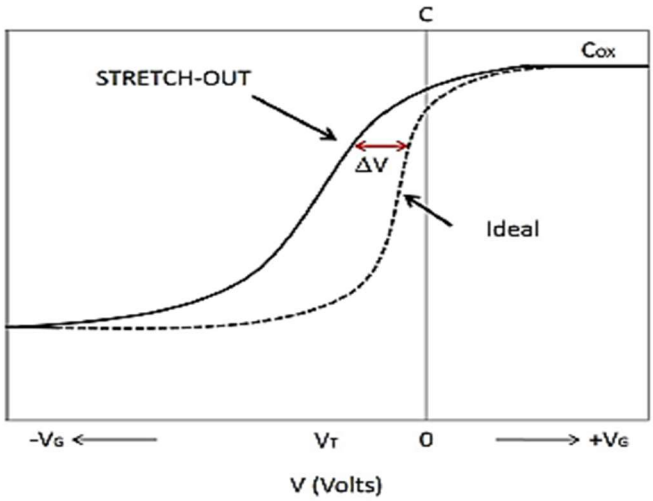

Figure 2.12 The C-V curve stretch-out due to the presence of Q_{it} [9].

2.9 Summary

The studies of Au-compensated HRS and related topics have been outlined in this chapter. PSC effect is a serious issue that causes CPW attenuation loss in high frequency application. Since 1994, a few methods have been suggested to solve this issue, and the attenuation loss is reducing. Besides, from the studies, the C-V curve of MOS capacitor can be plotted according to general and exact equations based on the equivalent circuit of low resistivity silicon model. Effect of associated charges can contribute to variation in C-V curve.

CHAPTER 3

METHODOLOGY

3.1 Introduction

This chapter begins with a general overview of the process involved to conduct a comparative study on the C-V behaviour of MOS capacitor on Au-compensated silicon in Section 3.2. Next, the review of capacitor design work obtained from Hashim [9] is covered in Section 3.3. The mathematical equations of C-V behaviours for low and high frequencies condition based on two methods are included in Section 3.4. Next, the proposed equivalent circuit model is mentioned in Section 3.5. Follow by all the default parameter values involved in the simulation are shown in Section 3.6. The details of simulations in MATLAB and SILVACO are further stated in Section 3.7 and Section 3.8. Finally, a summary of the entire chapter is summarised in Section 3.9.

3.2 Project Flow of Analysis

This project begins with the literature review on a detailed study of topics related to this research area, such as low and high resistivity silicon, parasitic surface conduction effect, MOS capacitor theory and others as covered in Chapter 2. Two different methods with its several mathematical equations are found in related journals and books. Based on the equations, the first simulation is carried out in MATLAB. The simulation results are analysed and a most suitable method is determined by the two methods.

From the previous low resistivity silicon substrate of MOS capacitor C-V simulation, a simple equivalent circuit is used. Since Au-compensated silicon substrate is