TERJEMAHAN

UNIVERSITI SAINS MALAYSIA

Second Semester Examination
2000/2001 Academic Session

February/Marc 2001

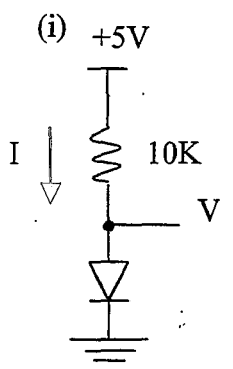
ZCT 106/4 - Electronic

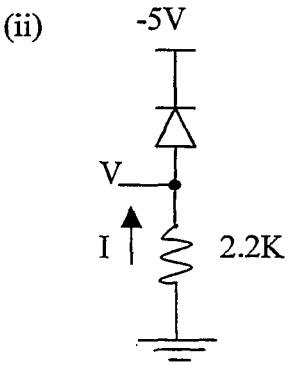
Time : 3 jam

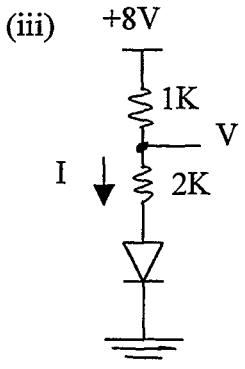
Please check that the examination paper consists of **FOURTEEN** printed pages before you commence this examination.

Answer all FOUR questions. Candidates may choose to answer all questions in the Malay Language. If candidates choose to answer in the English Language, it is compulsory to answer at least one question in the Malay Language.

1. (a) In Fig. 1.1, find the voltage V and the current I as indicated. The diodes drop $V_D = 0.7V$ when conducting.







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(iv)

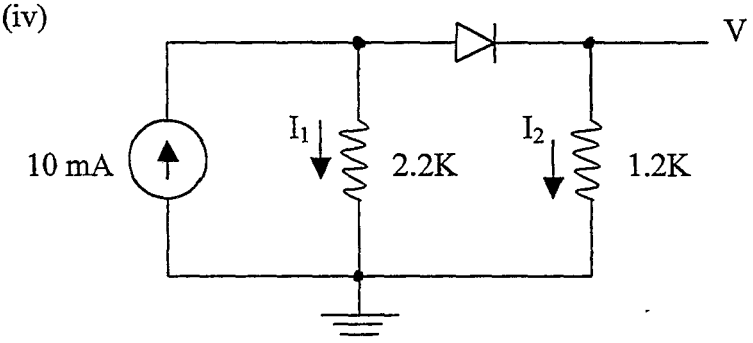
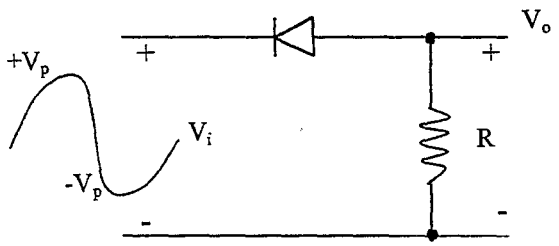


Fig. 1.1

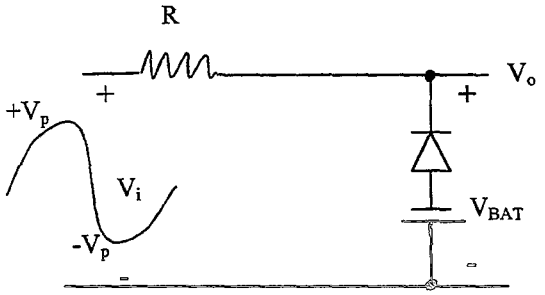
(45/100)

(b) In Fig. 1.2, sketch V_o . $V_D = 0.7V$.

(i)



(ii)



(iii)

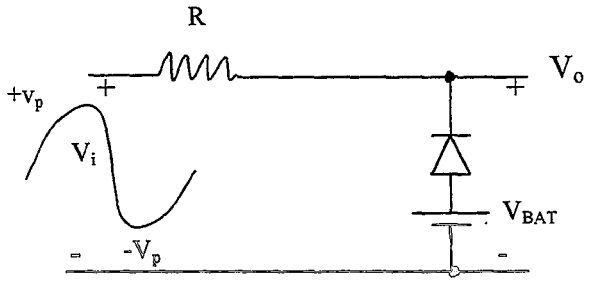


Fig. 1.2

(15/100)

... 10/-

(c) Determine I_B , I_C , I_E and V_{CE} for the silicon transistor circuits as shown in Fig. 1.3. Take $\beta = 100$.

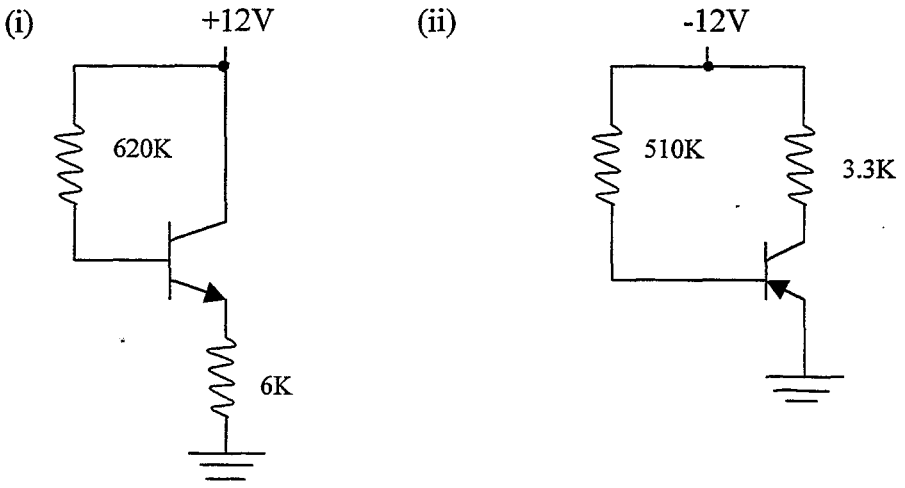
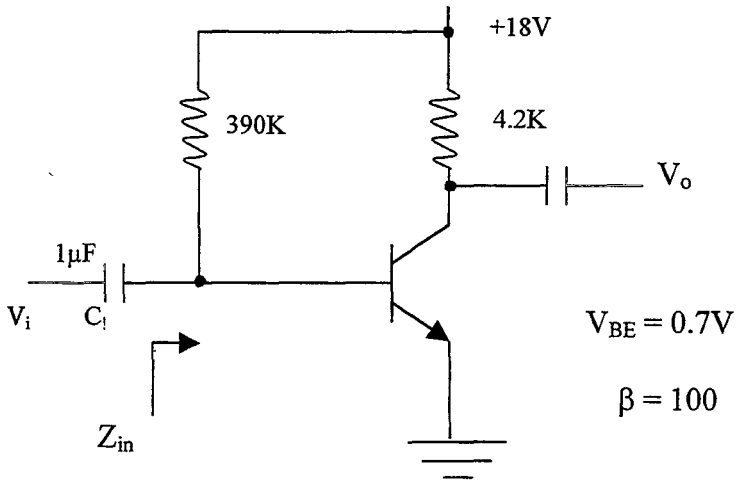


Fig. 1.3

(40/100)

2. (a) For the network of Fig. 2.1

(i) Determine Z_{in} .
(ii) Calculate the gain.
(iii) Calculate the cut off frequency formed by C1.
(iv) Draw the small signal π model of the circuit.



(40/100)

Fig. 2.1

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(b) Find the value of the output v_o as indicated in Fig. 2.2.

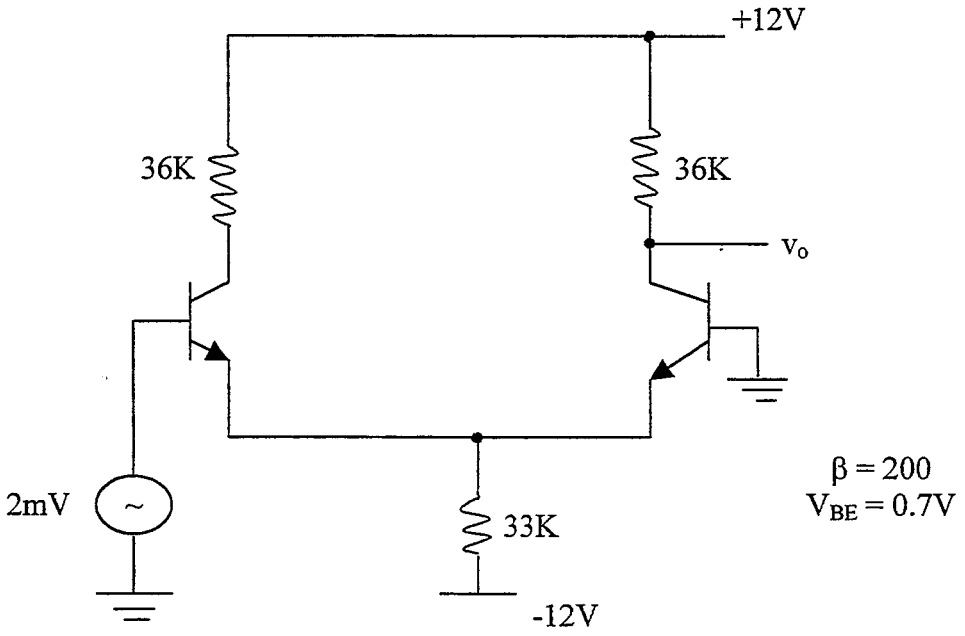

Fig. 2.2

(30/100)

(c) Determine Z_{in} and the total gain of the circuit in Fig. 2.3

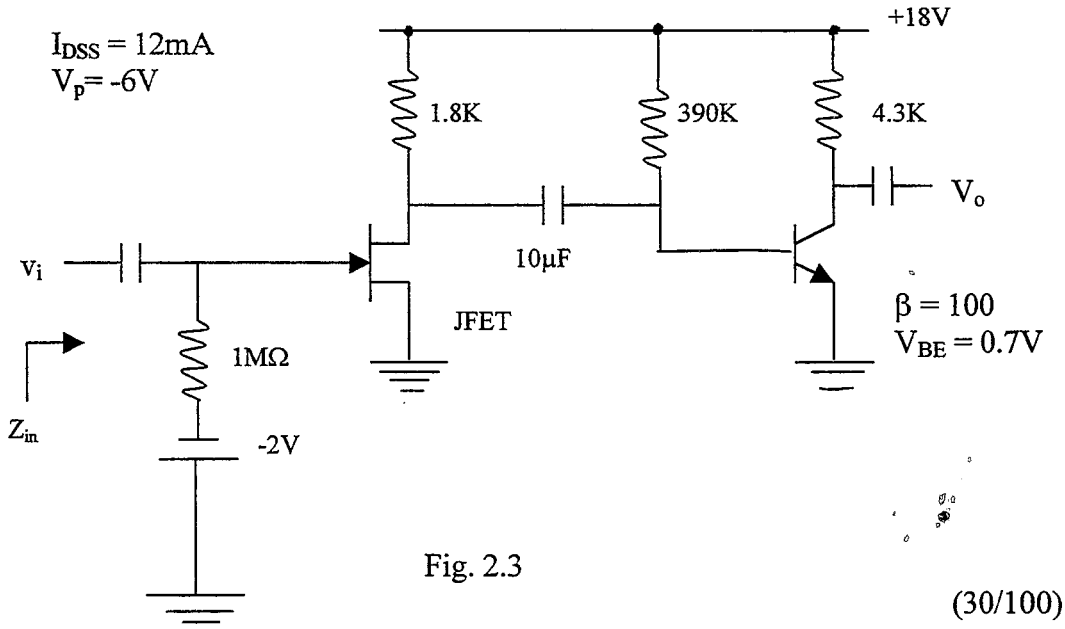

Fig. 2.3

(30/100)

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3. (a) (i) Calculate the output voltage for an input of V_{in} =5mV, for the circuit in Fig. 3.1.

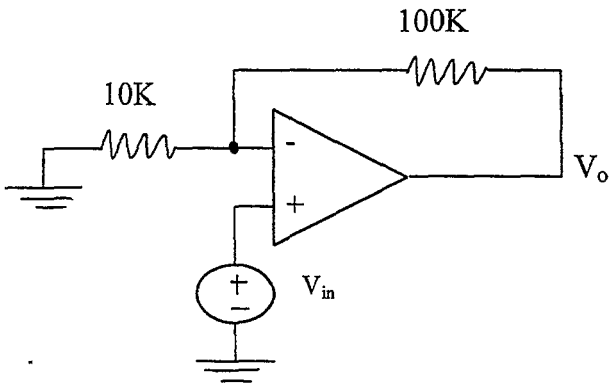


Fig. 3.1

(ii) Calculate the output voltage for the circuit of fig. 3.2 with V_1 = 40mV and V_2 = 20mV.

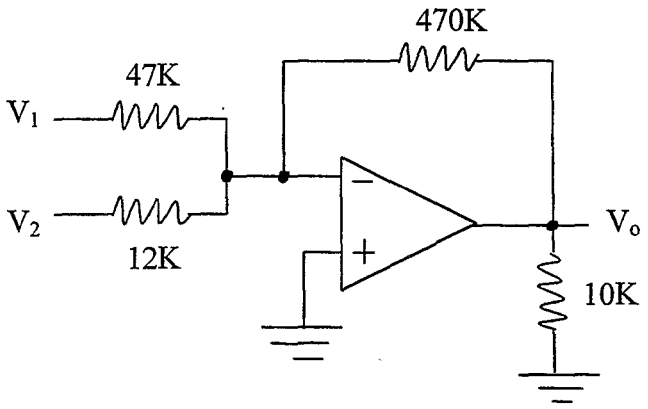
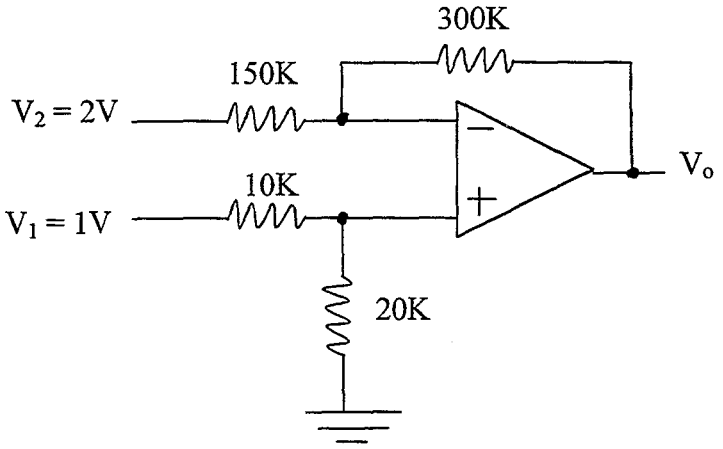


Fig. 3.2

(iii) Determine the output voltage for the circuit of Fig. 3.3.



(60/100)

Fig. 3.3

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(b) (i) Sketch the frequency response, indicating the gain in dB, of the circuit shown in Fig. 3.4.

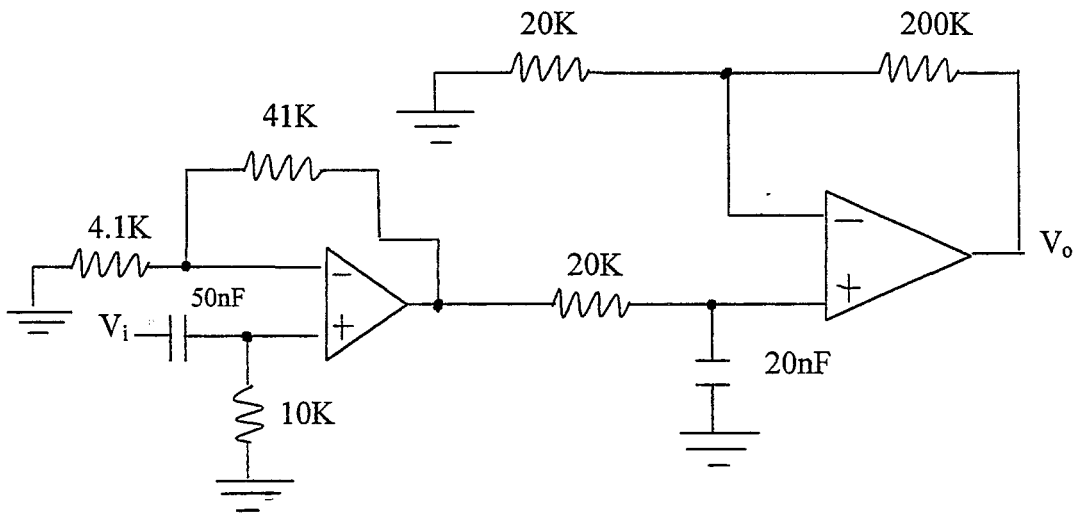

Fig. 3.4.

(20/100)

(ii) Calculate the gain of a negative feedback amplifier having an open loop gain, A = -2000 and a feedback factor $\beta = 1/10$.

(20/100)

4. (a) Determine R_b and R_c for the transistor switch if $I_{csat} = 10mA$.

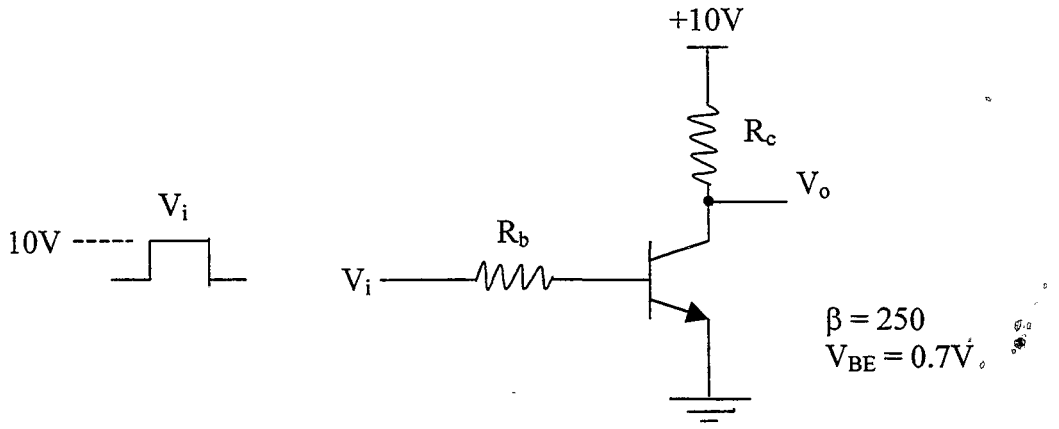

Fig. 4.1.

(20/100)

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(b) (i) Draw a FET phase shift oscillator circuit.

(ii) Calculate the operating frequency of the oscillator if R = 6KΩ and C = 1500pF.

(iii) Select a suitable value for R_D if g_m = 2mS.

(30/100)

(c) Calculate the output voltage and the Zener diode current in the regulator circuit of Fig. 4.2

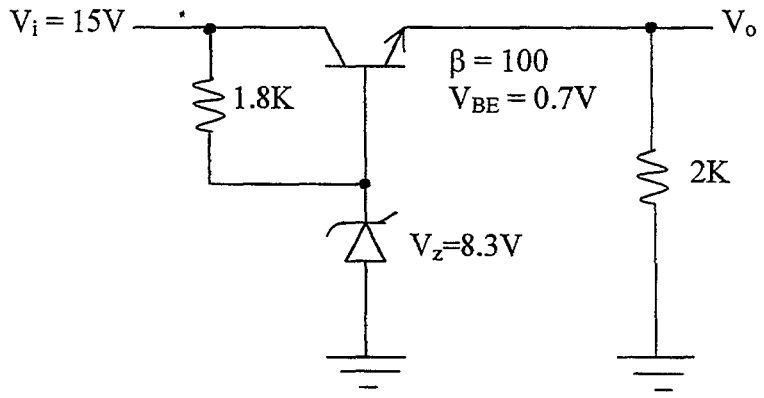

Fig. 4.2.

(20/100)

(d) Determine the maximum value of load current at which regulation is maintained for the circuit of Fig. 4.3.

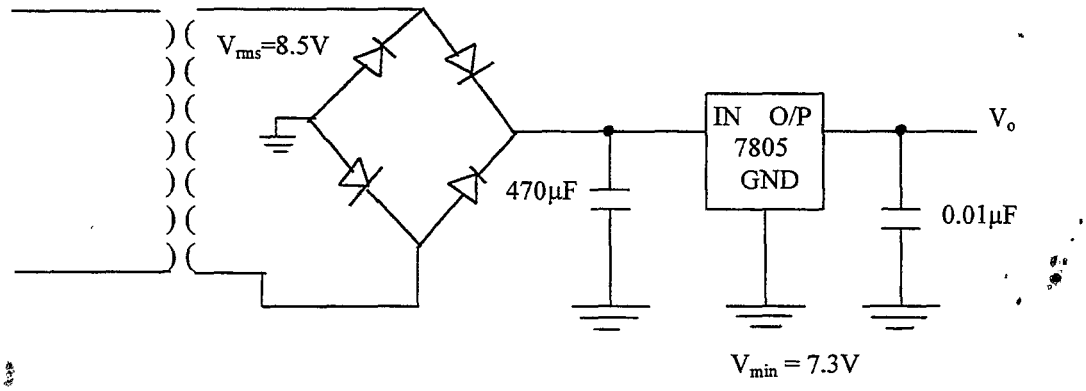

Fig. 4.3

(30/100)

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