IMPROVED STRUCTURED FILTER DESIGN AND ANALYSIS OF PERTURBED PLL SYSTEMS WITH CONVEX OPTIMIZATIONS

SITI JULIANA ABU BAKAR

UNIVERSITI SAINS MALAYSIA

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by

SITI JULIANA ABU BAKAR

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LIST OF ABBREVIATIONS

ADPLL	All Digital PLL
APLL	Analog PLL
ARE	Arithmetic Riccati Equation
CMOS	Complementary Metal-Oxide-Semiconductor
DA	Direct Analog
DC	Direct Current
DD	Direct Digital
XOR	Exclusive OR
FK	Frequency Keying
FSK	Frequency Shift Keying
FM	Frequency Modulation
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HJIE	Hamilton-Jacobi-Isaacs Equation
IC	Integrated Circuit
KYP	Kalman-Yakubovich-Popov
LF	Loop Filter
LMI	Linear Matrix Inequality
LTE	Long Term Evolution

LTI	Linear Time Invariant
PC	Phase Comparator
PFD	Phase Frequency Detector
PLL	Phase-Locked Loop
PI	Proportional Integral
RF	Radio Frequency
Sedumi	Self-Dual Minimization
VCO	Voltage Controlled Oscillator
WiMAX	Worldwide Interoperability Mobile Access
Yalmip	Semidefinite Programming Solver

LIST OF SYMBOLS

$\bar{\sigma}(A)$	Maximum singular values of A
$\triangle f$	VCO Frequency
C	Capacitor
$F(s)$	Loop Filter Transfer Function
f_{in}	Input Signal Frequency 1
f_{fed}	Feedback Signal Frequency
f_L	VCO Frequency Range
f_{ref}	Input Signal Frequency
f_0	Output Signal Frequency
γ	Gamma
$G(s)$	Closed-loop Transfer Function
$\mathrm{He}(X)$	$X + X^*$ Complex conjugate of X
K_c	Nonlinear Sector-Bound
K_d	Phase Comparator gain
K_l	Nonlinear Lower Slope-Bound
K_{max}	Maximum Loop Gain
K_T	Open Loop Gain
K_u	Nonlinear Upper Slope-Bound
K_v	Voltage-Controlled Oscillator Gain

$LF(0)$	DC Gain of Loop Filter
N	Feedback N Divider
M	Reference M Divider
M_ω	Peak Amplitude of System
ω_c	Cut-off Frequency of Filter
ω_H	Hold Range
ω_{in}	Input Frequency
ω_L	Lock Range
ω_n	Natural Frequency
ω_o	Output Frequency of VCO
ϕ_m	Phase Margin
R	Resistor
$\Re$	Real numbers
$\Re^+$	Positive real numbers
$\Re^{n\times p}$	Real $n \times p$ matrices
S_L	Sector-bounded Lower
S_U	Sector-bounded Upper
σ	Maximum Singular Value of A
τ	Time Constant
τ_1	Filter Coefficient 1
τ_2	Filter Coefficient 2

$\theta_e(s)$	Phase Error
$\theta_{fed}(s)$	Phase of PLL Output Signal
$\theta_{ref}(s)$	Phase of PLL Reference Signal
T_d	Time Delay
T_s	Sampling Time
t_s	Acquisition Time
V_d	Voltage Phase Comparator
V_{DD}	IC Power Supply
V_f	Voltage Loop Filter
$\varphi_1(.)$	Nonlinear Characteristic of Sine-wave PC
$\varphi_2(.)$	Nonlinear Characteristic of Triangular-wave PC
ξ	Zeta
ζ	Damping Factor

REKA BENTUK PENAPIS BERSTRUKTUR YANG DIPERBAIKI DAN ANALISIS SISTEM GELUNG TERKUNCI FASA TERGANGGU DENGAN PENGOPTIMUMAN CEMBUNG

ABSTRAK

Gelung terkunci fasa (PLL) adalah litar penting yang banyak digunakan dalam pelbagai aplikasi seperti komunikasi dan sistem elektronik. Kepentingan litar ini telah mendorong minat para penyelidik dalam mengkaji dan menganalisis kestabilan dan prestasi sistem PLL. Walaupun banyak analisis adalah berdasarkan kepada model lelurus sistem PLL, kestabilan PLL tidak dijamin kerana sistem itu mungkin terganggu oleh gangguan dalaman dan luaran yang termasuk perlakuan tidak linear dari komponen PLL serta lengah masa. Oleh kerana gangguan ini membawa kepada kemungkinan yang lebih tinggi terhadap kemerosotan prestasi dan ketidakstabilan, kerja-kerja terkini telah menunjukkan peningkatan jumlah penyelidikan berkaitan pemodelan sistem PLL yang lebih tepat dan analisis mengenai kesan ketidakpastian tersebut terhadap perlakuan keseluruhan sistem. Dalam kajian ini, pendekatan baru untuk memodelkan perlakuan tidak lelurus PLL secara sistematik dan mereka bentuk penapis yang bertanggungjawab untuk menentukan kestabilan dan prestasi sistem adalah dicadangkan. Pendekatan ini berdasarkan sintesis kawalan H_∞ yang juga diintegrasikan dengan kriteria kestabilan tidak lelurus yang sesuai. Kaedah-kaedah yang dihasilkan kemudiannya diformulasikan menjadi masalah pengoptimuman cembung yang dapat menjamin keoptimuman parameter-parameter yang direka bentuk. Hasilnya kemudiannya diperluaskan kepada aplikasi sintesis frekuensi yang juga tertakluk kepada gangguan yang tidak diingini. Perkembangan seterusnya bagi kaedah yang dicadangkan adalah dalam menganalisa sistem PLL yang juga tertakluk kepada lengah masa, yang mungkin

diwarisi dari sistem itu sendiri atau diperkenalkan secara buatan untuk memenuhi keperluan reka bentuk PLL tertentu. Penemuan-penemuan semasa menunjukkan bahawa keupayaan pengesanan sistem PLL boleh dibuktikan secara teorinya melalui kaedah-kaedah yang dicadangkan yang seterusnya membawa kepada julat kunci yang lebih luas sebanyak 59% dan masa pengambilalihan yang lebih cepat sebanyak 22% berbanding kaedah lelurus. Di samping itu, keputusan juga menunjukkan bahawa sistem PLL dengan penapis yang direka bentuk melalui kaedah yang dicadangkan lebih baik dari kaedah yang sedia ada. Sebagai contoh, apabila kaedah yang dicadangkan dibandingkan dengan kaedah (Ahmad, 2017), kaedah yang dicadangkan dapat menghasilkan julat kunci lebih besar sebanyak 87% dan masa pengalihan yang lebih cepat sebanyal 5733% daripada kaedah tersebut. Keputusan-keputusan ini juga disahkan melalui satu siri simulasi dan eksperimen yang menunjukkan kecekapan kaedah yang dicadangkan untuk meningkatkan prestasi PLL. Selain itu, analisis mengenai PLL yang tertakluk kepada kedua-dua ketidaklelurusan dan lengah masa telah juga didapati bermanfaat dalam reka bentuk PLL disebabkan oleh kaedah pemodelan secara sistematik yang diperkenalkan bersama dengan teknik pengoptimuman cembung. Kajian ini boleh disimpulkan bahawa kajian ini telah membawa kepada pendekatan baru untuk memperbaiki struktur PLL sebenar dengan kerumitan pengiraan yang rendah dalam kaedah reka bentuk dan analisis.

IMPROVED STRUCTURED FILTER DESIGN AND ANALYSIS OF PERTURBED PLL SYSTEMS WITH CONVEX OPTIMIZATIONS

ABSTRACT

Phase-locked loops (PLLs) are essential circuits that are widely used in many applications such as communication and electronic systems. The importance of this circuit has prompted a great interest among researchers in studying and analyzing the stability and performance of PLL systems. Although many analyses are based on linearized models of the PLL system, the stability of the PLL is not guaranteed as the system may be interrupted by internal and external perturbations which include nonlinear behavior from the PLL components as well as time delay. As these perturbations lead to higher probability of performance degradation and instability, recent works have shown an increasing amount of research into a more accurate modeling of PLL system and analysis on the impacts of such uncertainties to the overall system's behavior. In this study, a new approach to systematically model the nonlinear behavior of the PLL and to design the filter which is responsible to determine the system's stability and performance is proposed. This approach is based on the H_∞ control synthesis which is also integrated with a suitable nonlinear stability criterion. The resulting methods are then formulated into convex optimization problems which can guarantee optimality of the designed parameters. The results are then extended to applications of frequency synthesis which is also subject to the unwanted perturbations. A further extension of the proposed method is on the analyses of the PLL system that is also subject to time delay, which may be inherent from the system itself or artificially introduced to meet a certain PLL design requirement. The current findings reveal that the tracking capability of the PLL system can be theoretically enforced via the proposed methods which consequently lead to a

wider lock range by 59% and a faster acquisition time by 22% as compared to the linear approximation method. Additionally, the results also show that the PLL system with the filter designed via the proposed method outperforms the existing methods. For example, when the proposed method is compared with the (Ahmad, 2017), the proposed method is able to produce a larger lock-in range by 87% with faster acquisition time by 5733% than that method. The results are also validated via a series of simulations and experiments which demonstrate the efficiency of the proposed methods in enhancing the frequency synthesis PLL performance. Apart from that, the analyses on the PLL subject to both nonlinearity and time delay have additionally been found to be beneficial in PLL design due to the systematic modeling method introduced along with the convex optimization techniques. It can also be concluded that this study has led to a new approach to further improve the real PLL structure with low computational complexity in the design and analysis methods.

CHAPTER 1

INTRODUCTION

1.1 Background

Phase-locked loop (PLL) circuits have been around since early 1930s during which the initial interest was the synchronization of two oscillators (typically between the reference oscillator and the local oscillator). Originally, this phase-locking concept was explored by De Bellescize. The first widespread use of the PLL concept began in 1940s for horizontal-sweep synchronization in television receivers (Wendt & Fredendall, 1943). The use of PLLs at the time, however, was limited due to low performance and high cost.

As the technology advances with time, many PLL circuits nowadays are miniaturized and fabricated in IC (integrated circuit) forms (Digi-Key, 2018; Nexperia, 2019; Semiconductor, 2003). The integration of PLLs with other circuit components also becomes more convenient and makes them more flexible for a broad range of applications such as clock synthesizers, clock generators, servo motor, and timing recovery (Austin, 2002; Ismaili et al., 2015; Mishra et al., 2011; Mondal & Mandal, 2016). Not only limited to the aforementioned applications, PLL principle is also widely used in various communication applications, such as Global System for Mobile Communications (GSM) and Global Positioning System (GPS), frequency keying/frequency-shift keying (FK/FSK) demodulation, and carrier phase tracking (Kazemi, 2011; Liu & Wu, 2018; Luo et al., 2018; Stevanovic & Pervan, 2018; Xu, 2014; Zakia & Samir, 2018).

A basic PLL systems consists of a phase comparator (PC), a loop filter (LF), and a voltage-controlled oscillator (VCO) which are connected to form a feedback loop as shown in Figure 1.1. Its fundamental operation is to synchronize the VCO's output frequency with the reference frequency which typically comes from a reference oscillator. Since the PLL system are used for various applications, there is no unique way to design this circuit. Hence, various combinations of PCs, LFs, and VCOs can be considered to produce a flexible PLL circuit, and continuous development of these essential components is highly beneficial for the improvement of PLL system performance. There are several variations of the PLL system. These include analog PLL (APLL), classical digital PLL (CDPLL), all digital PLL (ADPLL) and software PLL (SPLL). Each type is different depending on the implementation of components integrated into the system. The configuration of PLLs can either be in analog or digital, but most of them are hybrids where they contain both analog and digital components (Best, 2003).

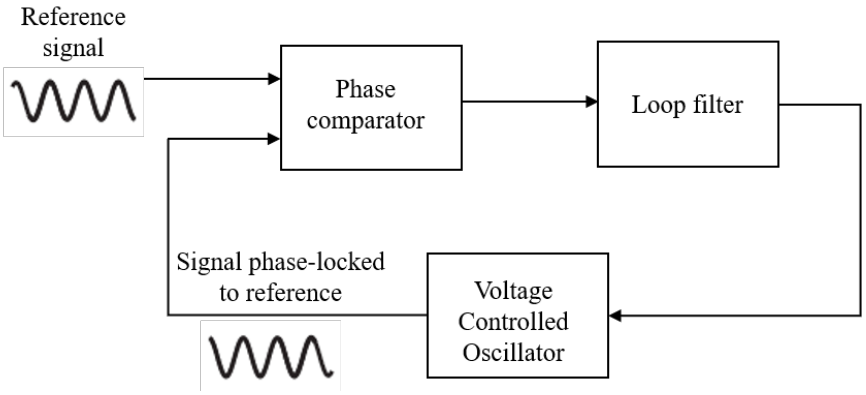

Figure 1.1: General PLL block diagram (Abramovitch, 2002).

The performance of the PLL can be measured by the dynamic behavior of the system upon which is greatly influenced by the loop filter that introduces poles to the closed-loop system Best (2003). The main responsibility of the loop filter however, is

to remove unwanted frequency components resulting from the phase comparison. This is important as the components may affect the bandwidth and the key performances (such as operating frequency range and acquisition time) of the PLL in general. There are three type of filters that are commonly employed in the PLL system which are passive lead-lag, active lead-lag and active propositional integral (PI) filters.

Since the structure of the filter for any PLL applications is not rigid, this component can be designed through various approaches (Chou et al., 2007, 2006; Erkens et al., 2007; Gentile, 2015; Mirabbasi & Martin, 1999). Numerous heuristic approaches to tune the parameters of the filter have been published in the literature (Austin, 2002; Banerjee, 2016; Golestan et al., 2013). One of the important parameters that can be considered to obtain the coefficients of the filter is phase margin. Several works that preassigned this parameter a priori to meet the desired performance and guarantee a stable operation of the PLL system include (Carlosena & Manuel-Latzaro, 2006; Kishine et al., 2004; Ugarte & Carlosena, 2015). However, these analytical design methods do not guarantee optimal values of the filter's coefficient. To provide a more systematic design technique for optimizing the filter, a modern control approach via H_∞ synthesis has been adopted in a number of studies on PLL filter design (Ahmad & Bakar, 2016; Chen & Chang, 2012; Suplin & Shaked, 2001). Several works that adopted the convex optimization method based on linear matrix inequality (LMI) in filter design can be found in (Ahmad, 2017; Chen & Chang, 2012; Chou et al., 2007). Based on the convex optimization approach, there is only one optimum solution in the filter design that guarantees the system to be globally optimal.

Despite the effectiveness of the proposed techniques, the stability of the PLL is

not guaranteed as the system may be disrupted by other factors such as internal and external perturbations (Banerjee & Biswas, 2018; Buckwalter et al., 2002; Leonov et al., 2015; Liu et al., 2013; Smirnova et al., 2015). Internal perturbation may exist from the nonlinearity of the PC and VCO, while an external perturbation may be caused by delay and noise. This issue has sparked great interest amongst researchers to conduct studies on comprehensive stability analysis of the nonlinear PLL system Ahmad (2017); Aleksandrov et al. (2016); Kuznetsov et al. (2014).

Prior work provides an intuitive insight about these nonlinear effects on the PLL based on a graphical technique known as phase plane portrait. In this method, however, the analysis is restricted to low order (i.e. first and second) PLLs. For higher order systems where the nonlinearity is sector restricted, the Lyapunov methods which are based on energy functions are more relevant but the analysis may become unmanageable as the order gets higher (Rahmani & Nodozi, 2015). Another approach that can guarantee the stability of the nonlinear PLL system is via the circle and popov criteria, which was initially derived in frequency domain (Ahmad, 2014). The analysis based on this criterion is also suitable for higher order systems as it can be converted to time domain conditions to form linear matrix inequalities that can be efficiently solved via convex optimization methods. Since an external perturbation from time delay is unavoidable in the real-time design of PLL systems especially for high-frequency range, ignoring the delay in the analysis of the PLL system therefore not only degrades the performance of PLLs but also leads the system towards instability.

1.2 Problem Statements

As the dynamic performance (such as the operating frequency range and acquisition time) of PLL systems is greatly influenced by the filter, various techniques have been reported in the literature to tune the parameters of the filter (Ahmad, 2017; Banerjee, 2016; Chen et al., 2010). The classical control method such as damping factor and natural frequency is usually employed to obtain the coefficients of the filter. These parameters can be used to minimize the peak of overshoot and to reduce the settling time and ultimately improved the time-domain response of the closed-loop PLL system (Li & Meiners, 2000; Mishra et al., 2011). These analytical design methods, however, do not guarantee optimal values of the filter's parameters. Another approach can be employed to tune the parameter of the filter is phase margin. This methods become the main interest in several design considerations since they are known to dominate the transient state of the system. This technique also able to provide a good jitter tolerance and guarantee stable operation for high order PLLs (Gentile, 2015; Ugarte & Carlosena, 2010; Zakia & Samir, 2018).

Another disruption of the PLL system may exist from the external perturbation, which is the time delay. In a real-time simulation of the PLL system, the existence of time delays is an inevitable issue, especially for high-frequency and discrete-time PLL systems (Buckwalter et al., 2002; Liu et al., 2013; Wilson, Nelson, & Farhang-Boroujeny, 2009). Therefore, by ignoring delay in the analysis of the PLL system not only causes the system to be less stable but also leads to degradation of the PLL performance (Harb, 2014). It will therefore be an advantage to determine the stability of time-delayed PLL systems with nonlinearity property that is included in the analysis.

1.3 Research Objectives

This research focuses on the improved structured filter design and the analysis of perturbed PLL systems. In this work, the structured filter refers to the active PI filter. The main objectives of this research are stated as follows:

1. To propose convex optimization methods for structured filter design based on H_∞ norm constraints and nonlinear stability criterion when the PLL system is subject to nonlinear effects from the PC.

2. To develop and implement frequency synthesis based on the proposed methods in objective 1, and to validate the results via simulations.

3. To systematically analyze the stability of the PLL system subject to both nonlinearity characteristic and time delay in continuous- and discrete-time frameworks with convex analysis.

1.4 Research Scope

The scope of this research is limited to the analysis of the PLL system perturbed by nonlinearity from the PC (arises from the over-driven mixer and XOR-gate which produces a triangular-waveform), while the VCO is assumed to be working in a linear region. Other nonlinear characteristics of PC such as sawtooth and sequential form are not covered in this research work. For the first contribution of this research, the structured filter (as refer to an active proportional integral) filter is considered to be designed. The result from the filter designed via the proposed method is then applied to the applications of frequency synthesis. For this application, the modeling and simula-

tion are conducted in Simulink Matlab and the parameters are taken from the datasheet CMOS CD4046BE.

Since pure time delay is infinite-dimensional variable, the Taylor approximation is the main technique to be considered in the analysis. This is because Taylor approximation gives better performance through empirical studies as compared to Pade and all-poles approximations. For the analysis of maximum loop gain of time-delayed PLL systems perturbed by nonlinear effects from PC, Butterworth and Bessel filters are considered as in this analysis. Other types of filters such as Sallen-key and Chebyshev are beyond the scope of this research.

1.5 Structure of the Thesis

This thesis consists of five chapters. Chapter 1 briefly describes the overview of the PLL system including its operation and applications. In this chapter, the problem concerning stability and performance of PLL systems is outlined in the problem statement. The motivations and research objectives are also discussed in this chapter. In addition, the research scope is highlighted in this section.

In Chapter 2, the basic structure of the PLL system including its vital components is reviewed. The mathematical equations of s- and $z-$domain models of the PLL system are further discussed based on classical textbooks and papers. Further in this chapter, a number of classical and modern works devoted to the computation of stability analysis of the linear and nonlinear PLL systems are discussed. The performance of the PLL system based on H_∞ approach is described. The important parameters that determine the operating range of the PLL system are also given in this chapter. Additionally,

some of the related works regarding the analysis of perturbed PLL system (such as time delay) are reviewed and discussed. Lastly, the literature review on the applications of the PLL system for frequency synthesis is also given.

The proposed method to design the filter for nonlinear PLL systems is introduced in Chapter 3. In this chapter, the nonlinear PLL model resembling a Lur'e structure is given and the formulation of linear matrix inequalities (LMIs) used to design the filter is presented. In addition to that, the modeling of frequency synthesis for the application of PLLs is also presented. In this chapter, stability and performance analysis of nonlinear time-delayed PLL systems is also presented. A systematic approach to obtain a maximum loop gain such that the stability of the PLL system is guaranteed when the PLL system is perturbed by time delay and nonlinear effects from PC is then presented. The algorithm to analyze the maximum loop gain with the existence of time delay and nonlinearity is also given.

In Chapter 4, the results for the filter design are presented and discussed. Additionally, some numerical examples to demonstrate the effectiveness of the proposed method are presented and discussed. The simulation results for frequency synthesis are also presented and discussed. In this chapter, the results on the analysis of nonlinear time-delayed PLL system is also presented. The maximum loop gains obtained via the proposed method is given. Lastly, the analysis and simulation of lock range for time-delayed PLL system with different nonlinear characteristics of PC are also given.

Finally, the conclusion of this thesis is presented in Chapter 5. This chapter also covers some future works to improve the PLL system design.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This chapter intends to review the PLL system design as well as its essential components. The related works on stability analysis of linear and nonlinear PLL systems will also be discussed in this chapter. Additionally, the absolute stability for nonlinear analysis of PLL systems which resembles the Lur'e problem will be discussed. Some of the related works on the applications of PLL for frequency synthesis will also be highlighted in this chapter. Finally, the overall PLL system design consideration will be given in the last section of this chapter.

2.2 PLL Systems Design

The PLL system comprises a PC (also known as a phase detector), a loop filter, and a VCO. There are many works that discuss the implementation of each of these components in the PLL system design. The PC plays a very important role in detecting the frequency or phase difference between the reference and feedback signals. If there is a phase difference between these two signals, it will generate an output voltage which is proportional to the phase error of these two signals. There are two broad categories of PCs; multiplier PC (memoryless device) and sequential PC (memory device). Generally, the type of PC to be employed in a specific situation depends on its application. The multiplier PC (also known as classical mixing PC) is the most common PC used in linear PLL systems (Best, 2003). A simple diagram of the multiplier PC and sequen-

tial PC are shown in Figure A.2 and Figure A.4 respectively. Table 2.1 summarizes the classification of phase comparators with their characteristics and linear ranges. The corresponding characteristics of the average output signal, V_d against phase difference, θ_e for the aforementioned PCs are summarized in Figure 2.1. From the figure, the curves for all PC characteristics are plotted with the same slope of phase error $\theta_e = 0$ and the same factor of K_d.

Table 2.1: Classification of Phase Comparators.

Type	Class	Characteristic	Linear range
Multiplier	Analog	Sine-wave	$-\pi/2$ to $+\pi/2$
XOR gate	Digital	Triangular-wave	$-\pi/2$ to $+\pi/2$
JK flip-flop	Digital	Sawtooth-wave	$-\pi$ to $+\pi$
PFD	Digital	Sequential PFD	-2π to $+2\pi$

Since the phase comparator is a nonlinear device, this nonlinear behavior may affect the stability of the PLL system. Thus, constructing an adequate mathematical model of the PLL system is very important. This issue has sparked great interests among researchers to study the nonlinear characteristic of the PC (Best et al., 2015; Blagov et al., 2019; Kuznetsov et al., 2012; Leonov et al., 2015). Basically, the characteristic of the PC is dependent on its realization and the types of signal applied at its inputs. One of the works that discusses nonlinear analysis of classical PLL system with multiplier/mixer PC can be found in (Leonov & Kuznetsov, 2014). Some other works that present an adequate mathematical analysis of the PC characteristic with various signals (non-sinusoidal waveforms) are demonstrated in (Kuznetsov et al., 2015, 2014; Leonov, 2008; Leonov et al., 2015). By approaching nonlinear rigorous mathematical

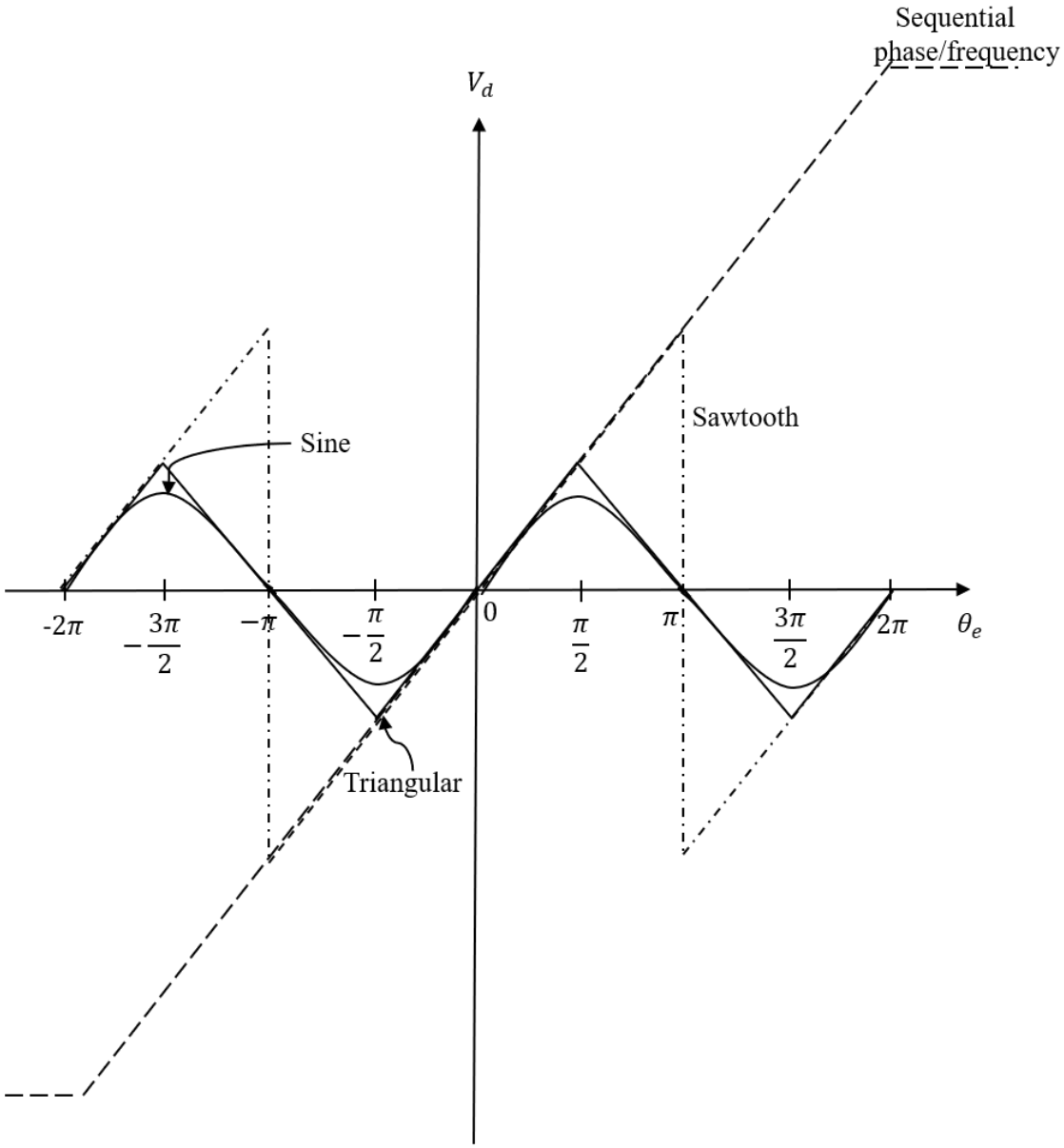

Figure 2.1: Characteristics of PC (Thomas, 1970).

equation of PC characteristic, the dynamic model of the nonlinear PLL system can analytically be implemented.

In PLLs, a low-pass filter is utilized as the loop filter. A low-pass filter smoothens the output of the PC by suppressing the high-frequency components. Generally, the dynamic performance (i.e., hold-in, pull-in, pull-out, lock-in), the loop bandwidth, and the switching speed of the PLL system are dependent on the loop filter (Razavi, 2012). The loop filter therefore is a critical component in the PLL system design. The loop filter is broadly divided into either a passive or an active filter. Since the active filter usually employs an operational amplifier that generates a lot of noise, the passive filter is therefore regularly preferred as the loop filter. However, in cases where the VCO requires a tuning voltage larger than what the PC can supply, an active filter might be needed (Banerjee, 2016). The three basic filter types that are commonly employed in PLL systems are the passive lag-lead, the active lead-lag and the Proportional Integral (PI) filters (Best, 2003). The structures of these filters are depicted in Figures A.5 to A.7 and the corresponding transfer functions can be expressed as Equations A.2 to A.4 respectively.

The performance of the PLL system is usually indicated by the lock range and settling time and these parameters rely on loop filter characteristic Best (2003). As has been discussed by Eklund (2006), the best type of filter is chosen based on its ability to provide a minimum or a zero-phase error. Generally an active filter has a pole at $s = 0$, which makes it capable of reducing the phase error to zero. Theoretically, an active PI filter can provide an infinite hold range and pull-in range, and also can have a good phase tracking (Chou et al., 2007). Referring to the report that has been discussed by

(Austin, 2002), the best recommendation for a general-purpose PLL systems would be to employ an active filter. Therefore, under certain applications, an active filter is more preferable as compared to a passive one.

The structure of the loop filter for any PLL applications is not rigid. Hence, the options to design this component exists in various approaches (Carlosena & Manuel-Latzaro, 2006; Erkens et al., 2007). Applications in data communication systems, for instance, require high-order Bessel-type filter to produce superior loop dynamics and improve the jitter performance (Mirabbasi & Martin, 1999). For other applications where the lock-in time or acquisition time is not a major concern, and the main requirement is only to synchronize two frequencies, a simple RC or passive filter will be sufficient. When a simple passive filter is required but the phase margin needs to be increased or the phase noise performance needs to be enhanced, the lag-lead filter will be advantageous as its zero can be used to modify the system's frequency response (Gentile, 2015; Yao & Yeh, 2008). In applications that involve high speed or high-frequency signals where the acquisition time and lock-in range are of major concerns, the active PI filter is the most popular type, and is also one of the commonly preferred filters in CMOS IC for general-purpose PLLs (Austin, 2002; Chou et al., 2007; Mirabbasi & Martin, 1999).

Numerous heuristic techniques have been reported in the literature to tune the parameters of the filter in order to accommodate different performance criteria related to the PLL's frequency response (Austin, 2002; Banerjee, 2016; Golestan et al., 2013). For instance the phase margin is specified a priori to provide a good jitter tolerance and guarantee a stable operation for high-order PLLs (Carlosena & Manuel-Latzaro,

2006; Kishine et al., 2004; Ugarte & Carlosena, 2015). The associated peak amplitude, damping factor and bandwidth have also become the main design considerations since they are known to dominate the transient state of the system. Similar to the phase margin technique, these parameters can be preassigned to meet the desired performance requirements, and the classical control method is usually employed to obtain the coefficients of the filter. These analytical design procedures, however, do not guarantee optimal values of the filter's parameters.

In order to provide a more systematic design technique that is able to optimize the filter, a modern control approach via H_∞ synthesis has been adopted in a number of studies on PLL filter designs (Ahmad, 2017; Ahmad & Bakar, 2016; Chen & Chang, 2012; Suplin & Shaked, 2001). By using this approach, an admissible controller exists and the frequency response peak of the closed-loop PLL system is minimized such that the stability and performance of the system are preserved. A design framework for this approach is shown in Figure 2.2. Given the system $M(s)$ represents the generalized plant and K_H is the matrix description of the controller (called as the filter in this respect). The signal w contains all exogenous inputs (i.e., disturbance and noise), z denotes the output of an error signal, y represents the measured output variables, and u is signifies a control signals.

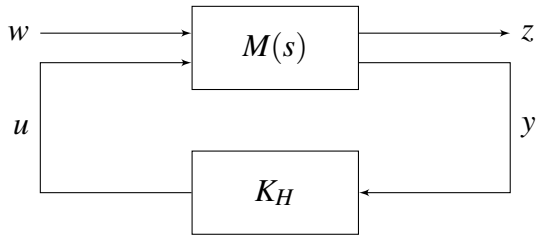

Figure 2.2: The standard H_∞ control framework.

Based on this structure, the admissible controllers $K_H(s)$ exists such that the infinity norm of the $\| T_{zw} \|_\infty$ is minimized and the stability of the closed-loop system is a guarantee. This approach is referred to the optimal H_∞ approach (Doyle et al., 1989). However, to find an optimal H_∞ controller is often complicated and not an easy task due to the optimal controller is not generally unique (Bosgra et al., 2001; Glover & Doyle, 1989). To find the close one in the norm sense to the optimal approach therefore have been introduced by Zhou and Doyle (1998). This approach is called suboptimal H_∞ approach. By using this approach, the performance level of the controller is determine by the parameter γ. Given $\gamma > 0$, admissible controllers $K_H(s)$ exists if there are any, such that $\| T_{zw} \|_\infty < \gamma$ is minimized. Some of the works that adopted this approach in the filter design for the PLL system can be referred to (Chou et al., 2007, 2006).

The methods to formulate and solve the H_∞ approach arises in a number of ways. It is includes Hamilton-Jacobi-Isaacs equation (HJIE) (Isidori, 1994; Van Der Schaft, 1993), algebraic Riccati equation (ARE) (Doyle et al., 1989), and Glover-Doyle algorithm (Doyle et al., 1989). Among all, the one based on the LMI is the most popular approach since it offers efficient convex optimization techniques (Gahinet & Apkarian, 1994; Iwasaki & Skelton, 1994). Through this method, the best solution of all feasible solutions can be solved quickly and efficiently. Additionally, this approach tends to offer more flexibility for incorporating several constraints on the closed-loop system (Boyd et al., 1994; Chilali & Gahinet, 1996). Several works have adopted this method to design the loop filter for PLL systems (Ahmad, 2017; Chen et al., 2010; Li & Fu, 1997). Based on this approach, it offers low computational complexity and the optimization problems also can efficiently be solved numerically. This method also offers possible solutions to enormous size of variables and constraints. For instance, the work

reported by (Chen & Chang, 2012) adopted this method to design the loop filter for the PLL system based on multi-objective functions that are included in the system design. This approach also allows the designer to parameterize the controller while minimizing the peaking of the closed-loop system, hence ensuring the tracking capability of the PLL in the presence of disturbances or noise for some targeted applications (Zhou & Doyle, 1998).

Another essential component of the PLL system is a voltage-controlled oscillator (VCO). The VCO is a nonlinear device that generates an output frequency that is directly proportional to its input voltage. Other than the PC and the loop filter, the VCO also plays an important role in determining the performance of the PLL system. Some of the work designing the VCO to improve the performance of the PLL system can be found in (Kumar, 2013; Mishra & Sharma, Gaurav Kr Boolchandani, 2014; Suman et al., 2016).

Many approaches concerning the stability analysis of the PLL system have been introduced. Several methods which include linear and nonlinear analyses of PLL systems in continuous- and discrete-time models will be reviewed in the next section.

2.3 Stability Analysis of PLL Systems

There are various methods and approaches available for analyzing the stability of the PLL system. Several methods and techniques commonly employed to analyze the stability of the PLL system is illustrated in Figure 2.3. From the figure, the analysis can be divided into the linear and nonlinear model with continuous- and discrete-time system. A well-known technique to analyze the stability of linear PLL circuit in the

continuous-time system is the Nyquist criterion. By using this criterion, the stability of the linear PLL system is preserved if all closed-loop poles are located in the left half s-plane. Some of the works that discus the stability of linear continuous-time PLL system by using this technique can be found in (Korytowski, 2015; Kroupa, 2003; Zhang et al., 2015).

In the work done by (Chen & Chang, 2012), the third-order passive filter for the linear PLL system was designed by using the convex method through the integration of multiple-objective which can be solved via the LMI method. Based on this proposed method, the ripple swing can be controlled by adjusting the filter pole to improve the spur performance. In addition to this, the PLL system was reformulated by using H_∞ synthesis to design the loop filter in order to improve the jitter peaking. Based on this work, the PLL system with the filter designed via the proposed method was able to produce large spur reduction without altering the loop bandwidth. However, this analysis is only useful for the linear PLL system.

Other work that analyze the performance of the PLL system based on the linearized model can be found in (Gentile, 2015). In this work, the optimal coefficient of the third-order passive filter was obtained by using the manipulation of gain bandwidth and phase margin as modified design parameters. The results verified that the passive filter obtained by using this simulation did match the theoretical frequency response analysis.

The discrete counter-part of the Nyquist criterion is called Jury criterion (Kuo & Golnaraghi, 1995). As reported by (Xiu et al., 2004), the Jury criteria is one of the

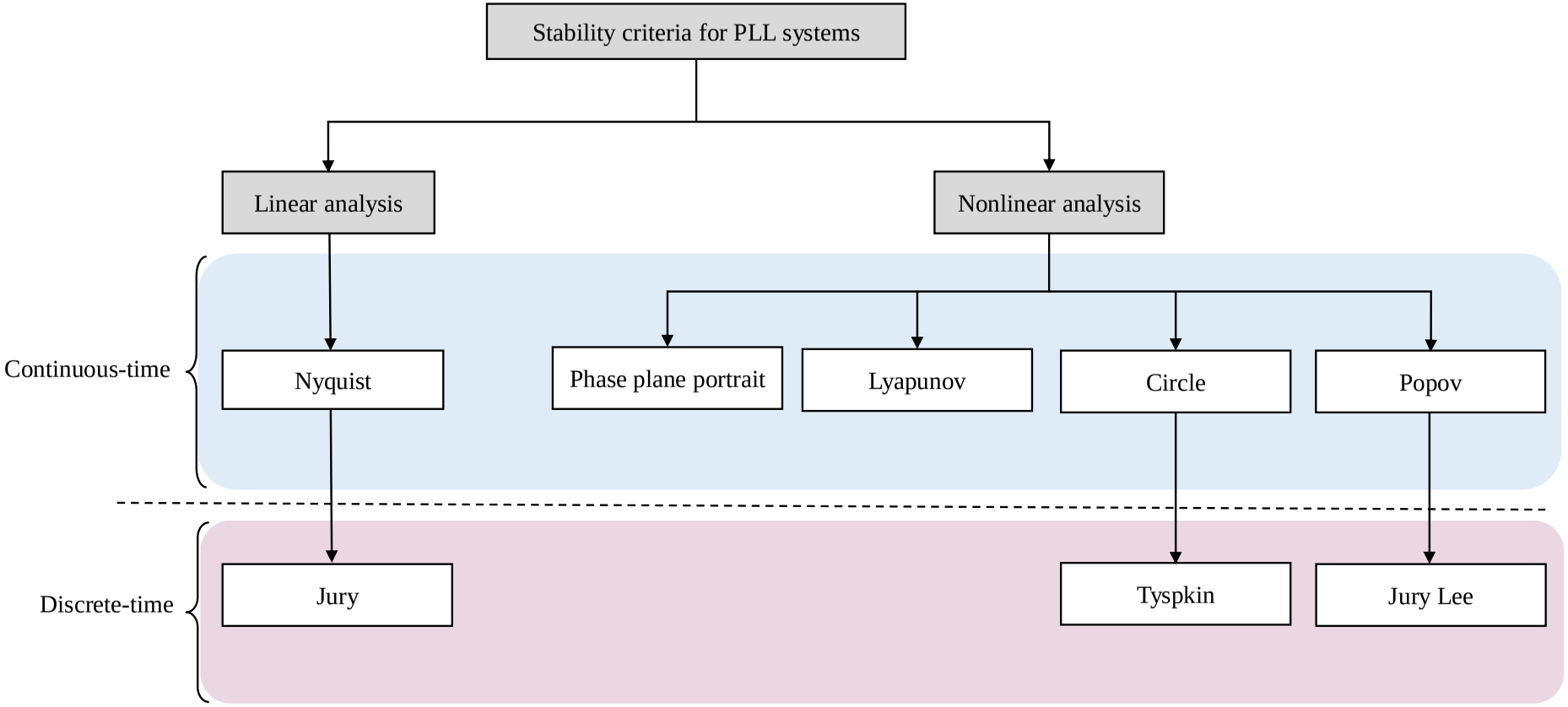

Figure 2.3: Stability criteria for linear and nonlinear PLL systems.

most effective criteria for testing the stability of the discrete-time system. This method provides easy and fast solutions in determining stability without performing complex calculations. Based on this criterion, in order to ensure the PLL system to be stable, all closed-loop poles should be located in the unit circle of z-plane. Technical report published by Texas instrument also employed this criterion to design the digital PLL system (Li & Meiners, 2000). Recently, a new method to design a fractional-N digital PLL system with spur cancellation scheme is presented (Ho & Chen, 2016). Based on this method, the range for a stable discrete PLL system can be determined using the Jury's criterion.

Despite the effectiveness of the linear analysis techniques for the PLL system, the stability of the PLL is not guaranteed as the system is inherently nonlinear due to the characteristics of the VCO and the PC (Daniels & Farrell, 2008; Kuznetsov et al., 2017; Leonov & Kuznetsov, 2014; Sarkar et al., 2014). Detailed nonlinear nature of the PLLs can be found in (Abramovitch, 2002; Tranter et al., 2010). By considering perturbation from the nonlinear characteristic of PC, the authors in Kuznetsov et al. (2015) investigated the performance of the nonlinear PLL system. In this work, it is shown that the simplification and the analysis of the linearized models of the control systems may result in incorrect conclusions. Based on this investigation, the motivation to develop rigorous analytical methods for the analysis of nonlinear PLL models has been suggested. The computation of various types of PC characteristics such as sine-wave and triangular-wave is also discussed.

As this perturbation leads to high probability of performance degradation and it subsequently causes the system to drop out of lock, recent work have shown an increas-

ing amount of research into developing a more accurate PLL systems modeling. These work be found in (Best et al., 2014; Kuznetsov, Nikolay V Kuznetsova et al., 2015; Leonov et al., 2012). Prior work by Viterbi (1966) provides an intuitive insight about these nonlinear effects on the PLL based on a graphical technique known as phase-plane portrait. In this method, however, the analysis is restricted to low order (i.e. first and second) PLLs. For higher-order systems where the nonlinearity is sector restricted, the Lyapunov methods which are based on energy functions are more relevant but the analysis may become unmanageable as the order gets higher (Abramovitch, 1990; Rahmani & Nodozi, 2015). To overcome this difficult situation and which the nonlinearities can be categorized as a sector- and slope-bounded, the analysis of the nonlinear PLL system resembles a Lur'e structured can be applied (Lur'e & Postnikov, 1944). The detailed explanation of this structure can be referred in appendix A.8.

Two main theorems applying the Lur'e system which give sufficient conditions for absolute stability in the continuous-time system are circle and popov criterion. Some of the works that employed these criteria in order to determine the stability of the nonlinear PLL system can be found in Ahmad (2014); Korytowski (2015); Wu (2002). The analysis based on these two criteria is also suitable for higher-order systems as it can be converted from frequency domain conditions to form linear matrix inequalities (LMI) that can be efficiently solved via convex optimization methods (Abramovitch, 2002; Ahmad, 2014). Both of these criteria provide a sufficient condition for the global asymptotic stable (GAS) for nonlinear systems. In the case to determine the absolute stability of the nonlinear discrete-time PLL system, Tsypkin and Jury-Lee can be considered (Ahmad & Goh, 2018). Among these criteria, usually, a criterion is adopted based on which criteria is simpler to apply in accordance with the problem and which

criteria produces less conservative.

Furthermore, in the work produced by Ahmad (2017), the analysis and performance of the nonlinear PLL system with an active PI filter by exploring the peak amplitude (M_ω) of the closed-loop PLL system is presented. Based on this method, the optimal coefficient of the active PI filter was obtained via the minimization of M_ω to unity while satisfying the nonlinear constraint. In this proposed method, the optimal filter was obtained by utilizing convex optimization via the LMI method. Although the simulation results showed better performance (in terms of the lock-in range and tracking capability) than the linear approximation method (only M_ω is minimized without considering the nonlinearity), the tracking capability was still limited when the frequency became higher. By fixing the maximum value of M_ω at unity, it does not allow one to select the parameter bandwidth of the filter if it is limited to the design requirements. The summary for some of the related works that analyze and design the PLL system as reported in the literature is presented in Table 2.2.

2.4 Analysis of PLL Systems with Time Delay Perturbation

The existence of delays in real-time simulation of control systems is an undeniable issue. Ignoring delay in the analysis of the PLL system not only degrades the performance of the system but also causes the system to be less stable. Extensive studies on the impact of time delay to the stability and performance of the continuous-time PLL system can be found in (Banerjee & Biswas, 2018; Sarkar & De, 1998; Wischert et al., 1992). Additionally, some of the works that quantitatively discuss the significance of time delay for discrete-time PLL system can be referred to (Da Dalt, 2005;

Table 2.2: Some of the related works on the analysis and design of the PLL system

Author	**Perturbed PLL**	**Filter Design**		**Highlight**
		Yes/No	**Method**	
Chen and Chang (2012)	No	Yes	LMI	Design the loop filter for PLL systems using convex method
Gentile (2015)	No	Yes	Phase margin	Design second-order passive loop filter by using loop bandwidth and phase margin as a design parameters
Kuznetsov et al. (2015)	Yes	No	-	Use phase plane portrait to analyze the nonlinear PLL system. Found that the linearized models of the PLL systems may result in incorrect conclusions
Aleksandrov (2016)	Yes	No	-	Use phase plane portrait to analyze the nonlinear PLL system.
Kuznetsov et al. (2017)	Yes	No	-	Use phase plane portrait to analyze the nonlinear PLL system. The lock-in range of the PLL system with active PI filter can be guaranteed
Ahmad (2017)	Yes	Yes	LMI	Designed active PI filter using H_∞ synthesis integrated with nonlinear criterion. The proposed method is performed in convex optimization
Nexperia (2019)	No	Yes	Damping factor & natural frequency	Develop PLL system with a active filter for frequency synthesizer application with output frequency of 2 MHz to 3 MHz

De Gloria et al., 1999; Djaferis et al., 1995; Patapoutian, 2002; Wilson, Nelson, & Farhang-boroujeny, 2009).

Harb (2014) reported that a PLL system with delay exhibits different behavior compared to that without delay. The degradation of the PLL performance (such as pull-in range) when the time delay is increased can also be observed according to the author. The same observations were also reported by Buckwalter et al. (2002), where PLL systems with delay drastically show different behavior as compared to conventional PLL models. The fact that an undesirable property of many discrete-time PLL systems is inherent delay, the stability regions for the discrete-time PLL system was also investigated by the author. From the analysis, a useful insight into the stability region of the PLL system which is restricted by the delay was provided.

In the work of (Xueyan, 2015), the response of the closed-loop system with a different approximation of time delays (such as Taylor, Padé, and all-pole) was investigated. In this work, the effects for different orders of the closed-loop system has also been analyzed. A comprehensive analysis of the system response based on the aforementioned approximation also was presented. From the results, the higher the order of time delay approximation leads to the more closely it matches the exact system's response. However, this leads to intricate calculations and the system would become more complex.

Way back in 2001, (Yaniv & Raphaeli, 2001) proposed a simplified yet useful analysis of the PI filters design for PLL system. In this design, the analysis of the PLL system is incorporated with a large delay using Padé approximation. Based on

this design method, a near optimal performance of the second and higher-order PLL system is suitable for the applications of carrier and timing recover. Some of the similar works that used a Padé approximation on the filter design for PLL system can be found (Chen & Chang, 2012; Chou et al., 2007).

2.5 PLL Applications

The concept of the phase locking principle introduced by De Bellescize (1932) has brought new light into a various application field. In telecommunications, the PLL circuit is used for modulations and demodulations, data/clock synchronizations, clock recovery and signal recovery from a noisy channel (Best, 2003; Bhargav et al., 2016; Stevanovic & Pervan, 2018). In computer systems and microprocessors, the PLL circuit is particularly used for clock generation and frequency synthesis (Abramovitch, 2002; Akhmetov et al., 2018; Donald R. Stephens, 2007; Xu, 2014). Not only limited to these applications, the PLL system can also be found in Global System for Mobile Communications (GSM), Global Positioning System (GPS), frequency tracking, radio systems (AM/FM radio) and servo motor control (Choi et al., 2015; Donald R. Stephens, 2007; Luo et al., 2018). Apart from being used in communication systems, it is also widely used in televisions, computers, and many other applications (Kameche & Feham, 2013; Keese, 1996; Moon, 2005).

Delivering a versatile PLL circuit is a never-ending challenge and is now becoming an industry priority. Since the PLL systems is used in various applications, there is no unique way to design this circuit. Hence, various combination of PCs, LFs, and VCOs can be considered to produce a flexible PLL circuit (Austin, 2002; Morgan, 2003;