WARPAGE BEHAVIOR OF THIN FCBGA PACKAGE AND PREDICTION OF ITS FIRST INTERCONNECT SnAg SOLDER JOINT SHAPE

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by

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LIST OF SYMBOLS

α	Coefficient of Thermal Expansion
α_c	CTE of composite material
α_m	CTE of composite of matrix
α_f	CTE of composite of fiber
μ	Poisson's ratio
μ_f	Poisson's ratio of fiber material
μ_m	Poisson's ratio of matrix material
χ	Contact angle between solder joint and substrate surface
E_m	Modulus of elasticity of matrix
E_f	Modulus of elasticity of phase (fiber)
E_c	Modulus of Elasticity of composite
R_r	Right solder joint fillet radius
R_l	Left solder joint fillet radius
S_r	Right solder spread from the die bump edge
S_l	Left solder spread from the die bump edge
V	Volume
θ_r	Right wetting angle
θ_l	Left wetting angle
CTE_{cx}	Curvature Coefficient of Thermal Expansion in x-direction
CTE_{cy}	Curvature Coefficient of Thermal Expansion in -direction
dL_{cx}	Curvature length delta in x-direction
dL_{cy}	Curvature length delta in y-direction
dL_x	Linear substrate expansion x-direction
dL_y	Linear substrate expansion y-direction

dh	Gap between center and edge
h_c	Gap height between die and substrate at the center of the die bump location
h_e	Gap height between die and substrate at the outermost die bump location

LIST OF ABBREVIATIONS

2D	2D IC (Two-Dimensional Integrated Circuit), die or dice are mounted in the package in a single plane.
2.5D	Die or dice are connected SiP through interposer
3D	2 or more dice stacked on top of each other
ABF	Ajinomoto Build Up Film
BGA	Ball Grid Array
BLT	Bond Line Thickness
C4	Controlled Collapse Chip Connection
CNW	Contact Non-Wet
CPU	Central Processing Unit
CTE	Coefficient of Thermal Expansion
DOE	Design of Experiment
EMIB	Embedded Multi-die Interconnect Bridge
FCBGA	Flip Chip Ball Grid Array
FEA	Finite Element Analysis
FR4	A NEMA grade designation for glass-reinforced epoxy laminate material
GPU	Graphics Processing Unit
HBM	High bandwidth memory
HTS	High Temperature Storage
I/O	Input/Output
MCM	Multi-Chip Module

NCO	Non-Contact Open
PCB	Printed Circuit Board
ppm	part per million
RDLs	Redistribution layers
Si	Silicon
SiP	System in Package
SnAg	Tin Silver Alloy
SAC305	Tin + 3% Silver+ 0.5% Copper Alloy
SB	Solder Bridging
SR	Solder Resist
SMT	Surface Mount Technology
SRO	Solder Resist Opening
TCB	Thermal Compression Bonding
Tg	Glass Transition Temperature
TSVs	Through-silicon vias
UBM	Under Bump Metal
UF	Underfill
um	Micron
WLP	Wafer Level Packaging

KELAKUAN PELEDINGAN PAKEJ NIPIS FCBGA DAN RAMALAN BENTUK SAMBUNGAN PATERI SnAg ANTARA-SAMBUNGAN PERTAMA

ABSTRAK

Pengaruh penyerakan ketumpatan tembaga substrat, kesamarataan benjolan substrat, proses pelekatan pengkaku, dan pengapitan substrat dengan bot magnetik semasa pemasangan dai terhadap kelakuan peledingan pakej FCBGA (Susunan Grid Bebola Cip Terbalik) telah dikaji secara terperinci. Kelakuan peledingan substrat sepanjang proses pemasangan pakej dicirikan dengan kaedah "Shadow Moire". Di dalam kajian ini, didapati bahawa kesimbangan penyerakan ketumpatan substrat tembaga (nisbah 50/50), penggunaan pra-pengkaku substrat sebelum pematerian benjolan cip terbalik, dan pengapitan substrat semasa pematerian mampu mengurangkan masalah sambungan pateri cip terbalik tercabut keluar. Pengurangan masalah sambungan pateri (<1%) ini disebabkan peledingan substrat yang rendah semasa pemasangan dai. Terutamanya, sambungan pateri tercabut keluar ini dapat dikorelasi dengan baik dengan peledingan kawasan pemasangan dai. Substrat dengan dan tanpa pengapitan semasa pematerian telah memenuhi keperluan kebolehpercayaan pakej di bawah 1200 suhu kitaran antara –40 °C hingga +125 °C. Kerja simulasi melalui Analisis Elemen Finit (AEF) terhadap peledingan substrat dan pakej telah dikaji dan dikorelasi dengan hasil eksperimen. Pelbagai sifat bahan dan reka bentuk pakej telah dikaji daripada korelasi model AEF dan kelakuan peledingannya telah difahami. Dengan pemahaman data peledingan melalui AEF, bentuk sambungan pateri SnAg dan penyambungan paterinya dapat difahami dengan perisian *Surface Evolver*. Kesan isipadu pateri, ketinggian jurang serta saiz UBM terhadap bentuk sambungan

pateri telah dikaji. Didapati isipadu pateri yang lebih besar dan ketinggian jurang yang lebih kecil akan meninggikan berlakunya penyambungan antara sambungan pateri. Pembentukkan sambungan pateri melalui teknologi tiang kuprum hujung pateri (*solder cap copper pillar*) ke atas substrat kuprum juga dijangkakan menggunakan *Surface Evolver*. Didapati geometri sambungan pateri tiang kuprum hasil simulasi daripada "Surface Evolver" berkorelasi baik dengan hasil eksperimen. Hubungan antara faktor-faktor seperti diameter benjolan dai, geometri pad kuprum, ketinggian dan isipadu pateri terhadap bentuk sambungan pateri berjaya ditentukan. Tahap optimum nisbah dai kepada lebar pad kuprum berjaya ditentukan daripada simulasi ini. Informasi ini boleh digunakan untuk menganggarkan isipadu kritikal pateri bagi reka bentuk pad kuprum yang baru dan berjarak lebih kecil supaya dapat membantu menjimatkan masa dan kos dengan mengelakkan perlunya bilangan eksperimen yang banyak sebelum penghasilan secara besar-besaran.

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ABSTRACT

The influence of substrate copper density distribution, substrate bump coplanarity, stiffener attach process, and substrate clamping by magnetic boat during die attach towards Flip Chip Ball Grid Array (FCBGA) assembled package warpage were evaluated. The substrate warpage behavior throughout the package assembly process was characterized using shadow moiré. In this study, it was found that a balanced substrate copper density distribution (50/50 ratio), pre-stiffener substrate before flip chip bump reflow, and substrate clamping during reflow able to reduce flip chip solder bridging fall-out. The decrease in solder bridging <1% was due to the lower substrate warpage seen during die attach. In particular, solder bridging fall-out was well-correlated to die attach area warpage. Substrate with and without clamping during reflow has met the package reliability requirement of temperature cycle 1200 condition G (–40 °C to +125 °C). Simulation works through FEA (ANSYS) on the bare substrate and package warpage was carried out and correlated to experiment data. Various material properties and package designs was evaluated from the correlated FEA model and its respective warpage behavior was understood. With understading of warpage data through FEA, SnAg solder joint shape and its solder bridging can be understood through Surface Evolver. The effect of solder volume, gap height and Under Bump Metalization (UBM) size towards solder joint was evaluated. Higher solder volume and smaller gap height led to higher occurrence of solder bridging. Solder joint formation through solder cap copper pillar onto copper trace was predicted through Surface Evolver. It can be shown that copper pillar solder joint geometry can be

successfully simulated and agreed with experiment. The relationship between various solder joint influencing factors such as die bump diameters, copper pad geometry, solder height and solder volume were established. The optimum die bump to copper pad width ratio can be obtained through this simulation work. The information can be used to estimate critical volume of solder needed for new, smaller pitch die bump and copper pad design which help to save cost and time by avoiding a large number of experiments prior to mass production.

CHAPTER 1:

INTRODUCTION

1.1 Introduction

Recent modern semiconductor packaging was driven by device miniaturization in order to meet the mobile devices such as laptop and mobile phones requirement. In certain section of the market, it demanded “near die size” type of packages in order to eliminate package cost and area. Figure 1-1 shows the semiconductor packaging trend evolved from low input/outputs (I/O) packages such as Dual In-line Package in 1970s to higher I/O density packages such as 2.5 D and 3D Integrated Circuits (IC). 2.5D and 3D IC packages are vertical integration on conventional 2D Flip Chip Ball Grid Array (FCBGA) and Flip chip Land Grid Array (FCLGA) platform (AnySilicon, 2016).

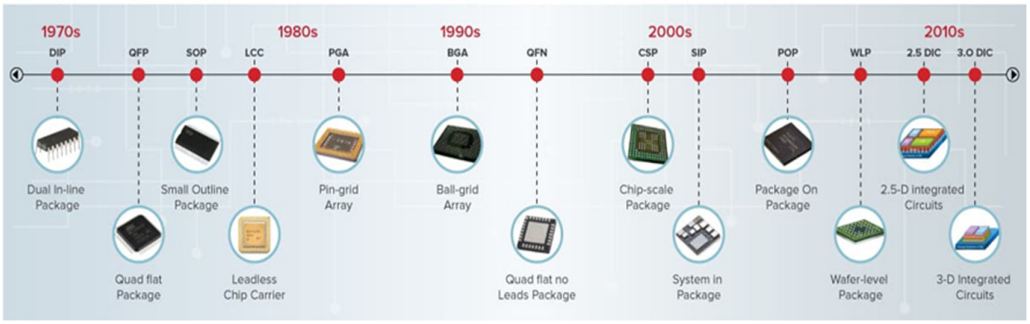

Figure 1-1 Semiconductor Packaging Trend Source (AnySilicon, 2016)

As market requirement to drive for higher speed and greater functionality of product, the increased in I/O density is inevitable. In order to pack more I/O on same foot print, bump to bump pitch was always the key factor to be scaled down from 500um pitch in 1970 to 40um pitch in year 2020 (Lau, 2016). This will allow product designer to pack more I/O which is expected to increase up to 50,000 bumps