UNIVERSITI SAINS MALAYSIA

Peperiksaan Semester Kedua
Sidang Akademik 2002/2003

Februari/Mac 2003

JEE 541 – ELEKTRONIK KUASA

Masa : 3 jam

ARAHAN KEPADA CALON:

Sila pastikan bahawa kertas peperiksaan ini mengandungi **SEMBILAN (9)** muka surat berserta Lampiran (6 mukasurat) bercetak dan **ENAM (6)** soalan sebelum anda memulakan peperiksaan ini.

Jawab **LIMA (5)** soalan.

Agihan markah bagi soalan diberikan disut sebelah kanan soalan berkenaan.

Jawab semua soalan di dalam Bahasa Malaysia.

S1. (a) Lakarkan simbol dan ciri *v-i* bagi peranti berikut:

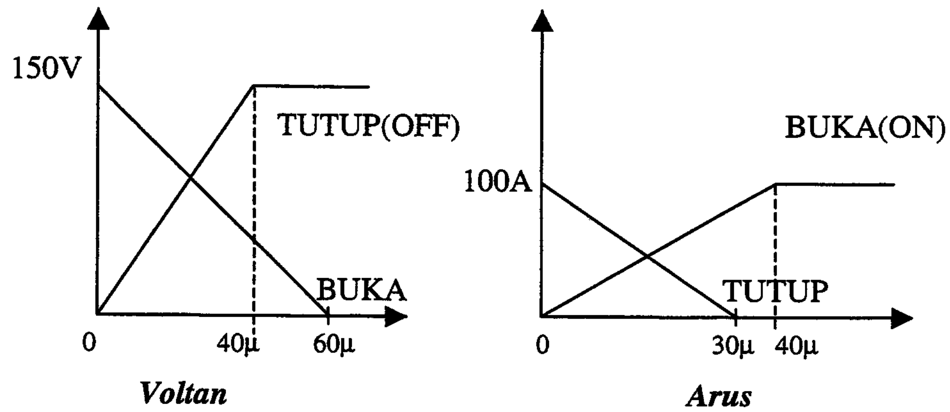
(i) GTO (ii) TRIAC (iii) SIT (iv) LASCR

(30%)

(b) Jelaskan kawasan pengendalian selamat bagi suatu peranti semikonduktor kuasa (SOA).

(20%)

(c) Satu suis mempunyai ciri pensuisan seperti ditunjukkan oleh Rajah 1. Jika purata kehilangan kuasa dihadkan ke nilai 600W, apakah kadar maksimum pensuisan yang boleh dicapai?



Rajah 1

(50%)

S2. (a) Jelaskan dengan ringkas kepentingan ***di/dt*** dan ***dv/dt*** sebagai pelindung dalam rekabentuk litar tiristor .

(20%)

(b) Huraikan kepentingan penyejukan dalam peranti semikonduktor kuasa.

(20%)

(c) Suatu peranti 2N6547 beroperasi dalam denyut berkala berfrekuensi 2 kHz. Untuk setiap tempoh 50μs berkala iaitu masa hidup, peranti mengalami kelesapan 80W, manakala untuk tempoh selain dari masa tersebut kehilangan adalah sifar. Gunakan data dari Lampiran 1. Jika T_A=75°C, R_{CS}=0.4°C/W, R_{CJ}=1.2°C/W dan T_J=150°C maksimum, kirakan:

(i) Nilai maksimum T_C yang dibenarkan

(ii) Nilai R_{SA} yang diperlukan.

(30%)

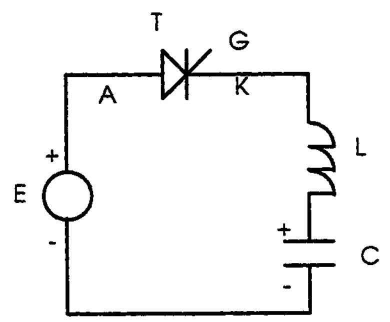
(d) Thiristor seperti ditunjukkan oleh Rajah 2a di HIDUPkan dan bentuk gelombang keluaran arus dan voltan ditunjukkan oleh Rajah 2b.

Jika $v_C(0)$ = 180 V, L= 120 μH dan C = 6μF hitung

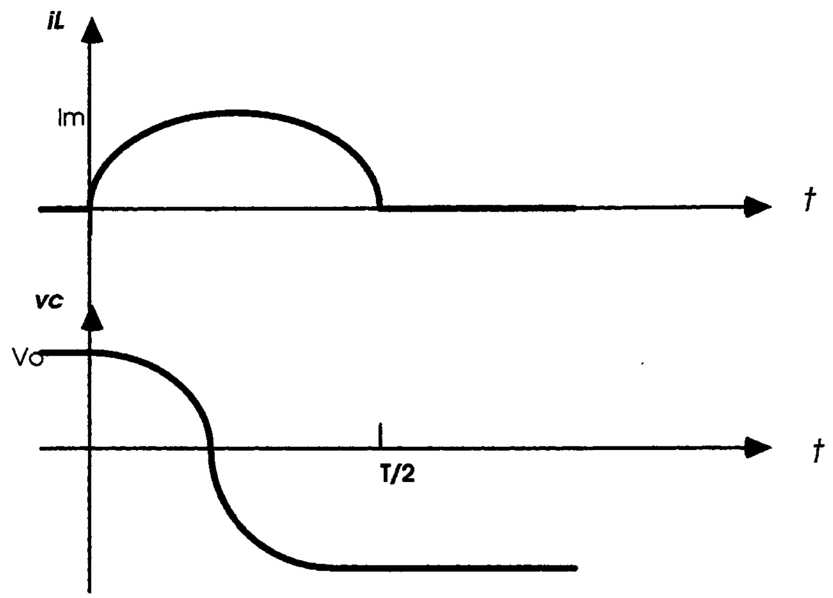
(i) arus puncak thiristor dan

(ii) tentukan berapa lama thiristor akan diHIDUPkan?

(30%)



Rajah 2a



Rajah 2b

S3. (a) Jelaskan prinsip litar rektifier satu fasa terkawal gelombang penuh beban R dan L.

(30%)

(b) Apakah kepentingan diod meroda bebas D_m dalam litar rektifier.

(20%)

(c) Litar rektifier seperti ditunjukkan oleh Rajah S3 dikendalikan dari punca 3 fasa sambungan Y, 208V, 60 Hz, mempunyai perintang R=20Ω. Jika voltan keluaran purata yang diperlukan ialah 60% dari voltan keluaran maksimum, kira:

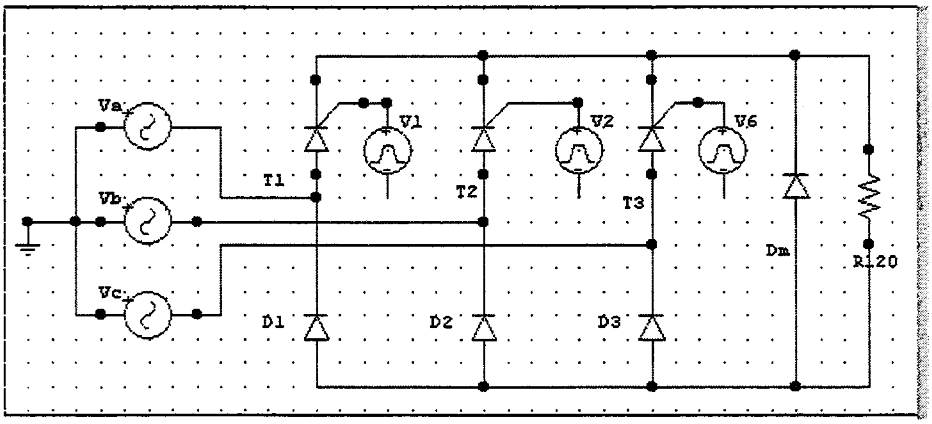
(i) Sudut lengah α

(ii) Arus rms dan arus purata beban

(iii) Arus rms dan arus purata thiristor

(iv) Faktor kuasa, PF.

(50%)



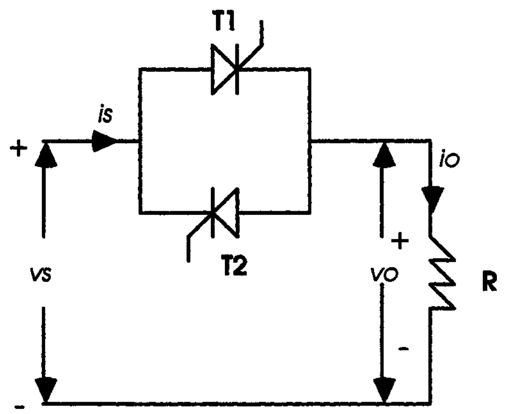
Rajah S3

S4. (a) Huraikan operasi litar pengawal ac satu fasa gabungan diod dan tiristor?

(20%)

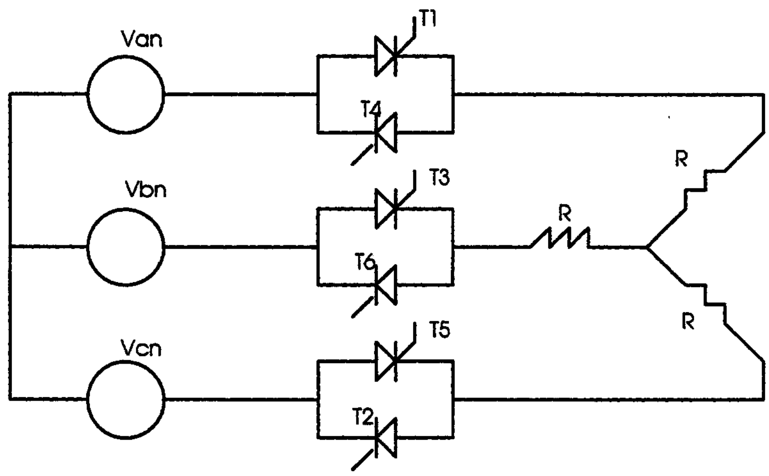
(b) Pengawal voltan ac satu fasa ditunjukkan oleh Rajah S4(a). Voltan V_s=240V rms, 50 Hz dan R=10Ω. Plotkan perubahan faktor kuasa lawan sudut lengah thiristor.

(40%)



Rajah S4(a)

(c) Litar pengawal ac 3 fasa ditunjukkan oleh Rajah S4(b). Lakarkan bentukgelombang voltan keluaran untuk sudut picuan 60°



Rajah S4b

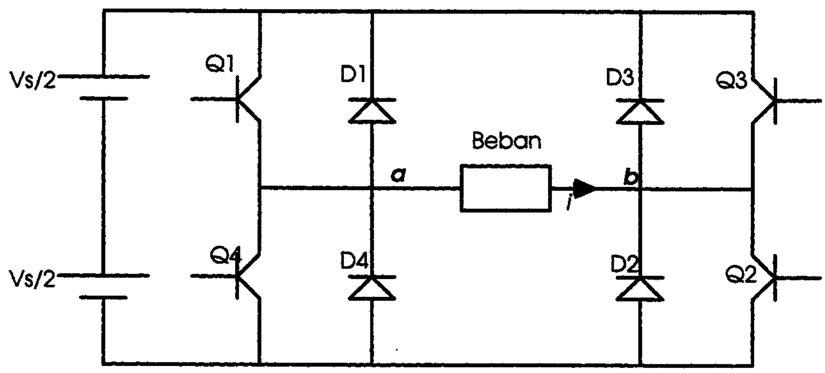
(40%)

S5. (a) Jelaskan dengan ringkas parameter prestasi bagi inverter.

(20%)

(b) Jelaskan operasi litar seperti ditunjukkan oleh Rajah S5.

(30%)



Rajah S5

(c) Inverter dalam Rajah S5 mempunyai beban $R=5\Omega$, $C=100\mu F$ dan $L=20mH$. Frekuensi operasi inverter ialah $f_o=60Hz$ dan $V_s=220V$. Terbitkan hubungan voltan talian seketika $V_{ab}(t)$ dan arus $i_a(t)$ dalam sebutan siri Fourier. Tentukan.

(i) Faktor harmonic THD

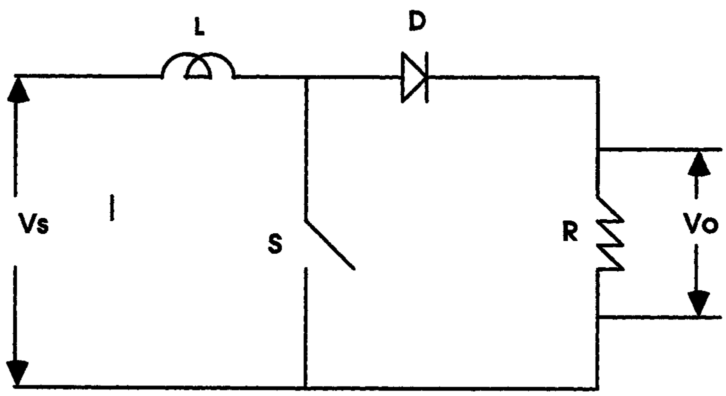
(ii) Jumlah herotan harmonik THD

(iii) Faktor herotan DF

(50%)

S6. (a) Jelaskan prinsip operasi pemenggal seperti ditunjukkan oleh Rajah S6(a).

(30%)



Rajah S6(a)

(b) Bagi pemenggal Buck-Boost seperti ditunjukkan oleh Rajah S6(b) terbitkan hubungan voltan dan arus untuk analisis arus berterusan.

(30%)

(c) Pemenggal dalam Rajah S6(b) membekalkan 200W, 60V ke perintang R dari punca voltan 20V. Jika T=150μs dan L=500μH tentukan:

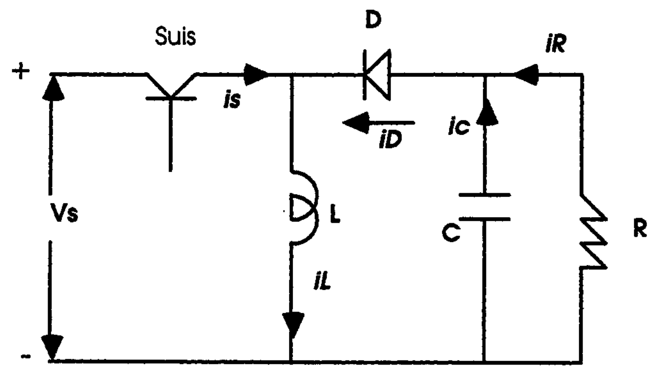
(i) Nilai kitar tugas k

(ii) I_{min} dan I_{mak}

(iii) Purata arus suis

(iv) Purata arus diod

(40%)



Rajah S6(b)

oooOooo

B.5 2N6546

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N6546
2N6547

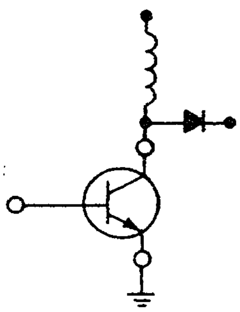
Designer's Data Sheet

SWITCHMODE SERIES
NPN SILICON POWER TRANSISTORS

The 2N6546 and 2N6547 transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for 115 and 220 volt line operated switch-mode applications such as:

- Switching Regulators
- PWM Inverters and Motor Controls
- Solenoid and Relay Drivers
- Deflection Circuits

Specification Features –
 High Temperature Performance Specified for:
 Reversed Biased SOA with Inductive Loads
 Switching Times with Inductive Loads
 Saturation Voltages
 Leakage Currents



15 AMPERE
NPN SILICON
POWER TRANSISTORS
300 and 400 VOLTS
175 WATTS

Designer's Data for "Worst Case" Conditions

The Designers Data Sheet permits the design of most circuits entirely from the information presented. Limit data – representing device characteristics boundaries – are given to facilitate "worst case" design.

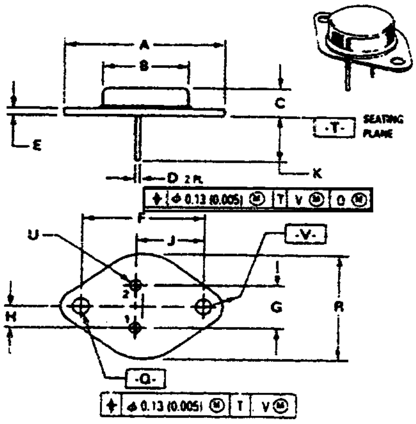
***MAXIMUM RATINGS**

Rating	Symbol	2N6546	2N6547	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	300	400	Vdc
Collector-Emitter Voltage	$V_{CEX(sus)}$	350	450	Vdc
Collector-Emitter Voltage	V_{CEV}	650	850	Vdc
Emitter Base Voltage	V_{EB}	9.0		Vdc
Collector Current – Continuous – Peak (1)	I_C I_{CM}	15 30		Adc
Base Current – Continuous – Peak (1)	I_B I_{BM}	10 20		Adc
Emitter Current – Continuous – Peak (1)	I_E I_{EM}	25 50		Adc
Total Power Dissipation @ $T_C = 25°C$ @ $T_C = 100°C$ Derate above 25°C	P_D	175 100 1.0		Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	T_L	275	°C

*Indicates JEDEC Registered Data
(1) Pulse Test: Pulse Width = 5.0 ms, Duty Cycle < 10%.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2. CONTROLLING DIMENSION: INCH
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	–	39.37	–	1.550
B	–	21.08	–	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.84	4.19	0.151	0.165
R	–	26.67	–	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

STYLE 1
 PIN 1. BASE
 2. EMITTER
 CASE COLLECTOR

CASE 1-06
TO-204AA
(TO-3)

B.5 2N6546 *cont'd*

*ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted.)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
Collector Emitter Sustaining Voltage (I_C = 100 mA, I_B = 0)	2N6546	$V_{CEO(sus)}$	300	–	Vdc
	2N6547		400	–	
Collector-Emitter Sustaining Voltage (I_C = 8.0 A, V_{clamp} = Rated V_{CEX}, T_C = 100°C)	2N6546	$V_{CEX(sus)}$	350	–	Vdc
	2N6547		450	–	
(I_C = 15 A, V_{clamp} = Rated V_{CEO} – 100 V, T_C = 100°C)	2N6546		200	–	
	2N6547		300	–	
Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)		I_{CEV}	–	1.0	mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 100°C)			–	4.0	
Collector Cutoff Current (V_{CE} = Rated V_{CEV}, R_{BE} = 50 Ω, T_C = 100°C)		I_{CER}	–	5.0	mAdc
Emitter Cutoff Current (V_{EB} = 9.0 Vdc, I_C = 0)		I_{EBO}	–	1.0	mAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with base forward biased t = 1.0 s (non-repetitive) (V_{CE} = 100 Vdc)		$I_{S/b}$	0.2	–	Adc
ON CHARACTERISTICS (1)					
DC Current Gain (I_C = 5.0 Adc, V_{CE} = 2.0 Vdc)		h_{FE}	12	60	–
(I_C = 10 Adc, V_{CE} = 2.0 Vdc)			6.0	30	
Collector-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)		$V_{CE(sat)}$	–	1.5	Vdc
(I_C = 15 Adc, I_B = 3.0 Adc)			–	5.0	
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	2.5	
Base-Emitter Saturation Voltage (I_C = 10 Adc, I_B = 2.0 Adc)		$V_{BE(sat)}$	–	1.6	Vdc
(I_C = 10 Adc, I_B = 2.0 Adc, T_C = 100°C)			–	1.6	
DYNAMIC CHARACTERISTICS					
Current-Gain – Bandwidth Product (I_C = 500 mAdc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)		f_T	6.0	28	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1.0 MHz)		C_{ob}	125	500	pF
SWITCHING CHARACTERISTICS					
Resistive Load					
Delay Time	(V_{CC} = 250 V, I_C = 10 A, I_{B1} = I_{B2} = 2.0 A, t_p = 100 μs, Duty Cycle ≤ 2.0%)	t_d	–	0.05	μs
Rise Time		t_r	–	1.0	μs
Storage Time		t_s	–	4.0	μs
Fall Time		t_f	–	0.7	μs
Inductive Load, Clamped					
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 100°C)	t_s	–	5.0	μs
Fall Time		t_f	–	1.5	μs
			Typical		
Storage Time	(I_C = 10 A(pk), V_{clamp} = Rated V_{CEX}, I_{B1} = 2.0 A, $V_{BE(off)}$ = 5.0 Vdc, T_C = 25°C)	t_s	2.0		μs
Fall Time		t_f	0.09		μs

*Indicates JEDEC Registered Data.
(1) Puse Test: Pulse Width ≈ 300 μs, Duty Cycle ≈ 2%.

B.5 2N6546 *cont'd*

TYPICAL ELECTRICAL CHARACTERISTICS

FIGURE 1 – DC CURRENT GAIN

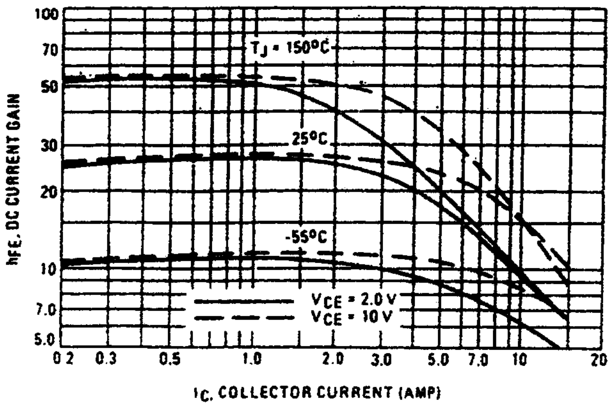


FIGURE 2 – COLLECTOR SATURATION REGION

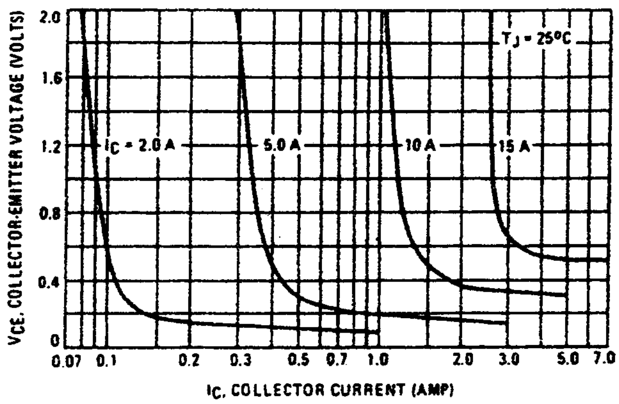


FIGURE 3 – "ON" VOLTAGE

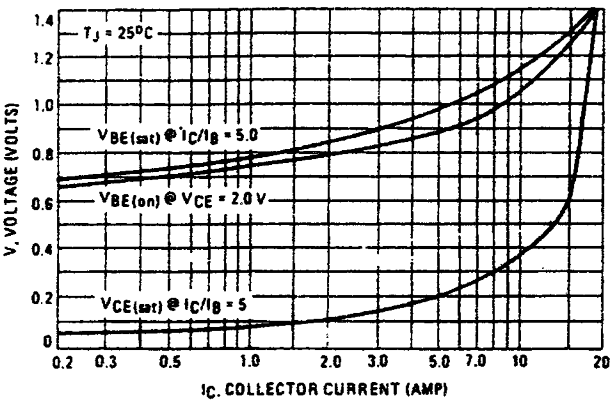


FIGURE 4 – TEMPERATURE COEFFICIENTS

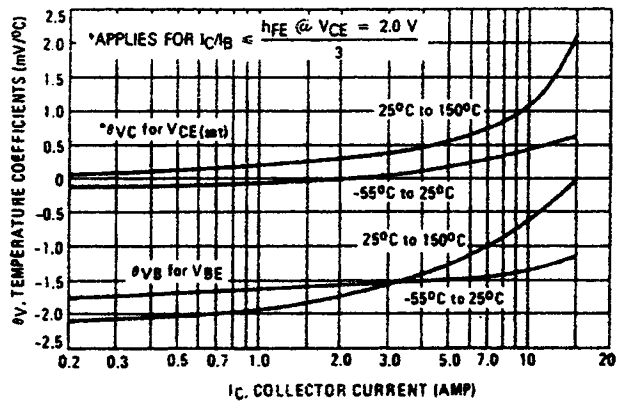


FIGURE 5 – TURN-ON TIME

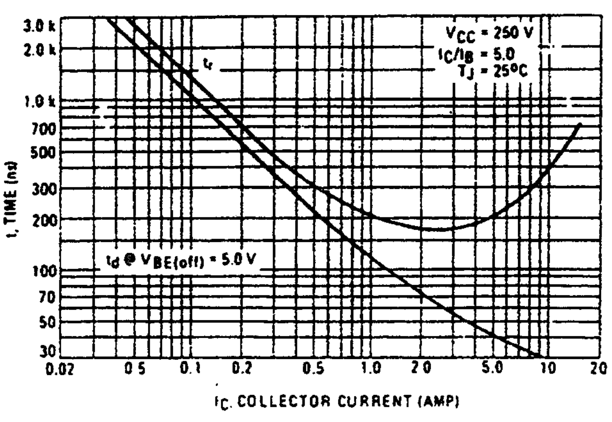
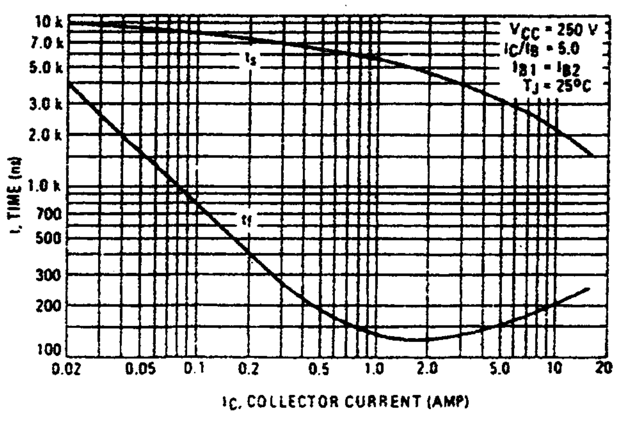


FIGURE 6 – TURN-OFF TIME



B.5 2N6546 *cont'd*

MAXIMUM RATED SAFE OPERATING AREAS

FIGURE 7 – FORWARD BIAS SAFE OPERATING AREA

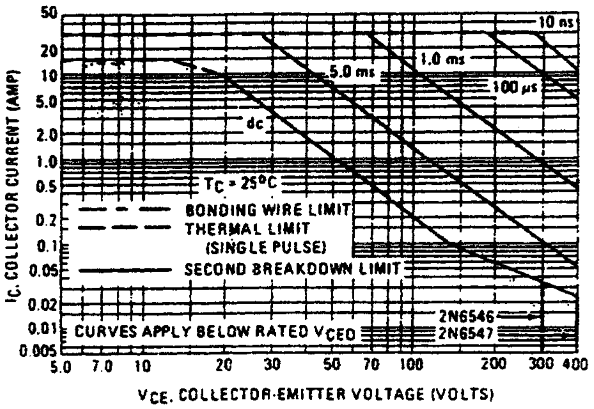


FIGURE 8 – REVERSE BIAS SAFE OPERATING AREA

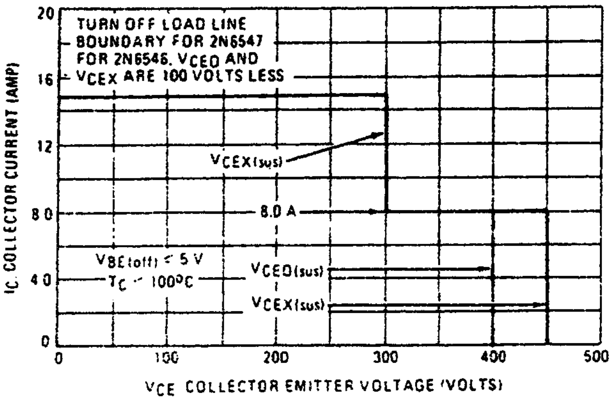
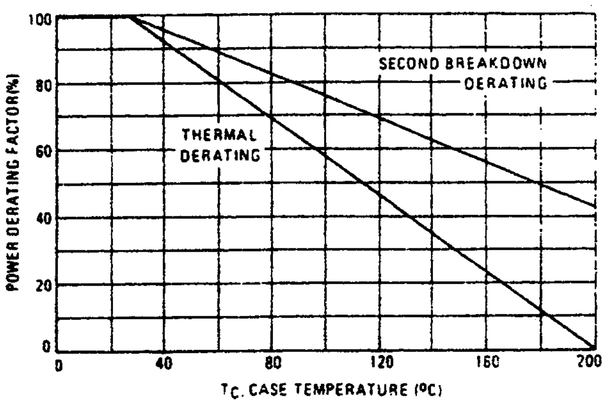


FIGURE 9 – POWER DERATING

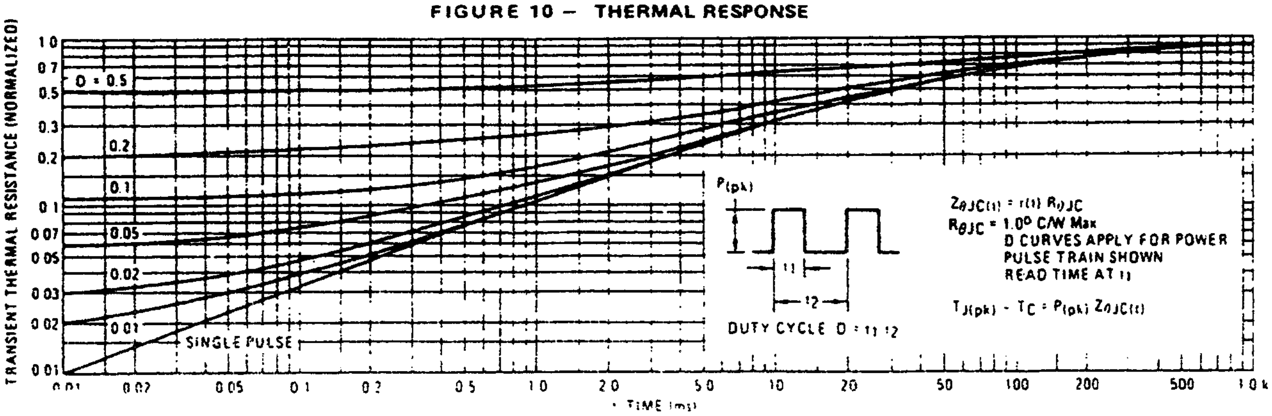


There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

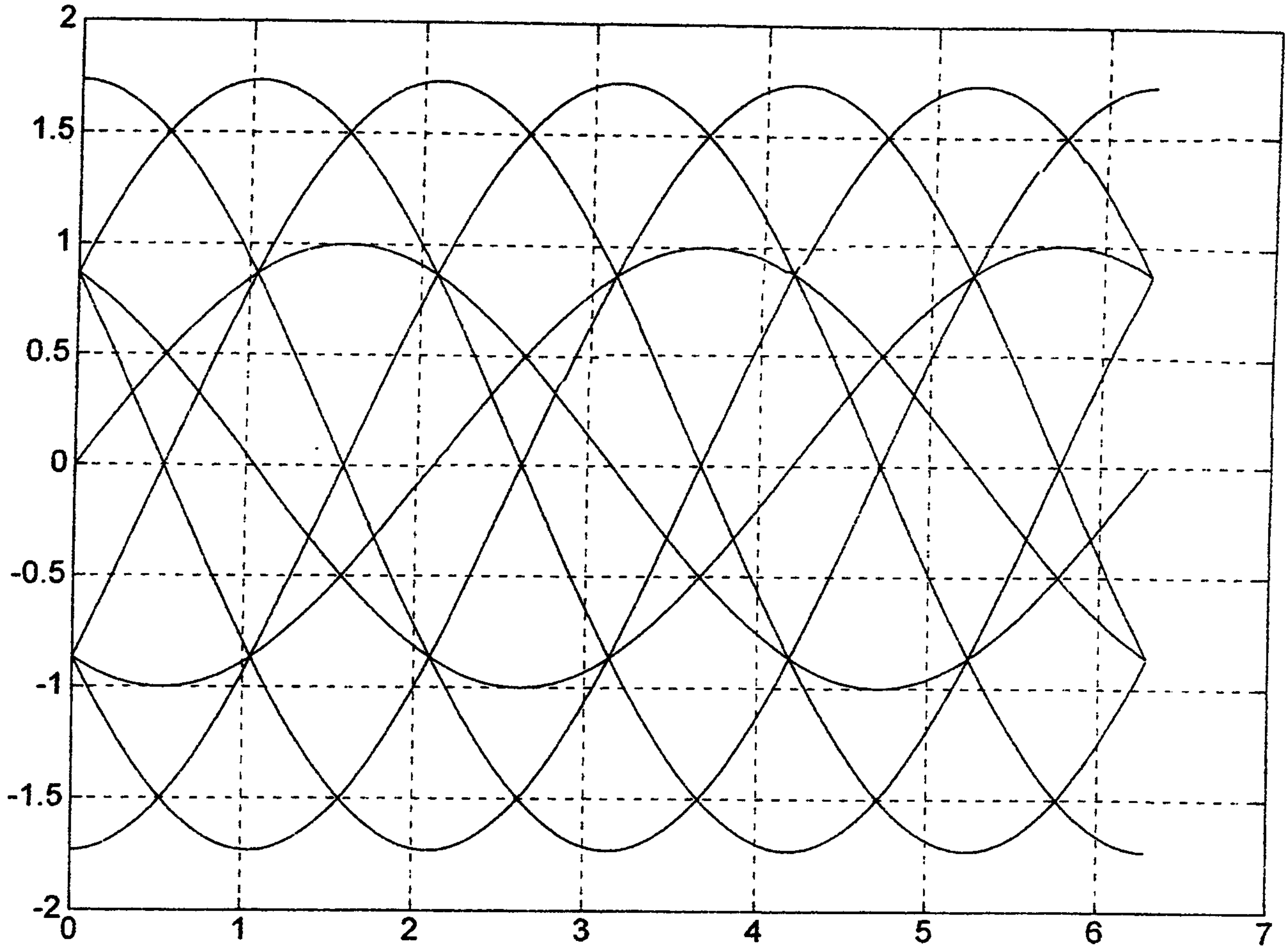
The data of Figure 7 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 7 may be found at any case temperature by using the appropriate curve on Figure 9.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 10 – THERMAL RESPONSE



Untuk Soalan 3



LAMPIRAN
Untuk Soalan 4