STABILITY IMPROVEMENT FOR THE LATENCY INSERTION METHOD BASED ON THE VERLET CONCEPT FOR SIGNAL AND POWER INTEGRITY SIMULATIONS

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by

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LIST OF ABBREVIATIONS

ADE	Alternating Direction Explicit
ADI	Alternating Direction Implicit
ADS	Advanced Design System
CFL	Courant-Friedrichs-Lewy
CIT	Complex Image Technique
CMOS	Complementary Metal-Oxide-Semiconductor
CPU	Central Processing Unit
DE	Discrete Element
DEM	Discrete Element Method
DGTD	Discontinuous Galerkin Time-Domain
EDA	Electronic Design Automation
EIP	Exchange Interaction Parameter
EM	Electromagnetic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
FDTD	Finite Difference Time Domain
FEEC	Finite Element Equivalent Circuit
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LIM	Latency Insertion Method
LU	Lower Upper
MNA	Modified Nodal Analysis
MOS	Metal-Oxide-Semiconductor
PCB	Printed Circuit Boards
PDN	Power Distribution Network
PEEC	Partial Element Equivalent Circuit
PI	Power Integrity
PSN	Power Supply Noise
RMSE	Root-Mean-Square Error

SDA	Spectral Domain Approach
SI	Signal Integrity
SPICE	Simulation Program with Integrated Circuit Emphasis
SSN	Simultaneous Switching Noise
SSO	Simultaneous Switching Output
VCC	Positive IC power supply pin
VIA	Vertical Interconnect Access
VRM	Voltage Regulator Modules
VSS	Negative IC power supply pin

PEMBAIKAN KESTABILAN UNTUK KAEDAH SISIPAN PENDAM BERASASKAN KONSEP VERLET UNTUK SIMULASI INTEGRITI ISYARAT DAN KUASA

ABSTRAK

Tesis ini membentangkan kaedah Latency Insertion Method (LIM) yang diubahsuai untuk simulasi integriti isyarat dan kuasa seperti dalam talian penghantaran, model litar 2-D dan model litar cip dengan pelbagai lapisan. LIM adalah salah satu teknik analisis yang pantas untuk simulasi model litar yang besar. Akan tetapi, disebabkan kelemahan formulasi eksplisit, teknik ini mempunyai saiz langkah masa yang terhad demi mematuhi syarat stabil analisis berangka, sama dengan teknik finite-difference time-domain (FDTD). Ini menimbulkan masalah terutamanya kepada model litar bermasalah di mana segolongan unit mempunyai induktans dan kapasitans yang amat kecil yang menyebabkan keperluan saiz langkah masa yang terlampau kecil. Dalam usaha untuk mengekalkan kestabilan LIM, syarat-syarat Courant-Friedrichs-Lewy (CFL) mestilah dipatuhi, iaitu mengehadkan saiz langkah masa yang pada dasarnya bergantung kepada kapasitans dan induktans yang terkecil dalam rangkaian model litar. Dalam tesis ini, kaedah inovasi LIM dengan pengamiran Verlet telah dibentangkan dengan tujuan untuk meningkatkan pretasi LIM dengan keupayaan stabil tanpa syarat tanpa kehilangan kejituan yang ketara. Kaedah yang dicadangkan telah diuji dengan tiga model litar yang berlainan termasuk keadaan litar bermasalah untuk setiap model. Semua simulasi menunjukkan yang hasil yang munasabah berbanding kaedah LIM biasa dengan kaedah yang dibentangkan. Kaedah LIM baru ini bukan sahaja mampu menunjukkan keupayaan stabil tanpa syarat tetapi kejituan yang mencapai 90% secara purata dengan 3 kali lebar saiz langkah masa berbanding dengan nilai maksimum daripada kaedah LIM biasa.

STABILITY IMPROVEMENT FOR THE LATENCY INSERTION METHOD BASED ON VERLET CONCEPT FOR SIGNAL AND POWER INTEGRITY SIMULATIONS

ABSTRACT

This thesis presents a modified Latency Insertion Method (LIM) that can be applied for signal and power integrity simulations of networks such as transmission lines, 2-D plane circuit model and multi-layered on-chip circuit model. LIM, as one of the transient analysis technique, is proven to be fast and reliable for large networks simulation. However, due to the behaviour of the explicit formulation, which derived from the finite-difference time-domain (FDTD) technique, shared the same limitation of the time step size to maintain its numerical stability. This creates a problem, particularly in ill-constructed circuit where a small number of elements possess smaller parasitic inductances and capacitances which necessitate the need for extremely small time step size. In order to maintain the LIM stability, one must comply with the Courant-Friedrichs-Lewy (CFL) condition, limiting the time step size which basically depends on the smallest inductance and capacitance of the entire network. In this thesis, an innovative LIM with Verlet concept has been proposed with the intention to enhance LIM with unconditional stability without sacrificing much on its accuracy. The proposed method has been tested on three different circuit model and each model included an ill-constructed condition. All the simulations show that feasible results which is similar to that of the normal LIM can be obtained through the proposed method. This improved LIM method gives not only unconditional stability, but accuracy up to 90% on average with a time step size of 3 times larger than the maximum time step size of normal LIM.

CHAPTER ONE

INTRODUCTION

1.1 Overview

The rapid advance in semiconductor technology is pushing the limit of the electronic system toward higher operating speed, lower power consumption, and smaller layout footprint, which create tremendous challenges for electronic designers. Besides that, with the trend moving towards deep sub-micron technology, which is focused on the increase of transistor density on-chip, the state-of-art on-chip interconnection feature size has achieved 10μm or less. The smaller the wire spacing, together with longer length in a larger chip, shorter cycle time, smaller power supply and fast switching speed, have led to significant noise problems in today's high-performance circuit. As a result, excessive noise can significantly affect the circuit performances and cause problems such as signal integrity (SI) [1] or additional delay [2]. Since the current design tools and work flows unable to capture the noise completely, system failures caused by signal and power integrity issues are unavoidable and this problems are on the rise. Therefore, power noise becomes increasingly important for circuit design engineers [3]-[4] because it directly reflects the performance and reliability of manufactured chips.

Signal integrity always refers to a set of interconnect design issues, such as crosstalk, ringing, distortion, etc. On the other hand, power integrity always refers to a set of power supply design issues, such as resonance, electro migration, voltage drop, and simultaneous switching noise (SSN), etc. Signal and power integrity check is becoming a necessity in current design flow as solving signal and power integrity

issues has becomes part of the design specification. In year 2002, international technology roadmap for semiconductors (ITRS) classify power noise management as one of the major challenges faced by the semiconductor industry in near future [5].

In general, power distribution network (PDN) for an electronic system normally contains voltage regulator modules (VRM), die, bulk capacitors, decoupling capacitors, printed circuit boards (PCBs), packaging and on-chip interconnects. PDN always refers to the power network that source from the VRM on the PCB and passing through stages of conducting structures collectively to the on-chip circuits. The PDN includes all the metal wires and vertical interconnect access (VIA) that deliver power to every gate in the chip. On-chip PDN is predominantly resistive but capacitive and inductive parasitic elements are also present. Specifically, due to the nonzero resistivity within the PDN, the supply voltage across the circuits is always less than the VRM supplied value. IR-Drop is generated due to the resistive elements of the PDN. Other than that, the voltage supply gets fluctuated when any circuit in the chip switches. Ground bounce is generated due to the inductive elements of the PDN. Normally, power supply noise (PSN) denotes the inconsistency of supply voltage from the VRM to the voltage that actually received by the circuits [6]-[9]. This power supply noise is also known as the simultaneous switching noise (SSN). The PSN can degrade the performance of the electronic system [6] by affecting the clock signal timing [10]-[11], which indirectly slows the system processing speed [12]-[13]. In some critical situation, PSN may bring logic failure [14] causing an error to the functionality of an electronic system.

Since the actual circuit network is always be nonzero resistivity, PSN is always going to be non-ideal. Although the PSN cannot be removed completely, it can be reduced and controlled. According to [15], the performance of the system is normally

unaffected if the amplitude of PSN is conserved under 10% of the ideal supply voltage. Therefore, modelling and simulating the PSN to ensure the functionality of the system before the project tape-out is a most common and cost effective way for industry practice. This simulation is used to ensure that the PSN is within the margin, given the geometry and switching source information.

1.2 Problem statement

Over the last decades, SPICE (Simulation Program with Integrated Circuit Emphasis) has become one of the popular simulation software as it contains the analysis and models needed to design integrated circuits with fast and reliable result for practical and industry usage. Either in academia or in industry, SPICE always served as a base for many other software and inspired the development in the circuit simulation field. The most prominent commercial versions of SPICE include HSPICE and PSPICE. PSPICE comes in with a schematic capture program that allow user to draw the schematic and automatically fit into the SPICE software. On the other hand, HSPICE allows user to select more integration method and customize it according to user preference.

The direct solver used by SPICE is based on Gauss elimination because it gives the most accurate result in solving the discretized system. However, depends on the sequences of nodes and the configuration of the circuit, using direct solver with a non-sparse matrix will increase the computational complexity. This can become practically unfeasible as the computational complexities can be scaled up to the second and third powers of the numbers of nodes. In order to reduce the computational complexity, obtaining a more efficient algorithm is more practical and feasible than optimizing the

SPICE. All the properties of the algorithm depend on the complexity of the equations, forms of the execution and the numerical integration rules that used for discretization. Later, researchers found out that the type of solver used to solve the full matrix is the most important key to improve the SPICE simulation steps.

The majority of the prior approaches on optimizing the SPICE was using a different solver other than the direct solver when it comes to the matrix solving part. The selection of the new solver include the iterative solvers [16]-[17] and the statistical solvers [18]-[19]. Unlike the direct solver, the iterative solver does not rely on the nodes configuration and thus it is comparatively computationally efficient. However, these new solvers show inadequacy either the accuracy or the convergence property compared to the original direct solver. Some approaches [20]-[21] try to reduce the complexity by dividing the full matrix into different smaller partition, solves it individually with the direct solver. Still, the computational complexity depends on the partitioning method and each partition size.

Later, Finite Difference Time Domain (FDTD) method was introduced and applied to the circuit simulation. It is an entirely new approach as it is not built upon SPICE derivatives. FDTD based approach [4]-[22] has the advantage over the SPICE based method as it usually results in a diagonal matrix where some mathematical method can be applied to improve the performance of direct solver. The solution becomes simpler and faster as the equation is now solved explicitly. These FDTD approaches have SPICE accuracy and numerical robustness. More importantly, these approaches offer a method where complexity scales linearly with the problem size.

A FDTD based method for circuits has been applied to simulate signal propagation in the transmission lines. Uniform transmission lines are done in [23] and a non-uniform transmission line are treated in [24]. In [24] the latency insertion method

is proposed where the FDTD method is augmented with artificial latency. LIM is able to generate SPICE accuracy, but it is only conditionally stable. The time step of the transient simulation cannot be arbitrary and depends on the smallest inductance and capacitance in the circuit. Just like any other FDTD based approach, LIM suffers from the Courant-Friedrichs-Lewy (CFL) condition where the simulation becomes unstable once the time step size is larger than the CFL upper bound limit. Thus, solving a large system using LIM with extremely small inductance or capacitance values requires an extremely small time step size and eventually burdens the computational dependency.

Throughout the years, a lot of effort had been made in order to overcome the CFL condition. Some hybrid implicit-explicit FDTD methods [25]-[26] have been proposed as an enhancement of the FDTD method. These methods try to relax the CFL condition without sacrificing much on the speed and accuracy. Next, alternating direction implicit (ADI) FDTD method [27] has been proposed to obviate the time step size issue. Although the ADI method is free from the time step size problem, its inconsistent performance varying on the circuit structure and the boundary condition becomes another issue. Therefore, the ADI algorithm is inappropriate for some circuit simulation especially PDN geometries. A block processing technique which utilizes the different time step size for each discretized circuit has been proposed [28]-[30]. Partitioning a large network according to the capacitance and inductance is indeed able to speed up the entire computational run time where each partitioned circuit calculation could have its own optimized time step size. Still, the partitioning method could be a problem if the circuit involves too many components with too many different values. In [31], an alternating direction explicit (ADE) LIM, adapted for solving the heat equation [32]-[33], significantly reduced the computational cost given its unconditionally stable behaviour and it's explicitly updating process. However, ADE-