Second Semester Examination
2018/2019 Academic Session

June 2019

EEE505 – Advanced Analog Integrated Circuit Design

Duration : 3 hours

Please check that this examination paper consists of SIX (6) pages and ONE (1) pages of printed appendix material before you begin the examination.

Instructions: This question paper consists of **SIX (6)** questions. Answer FIVE (5) questions. All questions carry the same marks.

Part A:

1. Investigate the cascode configuration of multi-transistor M_1 (common-source) and M_2 (common-gate) as shown in Figure 1 below.
Given $I_{D1} = I_{D2} = 250\ \mu A$, $W/L = 100$, $\lambda = 0.1\ V^{-1}$, $K'_n = \mu_n C_{ox} = 90\ \mu A/V^2$, $V_t = 0.7\ V$

   (a) Derive the expression for output resistance, R_O.

   (10 marks)

   (b) Determine the values for small-signal parameters;

   (i) Transconductance, G_M ($\approx g_m$).

   (4 marks)

   (ii) Output resistance, R_O.

   (4 marks)

   (iii) Open-circuit voltage gain, A_V.

   (2 marks)

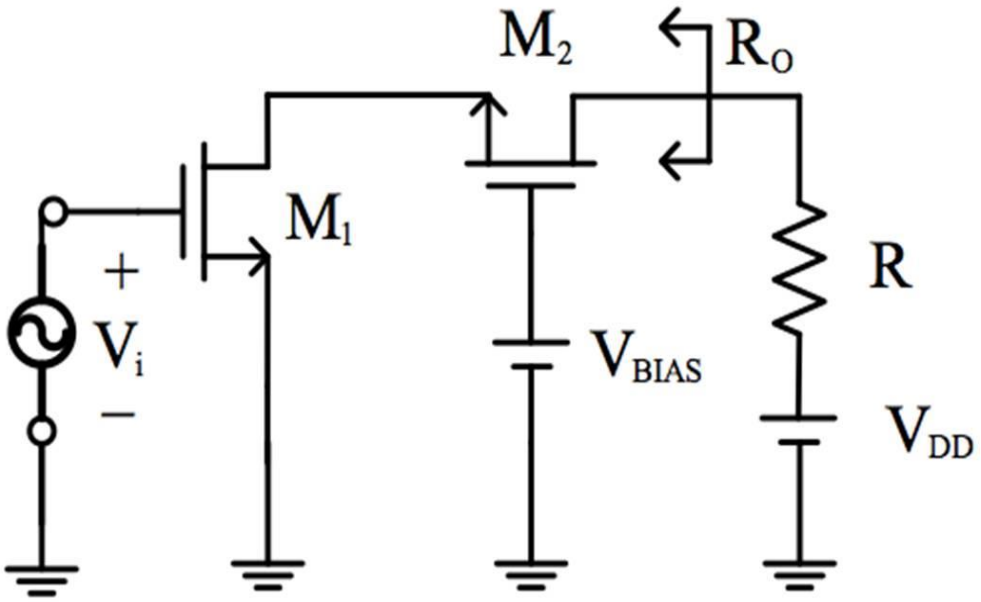

Figure 1.

2. For an active-loaded MOS differential amplifier shown in Figure 2, assume that for all transistors, W/L = 7.2 µm/0.36 µm, $\mu_n C_{ox}$ = 387 µA/V^2, $\mu_p C_{ox}$ = 86 µA/V^2, $|V'_{An}|$ = 5 V/ µm, $|V'_{Ap}|$ = 6 V/ µm, the bias current I_{TAIL} = 0.2 mA and Rss = 25 kΩ.

   (a) Determine the value of differential-mode gain, A_{dm}.
   (Note: No derivation needed)

   (15 marks)

   (b) Given the common-mode gain, A_{cm} = - 1/(2.g_m.Rss), determine the CMRR.

   (5 marks)

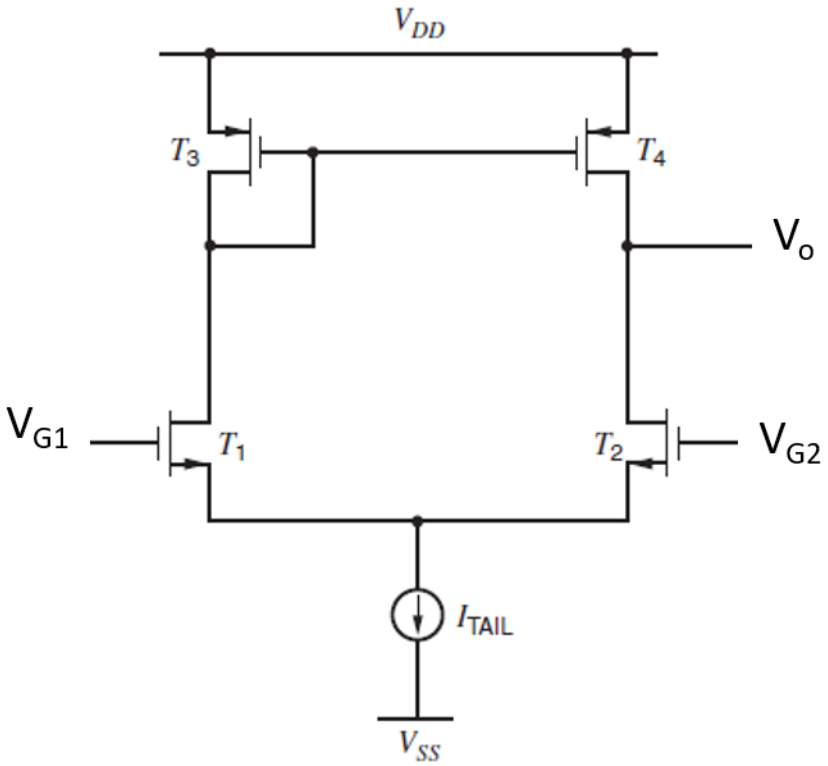

Figure 2.

3. Figure 3 refers to a current source design with all transistors are assumed to be operating in saturation region and both body-effect and channel-length modulation can be neglected.

   (a) Derive the expression for open-circuit voltage gain, A_V.

   (5 marks)

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(b) Derive the expression for output resistance, R_O.

(15 marks)

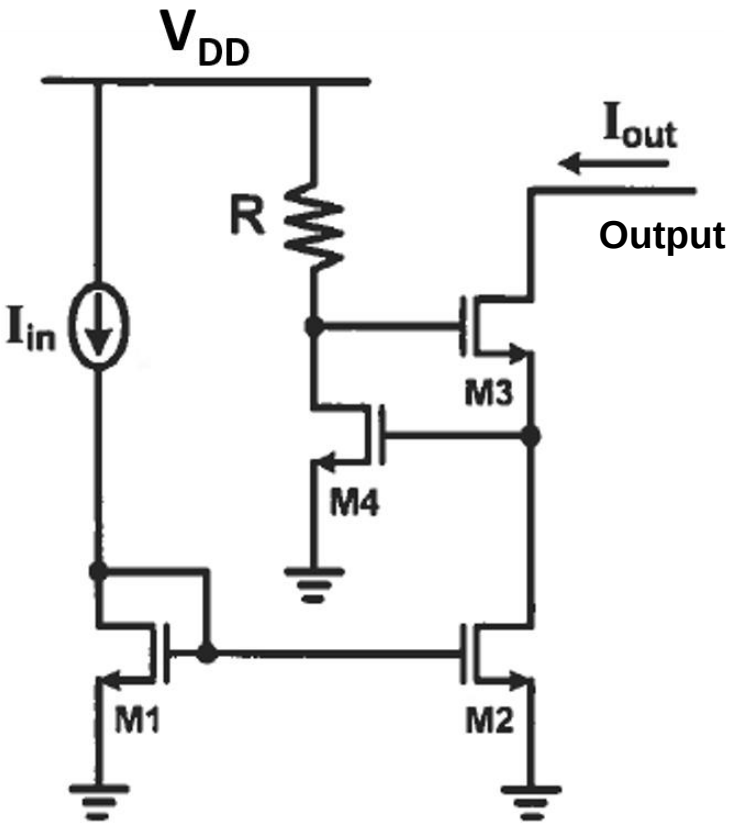

Figure 3

Part B:

4. (a) Figure 4 depicts the switched capacitor resistor circuit. By referring to the figure:

(i) Derive the equivalent resistance between v_1 and v_2 of the circuit in Figure 4.

(7 marks)

(ii) Calculate the resistance if the clock frequency is 0.5 MHz and C is 2 pF.

(3 marks)

(b) What is the operation of MOSFET whereby the behaviour of V_{GS} is similar as V_{BE} of bandgap device? Together with switched capacitor resistor, design a PTAT current generator. The final equation must be included together with the design.

(10 marks)

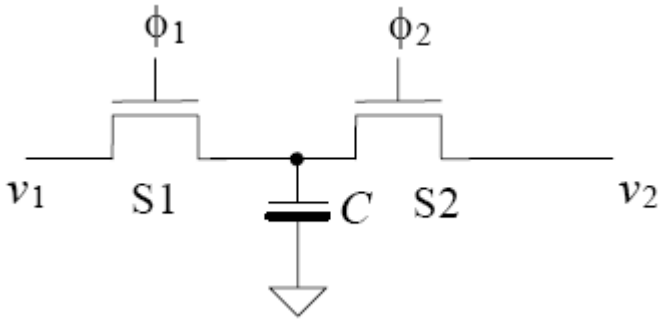

Figure 4

5. (a) State a simplified 3-bit DAC mathematical model. The model is based on current steering-resistor string approach. Draw the schematic of the DAC. Explain the functions of all the components in the schematic.

(12 marks)

(b) Extend the model up to 8-bit. Explain your model.

(8 marks)

6. (a) Figure 6 shows the biasing circuitries for a typical current steering DAC.

(i) Explain the function of the operational amplifier.

(2 marks)

(ii) What is the value of resistance R, if **I** is 1 mA and VREF = 1.2 V?

(2 marks)

(iii) Assuming VDD = 3.6 V and M1 is in saturation, W/L = 24/2, Vtp = -1, Kp = 40 μA/V^2 , calculate the required VSG of M1.

(6 marks)

(b) Draw the basic 8-bit DAC which must include the biasing circuitries and the DAC resistor string.

(10 marks)

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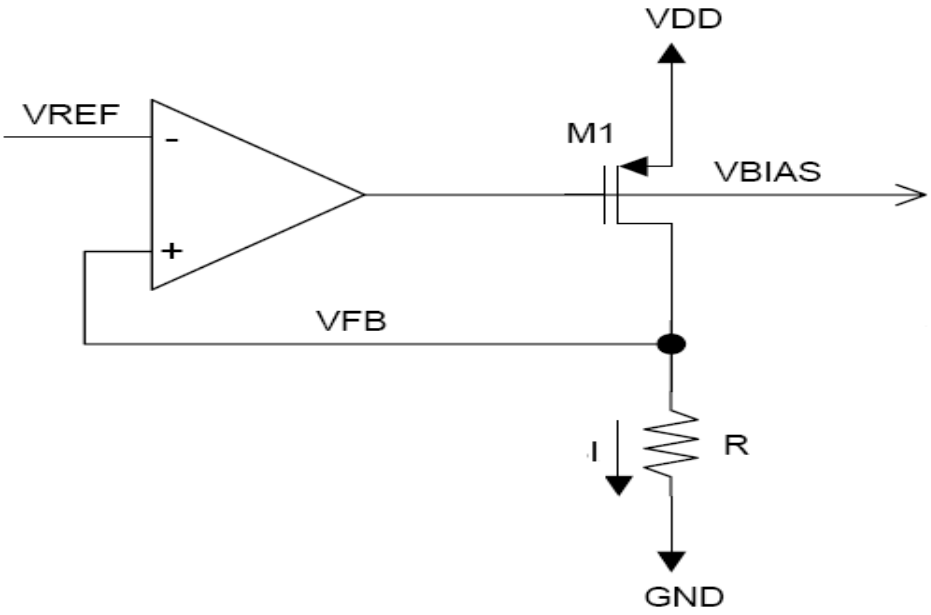

Figure 6

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APPENDIX

APPENDIX A

(b) NMOS Transistor Parameters

Quantity	Formula
Large-Signal Operation	
Drain current (active region)	$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{gs} - V_t)^2$
Drain current (triode region)	$I_d = \frac{\mu C_{ox}}{2}\frac{W}{L}[2(V_{gs} - V_t)V_{ds} - V_{ds}^2]$
Threshold voltage	$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{sb}} - \sqrt{2\phi_f}\right]$
Threshold voltage parameter	$\gamma = \frac{1}{C_{ox}}\sqrt{2q\epsilon N_A}$
Oxide capacitance	$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} = 3.45$ fF/μm² for $t_{ox} = 100$ Å
Small-Signal Operation (Active Region)	
Top-gate transconductance	$g_m = \mu C_{ox}\frac{W}{L}(V_{GS} - V_t) = \sqrt{2I_D\mu C_{ox}\frac{W}{L}}$
Transconductance-to-current ratio	$\frac{g_m}{I_D} = \frac{2}{V_{GS} - V_t}$
Body-effect transconductance	$g_{mb} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}g_m = \chi g_m$
Channel-length modulation parameter	$\lambda = \frac{1}{V_A} = \frac{1}{L_{\text{eff}}}\frac{dX_d}{dV_{DS}}$
Output resistance	$r_o = \frac{1}{\lambda I_D} = \frac{L_{\text{eff}}}{I_D}\left(\frac{dX_d}{dV_{DS}}\right)^{-1}$
Effective channel length	$L_{\text{eff}} = L_{\text{drwn}} - 2L_d - X_d$
Maximum gain	$g_m r_o = \frac{1}{\lambda}\frac{2}{V_{GS} - V_t} = \frac{2V_A}{V_{GS} - V_t}$
Source-body depletion capacitance	$C_{sb} = \frac{C_{sb0}}{\left(1 + \frac{V_{SB}}{\psi_0}\right)^{0.5}}$
Drain-body depletion capacitance	$C_{db} = \frac{C_{db0}}{\left(1 + \frac{V_{DB}}{\psi_0}\right)^{0.5}}$
Gate-source capacitance	$C_{gs} = \frac{2}{3}WLC_{ox}$
Transition frequency	$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd} + C_{gb})}$