Second Semester Examination
2018/2019 Academic Session

June 2019

EEE344 – *System VLSI*
*(*Sistem VLSI*)*

Duration : 2 hours
(Masa : 2 jam)

Please check that this examination paper consists of ELEVEN (11) pages of printed material before you begin the examination.

[Sila pastikan bahawa kertas peperiksaan ini mengandungi SEBELAS (11) muka surat yang bercetak sebelum anda memulakan peperiksaan ini.]

Instructions : This paper consists of **FOUR (4)** questions. Answer **FOUR (4)** questions.

*[**Arahan** : Kertas ini mengandungi **EMPAT (4)** soalan. Jawab **EMPAT (4)** soalan.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

1. (a) Explain the following region of enhancement n-MOSFET with an appropriate cross sectional MOSFET

(i) Depletion region

(ii) Inversion region

Terangkan rantau peningkatan n-MOSFET bersama keratan rentas MOSFET yang sesuai

(i) *Kawasan Susutan*

(ii) *Rantau penyongsangan*

(20 marks/*markah*)

(b) Refer to **FIGURE 1**

*Rujuk **RAJAH 1***

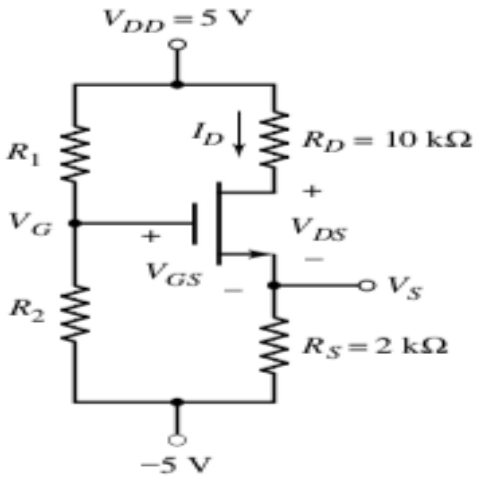

Figure 1

Rajah 1

Design the dc bias of a MOSFET based circuit as shown in Figure 1 to produce a specified drain current. Assume the MOSFET parameters are V_{TN} = 2V, K_n'= 80 μA/V^2, and W/L = 4, Choose R_1 and R_2 such that the current in the bias resistors is approximately one-tenth of I_D. Design the circuit such that I_D= 0.5 mA. In the final design, standard resistor values are to be used.

Reka pincang untuk litar MOSFET bagi menghasilkan spesifik arus sulir. Anggap MOSFET parameter adalah V_{TN} = 2V, K_n'= 80 μA/V^2, dan W/L = 4, Pilih R_1 dan R_2 di mana anggaran perintang pincang adalah satu-sepuluh I_D.

(30 marks/*markah*)

(c) Design an inverter with a resistive load by determining the value of load resistor R and the width of the nMOS transistor W, to meet following specification

$$P_{static} = 0.05mW, V_{OL} = 0.2V$$

Assume that the input voltage is low during 50% of the operation time and high during the other 50% and

$V_{DD} = 3.3V, V_{T0,n} = 0.75V, \mu_n C_{ox} = 60\mu A/V^2, L_n = 1\mu m.$

Neglect the channel-length modulation and substrate bias effect $(\lambda = 0, \gamma = 0)$

Rekabentuk sebuah penyongsang bersama beban perintang dengan menentukan nilai perintang R dan lebar saluran bagi transitor nMOS berdasarkan spesifikasi berikut

$$P_{static} = 0.05mW, V_{OL} = 0.2V$$

Anggap voltan masukan adalah rendah bagi 50% masa operasi dan tinggi bagi selebihnya dan $V_{DD} = 3.3V, V_{T0,n} = 0.75V, \mu_n C_{ox} = 60\mu A/V^2, L_n = 1\mu m.$ *Abaikan kesan perubahan panjang saluran dan substrate bias* $(\lambda = 0, \gamma = 0)$.

(50 marks/*markah*)

...4/-

2. (a) The design specification of a CMOS inverter is as follows:

V_{DD} = 3.3 V

$V_{TO,\ n}$ = 0.6 V

$V_{TO,\ p}$ = -0.7 V

K_n = 200 μA/V^2, K_p = 80 μA/V^2

Determine the noise margins of the circuit.

Spesifikasi rekabentuk penyonsang CMOS parameter:

V_{DD} = 3.3 V

$V_{TO,\ n}$ = 0.6 V

$V_{TO,\ p}$ = -0.7 V

K_n = 200 μA/V^2, K_p = 80 μA/V^2

Tentukan jidar hingar untuk litar tersebut.

(50 marks/*markah*)

(b) The input signal and corresponding output signal for an inverter are shown in Figure 2(b). Based on the graph given;

Isyarat input dan isyarat keluaran yang sepadan bagi penyongsang ditunjukkan dalam Rajah 2(b). Berdasarkan graf yang diberikan;

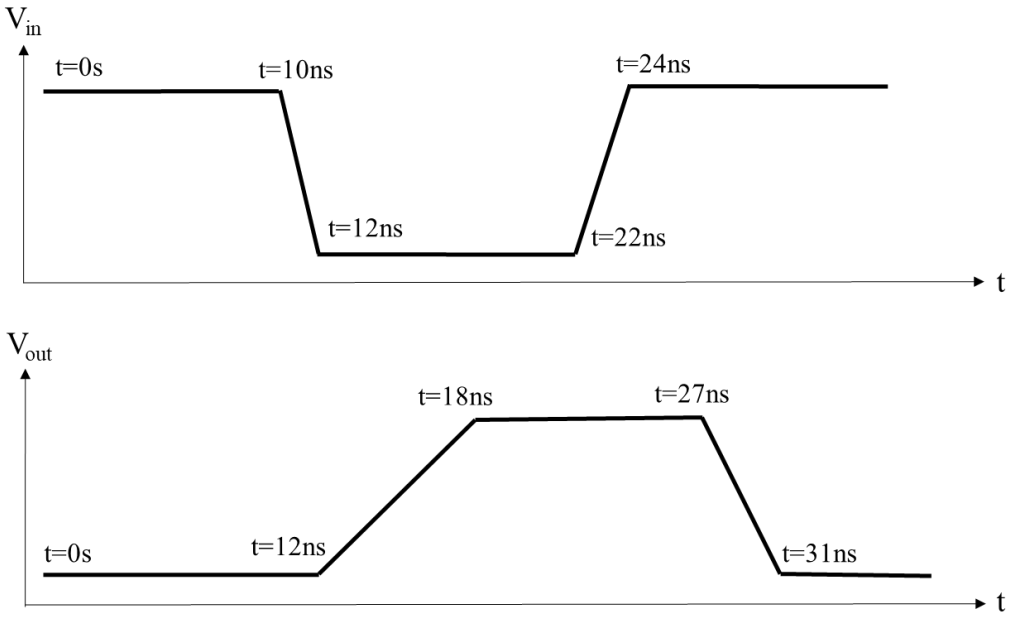

Figure 2(b)

Rajah 2(b)

(i) Calculate the rise time of the output.

Kirakan masa kenaikan keluaran

(5 marks/*markah*)

(ii) Calculate the fall time of the output.

Kirakan masa kejatuhan keluaran

(5 marks/*markah*)

(iii) Calculate the rising delay.

Kirakan kelewatan peningkatan

(5 marks/*markah*)

(iv) Calculate the falling delay.

Kirakan kelewatan penurunan

(5 marks/*markah*)

(c) Consider a CMOS inverter with the following device parameters for the transistors:

$$NMOS: V_{T0} = 0.8\,V, L = 1.0\mu m, \lambda = 0.0V^{-1}, \mu C_{ox} = 50\mu A/V^2$$
$$PMOS: V_{T0} = 1.0\,V, L = 1.0\mu m, \lambda = 0.0V^{-1}, \mu C_{ox} = 20\mu A/V^2$$

and assume the power supply voltage, V_{DD} is 5.0 V. The output load capacitance of this circuit is C_{out} = 2pF, which is independent of transistor dimensions.

Pertimbangkan penyongsang CMOS dengan parameter peranti transistor seperti berikut:

$$NMOS: V_{T0} = 0.8\,V, L = 1.0\mu m, \lambda = 0.0V^{-1}, \mu C_{ox} = 50\mu A/V^2$$
$$PMOS: V_{T0} = 1.0\,V, L = 1.0\mu m, \lambda = 0.0V^{-1}, \mu C_{ox} = 20\mu A/V^2$$

dan anggap voltan bekalan kuasa, V_{DD} ialah 5.0 V. Pemuat beban keluaran litar ini ialah C_{out} = 2pF, yang bebas daripada dimensi transistor.

(i) Determine the channel width of the NMOS and PMOS transistors such that the switching threshold voltage, V_{th} is equal to 2.2 V and the output rise time, T_{rise} = 5ns.

Tentukan lebar saluran transistor NMOS dan PMOS supaya voltan ambang V_{th} bersamaan dengan 2.2 V dan masa kenaikan keluaran, T_{rise} = 5ns.

(15 marks/*markah*)

(ii) Calculate the average propagation delay time for the circuit

Kirakan purata masa lengah perambatan untuk litar

(10 marks/*markah*)

(iii) How do the switching threshold V_M and the delay times change if the power supply voltage is dropped from 5 V to 3.3 V? Provide an interpretation of the results.

Bagaimanakah voltan ambang, V_M *dan masa lengah berubah jika voltan bekalan kuasa jatuh dari 5 V kepada 3.3 V? Berikan tafsiran hasilnya.*

(5 marks/*markah*)

3. (a) Figure 3(a) shows an enhancement load logic gate with;

- Pull-up transistor W/L = 5/5
- Pull-down transistor W/L = 100/5
- $V_{T0,\,n}$ = 1.0 V
- λ = 0.0 V^{-1}
- $\mu_n C_{ox}$ = 100 µA/ V^2
- γ = 0.4 $V^{1/2}$
- $|2\Phi_F|$ = 0.6 V

Rajah 3(a) menunjukkan penambah beban logik dengan;

- *Pull-up transistor W/L = 5/5*
- *Pull-down transistor W/L = 100/5*
- $V_{T0,\,n}$ *= 1.0 V*
- λ *= 0.0* V^{-1}
- $\mu_n C_{ox}$ *= 100 µA/* V^2
- γ *= 0.4* $V^{1/2}$
- $|2\Phi_F|$ *= 0.6 V*

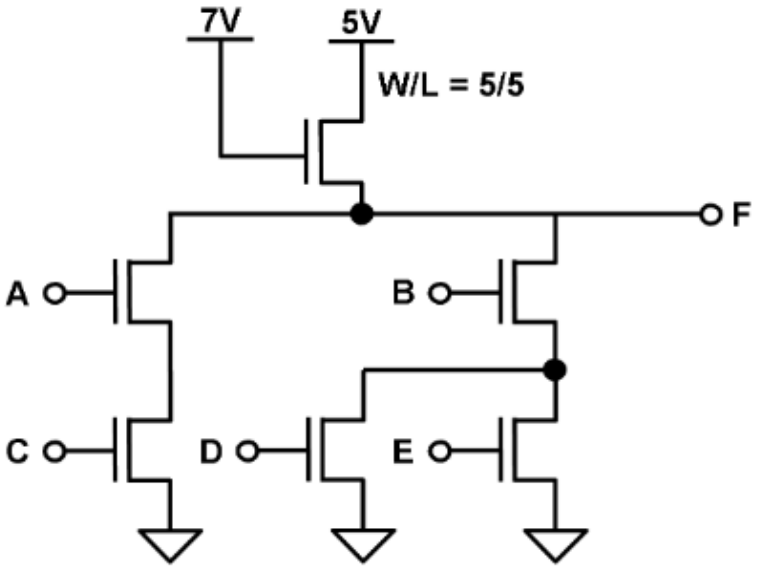

Figure 3(a)

Rajah 3(a)

(i) Write a Boolean expression for the output F as a function of the inputs.

Tulis ungkapan Boolean untuk output F sebagai fungsi input.

(5 marks/*markah*)

(ii) Identify the worse-case input combination(s) for V_{OL}.

Kenalpasti kombinasi input kes terburuk untuk V_{OL}.

(15 marks/*markah*)

(iii) Calculate the worse-case value of V_{OL}. Assume that all pull-down transistors have the same body bias and that, initially, $V_{OL} \approx 5\%$ of $V_{DD} = 5V$.

Kirakan nilai terburuk V_{OL}. Anggap bahawa semua transistor pull-down mempunyai berat yang sama dan pada mulanya $V_{OL} \approx 5\%$ of $V_{DD} = 5$ V.

(40 marks/*markah*)

(iv) Does the value of V_{OL} depends on $k_n = \mu_n C_{ox}$? Explain why or why not.

Adakah nilai V_{OL} bergantung kepada $k_n = \mu_n C_{ox}$? Terangkan mengapa atau mengapa tidak.

(5 marks/*markah*)

...8/-

(b) Figure 3(b) shows CMOS NAND2 gate with

- Two input switching simultaneously
- Top NMOS switching while the bottom NMOS's gate is tied to Vdd
- Top NMOS gate is tied to Vdd and the gate input of the bottom NMOS is changing

Use $k_n = k_p = 100\ \mu A/V^2$

Rajah 3(b) menunjukkan get CMOS NAND2 dengan

- *Dua input suis serentak*
- *NMOS bahagian atas bertukar manakala get NMOS bahagian bawah terikat kepada Vdd*
- *NMOS bahagian atas terikat kepada Vdd dan input get NMOS bahagian bawah bertukar*

Guna $k_n = k_p = 100\ \mu A/V^2$

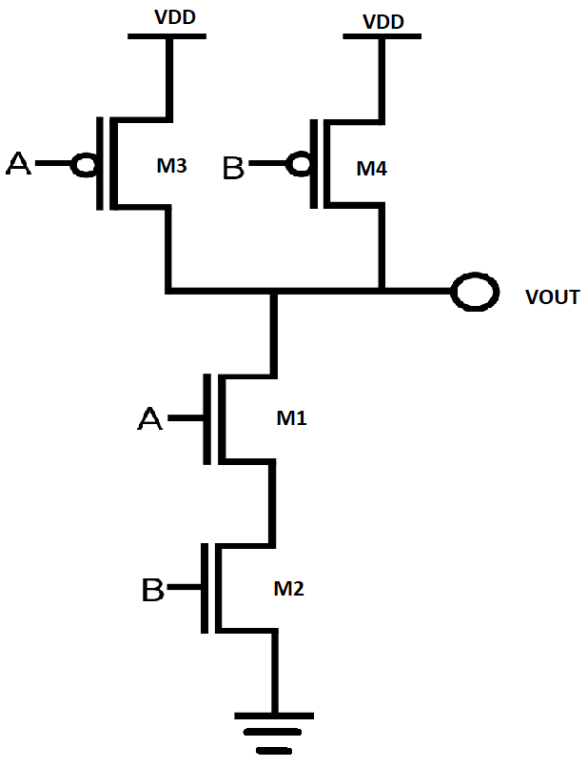

Figure 3(b)

Rajah 3(b)

(i) Derive an analytical expression for V_{th} corresponding to the first case.

Terbitkan unggkapan analisis untuk V_{th} bersamaan dengan kes pertama

(25 marks/*markah*)

(ii) Calculate the Vth base on (i) for the first case for V_{dd} =5 V when the magnitude of the threshold voltages are V_{Tn} =1 V, V_{Tp} = 1 V with γ = 0.

Kirakan Vth berdasarkan dengan (i) kes pertama untuk V_{dd} =5 V apabila magnitud voltan ambang adalah V_{Tn} =1 V, V_{Tp} = 1 V dengan γ = 0.

(10 marks/*markah*)

4. (a) Based on Figure 4a, the circuit is designed to drive a total capacitive load of C_L = 0.2 pF. For the NMOS devicse, assume V_{TO} = 1.0 V and k'$_n$ = 50 μA/V^2. For the PMOS devices, assume V_{TO} = -1.0 V and k'$_p$ = 25 μA/V^2. For all the devices, assume the W/L ratios for each device is shown in the figure. The initial voltage across the C_L is 0 V. The signal at input *E* is 0 V for all time. For the rest of the input, the signals are shown in the figure.

Berdasarkan Rajah 4a, litar ini direka untuk memacu 0.2 pF beban pemuat. Untuk peranti NMOS, andaikan V_{TO} = 1.0 V and k'$_n$ = 50 μA/V^2. Untuk peranti PMOS, andaikan V_{TO} = -1.0 V and k'$_p$ = 25 μA/V^2. Untuk semua peranti, andaikan nisbah W/L untuk setiap transistor adalah seperti dalam rajah. Voltan asal bagi C_L ialah 0 V. Isyarat signal dimasukkan E ialah 0 V pada setiap masa. Manakala untuk semua isyarat yang lain adalah seperti di dalam rajah.

(i) Calculate the time it takes for voltage across C_L to reach 50% of V_{DD}.

Kirakan masa supaya voltan bagi C_L adalah 50% daripada V_{DD}.

(40 marks/*markah*)

(ii) Sketch the voltage waveform across C_L. Mark the 50% crossing along the time axis.

Lukiskan bentuk gelombang voltan C_L dan dengan jelas tandakan silang 50% pada paksi masa

(10 marks/*markah*)

...10/-

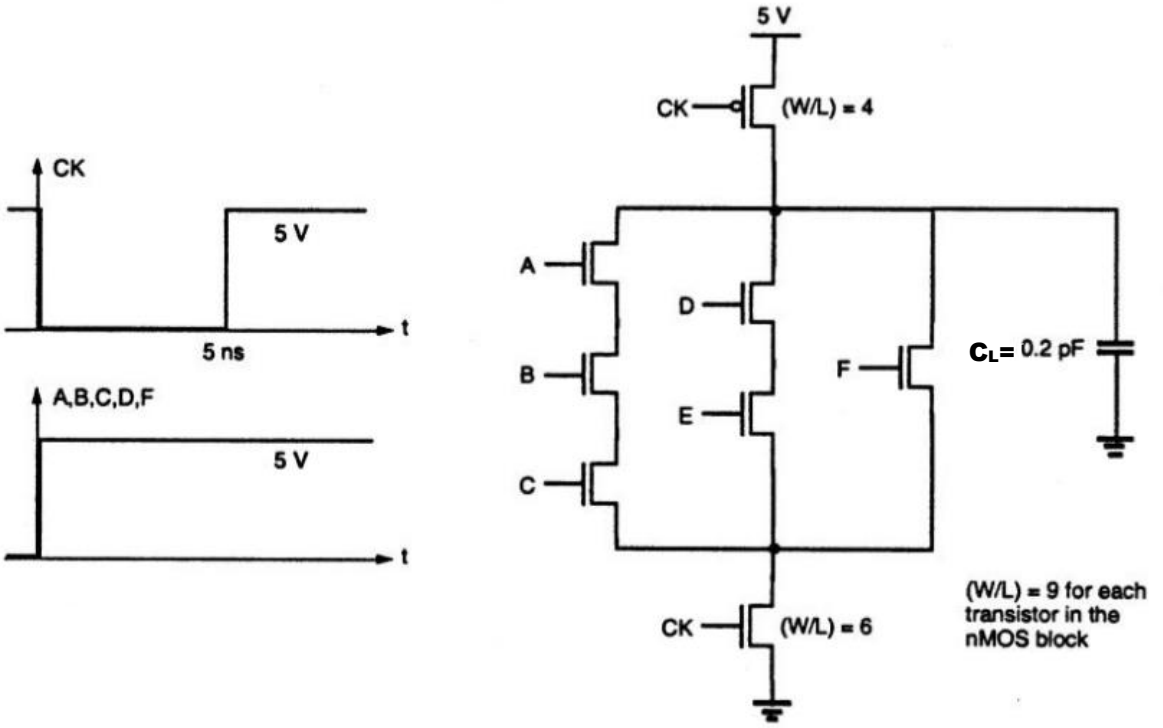

Figure 4(a)

Rajah 4(a)

(b) (i) What is volatile memory and non-volatile memory?

Apakah ingatan meruap dan ingatan tak meruap?

(10 marks/*markah*)

(ii) Based on Figure 4b, a single-transistor DRAM cell bit line is precharged to $V_{DD}/2$ by using a clocked precharge circuit. The *WRITE* circuit is assumed here to bring the potential of the bit line to V_{DD} or 0 V. Assume V_{TO} = 1.0 V, γ = 0.3 $V^{1/2}$ and $|2\phi_F|$=0.6 V. By ignoring the leakage current in the circuit, calculate the voltage at the bit line during Read-1 operation after bit line is first precharged to $V_{DD}/2$.

Berdasarkan Rajah 4b, talian bit sel DRAM satu transistor dicaskan kepada $V_{DD}/2$ dengan menggunakan litar precas berjam. Litar WRITE diandaikan digunakan untuk memastikan voltan talian bit kepada V_{DD} or 0 V. Sekiranya V_{TO} = 1.0 V, γ = 0.3 $V^{1/2}$ and $|2\phi_F|$=0.6 V. Dengan mengendahkan arus bocor, kirakan voltan pada talian bit semasa operasi Read-1 selepas talian bit telah dicaskan kepada $V_{DD}/2$.

(40 marks/*markah*)

...11/-

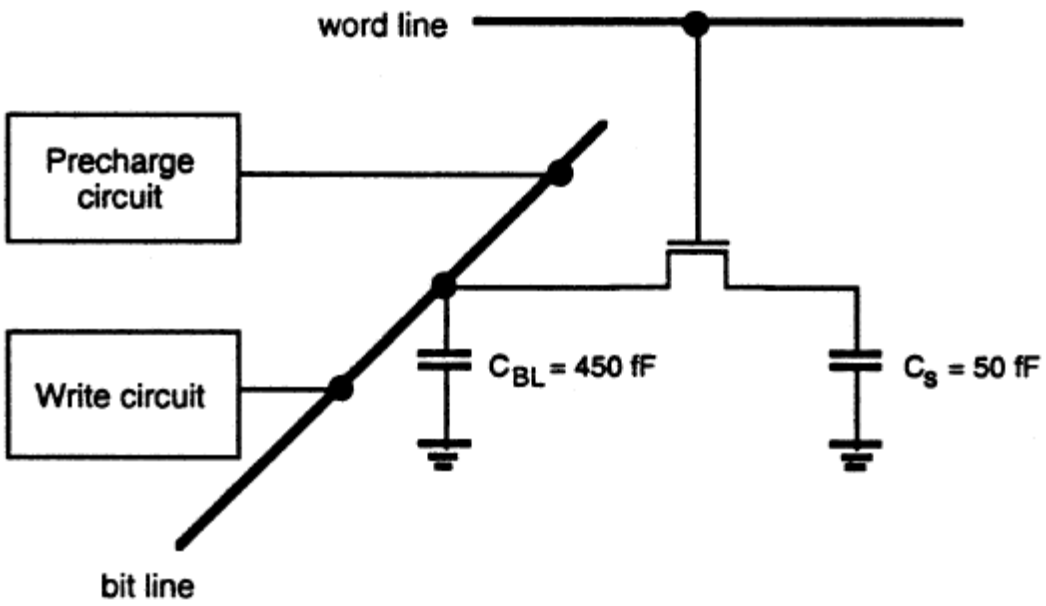

Figure 4(b)

Rajah 4(b)

-oooOooo-