Second Semester Examination
2018/2019 Academic Session

June 2019

EEE270 – Analog Circuit II
(Litar Analog II)

Duration : 3 hours
(Masa : 3 jam)

Please check that this examination paper consists of EIGHT (8) pages and ONE (1) apendix before you begin the examination.

[Sila pastikan bahawa kertas peperiksaan ini mengandungi LAPAN (8) muka surat dan SATU (1) lampiran yang bercetak sebelum anda memulakan peperiksaan ini.]

Instructions : This paper consists of **FIVE (5)** questions. Answer **ALL** questions. All questions carry the sama marks.

*[**Arahan** : Kertas ini mengandungi **LIMA (5)** soalan. Jawab **SEMUA** soalan. Semua soalan membawa jumlah markah yang sama.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

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1. Design a differential amplifier as shown in Figure 1. The gain, A_{DM} for the amplifier should be around 20 dB and differential-mode output resistance, R_{od} of 10 kΩ. Given value for $V_{DD} = V_{SS} = 5$ V. Assume $V_{TN} = 1$ V and $K_n = 25$ mA/V^2. Use a correct estimation (rule-of-thumb) to check feasibility of your design before starting with design calculation of the circuit. Then, find:

   Reka bentuk satu litar penguat kebezaan seperti ditunjukkan oleh Rajah 1. Nilai gandaan, A_{DM} bagi litar penguat harus dalam lingkungan 20 dB dan rintangan keluaran mod-kebezaan, R_{od} adalah bernilai 10 kΩ. Nilai diberikan ialah $V_{DD} = V_{SS} = 5$ V. Anggap $V_{TN} = 1$ V and $K_n = 25$ mA/V^2. Gunakan anggaran yang betul (rule-of-thumb) sebelum memulakan proses pengiraan bagi reka bentuk litar tersebut. Kemudian, dapatkan:

   (a) Sketch the small signal models for differential-mode and common-mode of this circuit.

   Lakarkan model isyarat kecil mod-kebezaan dan mod-sepunya bagi litar ini.

   (20 marks/*markah*)

   (b) Transconductance, g_m

   Transkonduktan, g_m

   (20 marks/*markah*)

   (c) Resistance, R_D and R_{SS}

   Rintangan R_D and R_{SS}

   (30 marks/*markah*)

   (d) Current, I_D

   Arus, I_D

   (20 marks/*markah*)

   (e) Estimation value of CMRR for this circuit

   Anggaran nilai CMRR bagi litar ini

   (10 marks/*markah*)

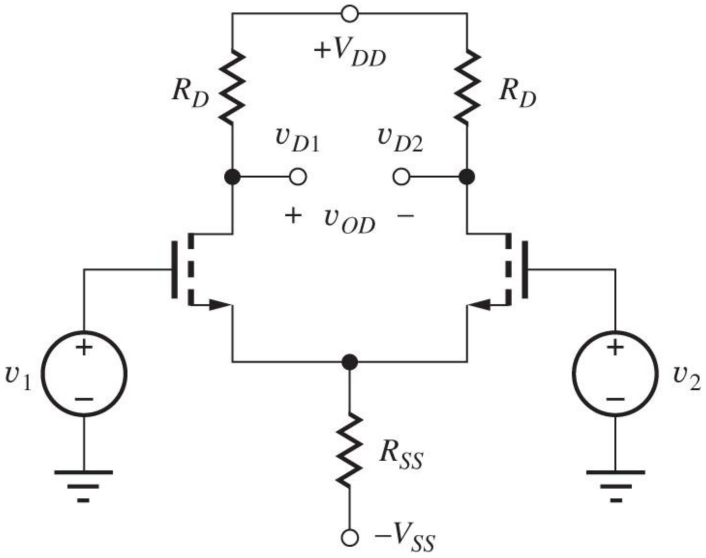

Figure 1

Rajah 1

2. Analyze the circuit of Figure 2. Given values are: $V_{CC} = V_{EE} = 5$ V, $I_1 = 200$ μA, $I_2 = 500$ μA, $I_3 = 2$ mA, $R_L = 2$ kΩ, $R_1 = 2$ MΩ.. Assume $V_A = 70$ V, $V_{TN} = 0.7$ V, $K_n = 5$ mA/V^2 dan $\beta_o = 100$. Based on the given values, find:

Analisa litar Rajah 2. Nilai-nilai yang diberikan adalah: $V_{CC} = V_{EE} = 5$ V, $I_1 = 200$ μA, $I_2 = 500$ μA, $I_3 = 2$ mA, $R_L = 2$ kΩ, $R_1 = 2$ MΩ. *Anggap* $V_A = 70$ V, $V_{TN} = 0.7$ V, $K_n = 5$ mA/V^2 *dan* $\beta_o = 100$. *Berdasarkan nilai-nilai tersebut, dapatkan:*

(a) Q-points values

Nilai-nilai titik-Q

(30 marks/*markah*)

(b) Differential mode voltage gain, A_{dm}

Gandaan voltage mod kebezaan, A_{dm}

(40 marks/*markah*)

(c) CMRR

CMRR

(10 marks/*markah*)

(d) Input resistances, R_{id} and R_{out}

Rintangan masukan, R_{id} *dan* R_{out}

(20 marks/*markah*)

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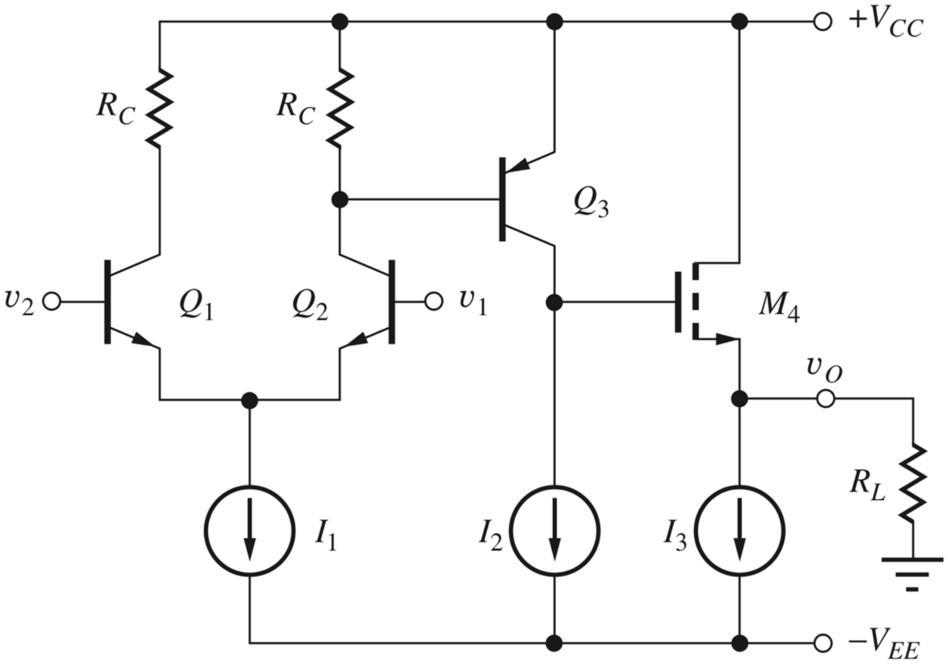

Figure 2

Rajah 2

3. (a) Calculate the current, I_d in the circuit of Figure 3 (a). Given values are: V_{TN} = 0.75 V, V_{TP} = -0.75 V, K_n = 400 μA/V^2, K_p = 200 μA/V^2, I_G = 500 μA and R_G = 4 kΩ.

Kirakan arus, I_d bagi litar Rajah 3 (a). Nilai-nilai yang diberikan adalah: V_{TN} = 0.75 V, V_{TP} = -0.75 V, K_n = 400 μA/V^2, K_p = 200 μA/V^2, I_G = 500 μA dan R_G = 4 kΩ.

(20 marks/*markah*)

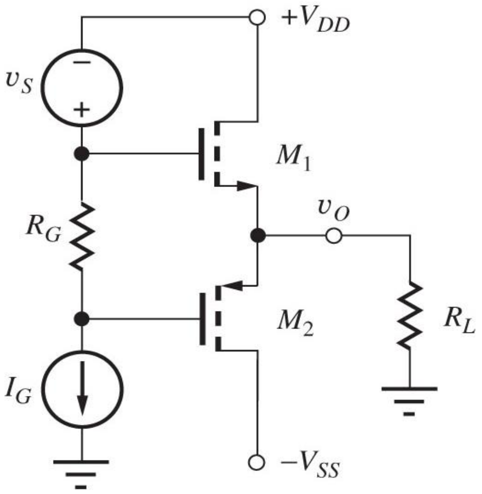

Figure 3 (a)

Rajah 3 (a)

(b) Calculate the output current and output resistance, I_o and R_{out} in the circuit of Figure 3 (b). Given values are:
$V_o = V_{DD} = 12$ V, $R_3 = 330$ kΩ, $R_4 = 680$ kΩ, $R_S = 3$ kΩ, $K_n = 500\ \mu A/V^2$, $V_{TN} = 0.7$ V and $\lambda = 0.01\ V^{-1}$.

Kirakan arus keluaran dan rintangan keluaran I_o dan R_{out} bagi litar Rajah 3 (b). Nilai parameter diberikan adalah:
$V_o = V_{DD} = 12$ V, $R_3 = 330$ kΩ, $R_4 = 680$ kΩ, $R_S = 3$ kΩ, $K_n = 500\ \mu A/V^2$, $V_{TN} = 0.7$ V and $\lambda = 0.01\ V^{-1}$.

(40 marks/*markah*)

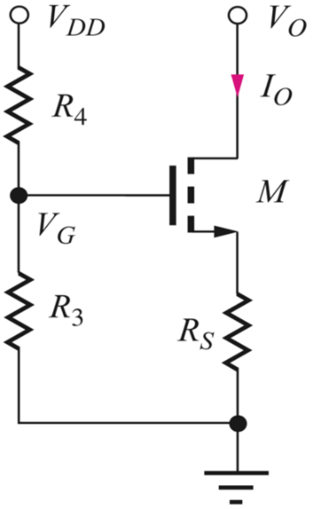

Figure 3 (b)

Rajah 3 (b)

(c) Derive G_m based on the Figure 3 (c).

Berdasarkan Rajah 3 (c), terbitkan G_m.

(40 marks/*markah*)

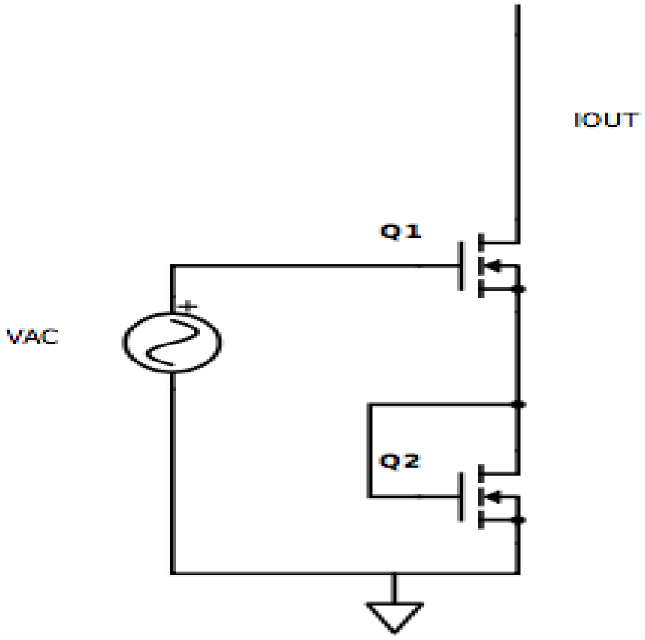

Figure 3(c)

Rajah 3(c)

4. For the circuit in Figure 4:

Bagi litar dalam Rajah 4:

(a) Derive Miller C_C for dominant pole expression.

Hasilkan persamaan Miller C_C bagi kutub dominan.

(50 marks/*markah*)

(b) Derive the expression of gain bandwidth.

Hasilkan persamaan gandaan jalur lebar.

(50 marks/*markah*)

Figure 4

Rajah 4

...8/

5. Figure 5 shows the folded cascode. If I_{REF} is 200 mA, lamda = 0.1:

Rajah 5 menunjukkan litar kaskod terlipat. Jika I_{REF} adalah 200 mA, lamda = 0.1:

(a) Find the DC gain

Dapatkan gandaan DC

(80 marks/*markah*)

(b) If CL at the out node is 1 pF, how much is the dominant frequency?

Jika CL di nod keluaran adalah 1 pF, berapakah frekuensi dominan?

(20 marks/*markah*)

Figure 5

Rajah 5

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APPENDIX A

LAMPIRAN A

Course Outcomes (CO) – Programme Outcomes (PO) Mapping

Pemetaan Hasil Pembelajaran Kursus – Hasil Program

Questions ***Soalan***	**CO**	**PO**
1	4	2
2	3	2
3	3	2
4	3	2
5	3	2