STUDY OF THE RELATIONSHIP BETWEEN DELTA DELAY AND ADJACENT PARALLEL WIRE LENGTH IN 45 NANOMETER PROCESS TECHNOLOGY

by

SHAMSUL ANUAR BIN MOHAMED

Thesis submitted in fulfillment of the requirements

for the degree of

Master of Science

JANUARY 2014

ACKNOWLEDGEMENT

In the name of god, most beneficent, most merciful, All the praised and thank to Allah most almighty, lord of the universe and peace be upon to His messenger Muhammad SAW, the last of the prophets.

I wish to take the opportunity to say thank for the commitment of all people that involve accomplishing this project. My sincerest appreciation must be extended to Dr Asrulnizam bin Abd Manaf, the supervisor for this research for his commitment and comment. He also explains clearly on the arrangement of the research. Besides, he also gives guidelines, idea and feedback for all steps from start until the end of the project. In addition he also advised me on the characteristic that should be included in my research and about the evaluation scheme for me to prepare and meet the requirements.

I also would like to express my sincere thanks to my mentor at Intel Microelectronic, Mr Teh, Chih Chiang who has provided guidance and helped me throughout the research. My thanks also go to Mdm Jennly Lee, Guat Peng and Miss Hanum Syahida for helping through the discussions and suggestions.

My sincere appreciations to my family for giving me the encouragement and morale support. All to all those who had been supported me in one-way or other during my research. They helped me out far more than they ever realized, their supports are very much appreciated.

TABLE OF CONTENTS

		Page
ACKNOWLEDGEMENT		ii
TABLE OF CONTENTS		iii
LIST OF TABLES		vii
LIST OF FIGURES		viii
LIST OF ABBREVIATION		xi
LIST OF PUBLICATION		xiii
ABSTRAK		xiv
ABSTRACT		xvi
CHAPTER 1 - INTRODUCTION		
1.0	Introduction	1
1.1	Problem Statements	3
1.2	The Research Objectives	4
1.3	Project Contributions	5
1.4	Scope of Project	5
1.5	Structure of Thesis	6
CHAPTER 2 - LITERATURE REVIEW		
2.0	Introduction	8
2.1	Basic Concept of Signal Integrity and Crosstalk Noise	8
	2.1.1 Functional Noise	9

2.1.2 Delay Noise 10
2.2 Hierarchical Design Flow 11
2.2.1 Interface Logic Model 12
2.3 Signal Integrity Management in a Design Flow 14
2.3.1 Early Noise Prevention 17
2.3.2 Timing Window Shifting 23
2.3.3 Repair Methodology Engineering Change Order (ECO) 24
2.4 Noise Modeling and Analysis Tool 25
2.4.1 Composite Current Source (CCS) 26
2.4.2 PrimeTime SI Crosstalk Noise Analysis Tool 27
2.5 Summary 28

CHAPTER 3 - METHODOLOGY AND IMPLEMENTATION

3.0 Introduction 30
3.1 Methodology to Obtain Delta Delay and Adjacent Wire Length Relationship 30
3.1.1 Noise Preventions Invested 33
3.1.2 Functional Noise and Delay Noise 34
3.2 Preventive Measurement For Adjacent Parallel Wire Length 36
3.3 Physical Design Flow for Hierarchical Design 39
3.3.1 Logic Synthesis for Hierarchical Design 41
3.3.2 Obtaining Timing Budget 43
3.3.3 Place and Route for Hierarchical Design 45
3.4 Post-route RC Extraction 54
3.5 Crosstalk Noise Analysis 55

3.5.1 PrimeTime SI 56

3.6 Summary 60

CHAPTER 4 - RESULTS AND DISCUSSIONS

4.0 Introduction 62

4.1 Logic Synthesis 62

4.2 Physical Implementation 66

4.2.1 Inter-Block Physical Implementation 67

4.2.2 Top Module Physical Implementation 71

4.3 Timing and Signal Integrity Analysis 73

4.3.1 Inter Block Analysis 73

4.3.2 Top Module Analysis 78

4.4 Delta Delay And Adjacent Parallel Wire Relationship 82

4.4.1 Hot Spot Diagnosis 84

4.4.2 Relationship Between Delta Delay, Coupling Capacitance and Adjacent Parallel Wire 86

4.5 Preventive Measurement 89

4.5.1 Adjacent Parallel Wire Length Limit 89

4.5.2 Prevention Reliability 90

4.6 Summary 93

CHAPTER 5 - CONCLUSIONS AND FUTURE WORKS

5.0 Conclusions 94

5.1 Future Works 95

REFERENCES 96

APPENDIX A: Physical Design Flow Scripts 101

APPENDIX B: Noise and Delay Report 113

APPENDIX C: Diagnosis Result 117

APPENDIX D: Coupling Capacitance, Delta Delay and Adjacent Length Correlation 118

APPENDIX E: Delay Noise After Noise Prevention Insertion 124

LIST OF TABLES

Page

Table 4.1:	Timing report for IP block	74
Table 4.2:	Timing report for top-level	79
Table 4.3:	Details of the delta delay	83

LIST OF FIGURES

		Page
Figure 2.1:	Functional noise (Synopsys Inc, 2010)	9
Figure 2.2:	Delay noise (Synopsys Inc, 2010)	10
Figure 2.3:	Hierarchical partition blocks	11
Figure 2.4:	A block and it's interface logic model	13
Figure 2.5:	SI management methodology for SoC designs - Block level, platform level, and chip level flow (Becer M., Vaidyanathan R., Oh C. and Panda R., 2003)	16
Figure 2.6:	Block shielding (Rajagopal KA et al, 2006)	20
Figure 2.7:	(a) Victim net placed on a single track (b) Victim net broken into parts	21
Figure 2.8:	LW pushing (Jung S., Zang N., Park E. and Kim J., 2008)	24
Figure 2.9:	FW pulling (Jung S., Zang N., Park E. and Kim J., 2008)	24
Figure 3.1:	Methodology to obtain Delay Noise and Length Relationship	32
Figure 3.2:	Correlation between functional noise and delay noise (Becer M., Vaidyanathan R., Oh C. and Panda R., 2003)	36
Figure 3.3:	Adjacent wires travel in parallel	38
Figure 3.4:	General Physical design flow	40
Figure 3.5:	Synthesis flow	41
Figure 3.6:	Place and route flow	46

Figure 3.7:	Power and ground ring (Synopsys, 2010)	47
Figure 3.8:	Power and ground straps (Synopsys, 2010)	47
Figure 3.9:	Top-level and inter-block integration	52
Figure 3.10:	Basic crosstalk analysis flow	57
Figure 3.11:	Crosstalk analysis flow for top-level design	59
Figure 4.1:	Schematic view of the inter-block	63
Figure 4.2:	Budgeted constraint for IP block	64
Figure 4.3:	Physical design cycle for IP block	66
Figure 4.4:	IP block power ring and straps	68
Figure 4.5:	IP block detail routing	69
Figure 4.6:	Top-level details routing	72
Figure 4.7:	SPEF summary report	75
Figure 4.8:	IP block delta delay histogram	76
Figure 4.9:	Accumulated bump voltage	77
Figure 4.10:	Before back-annotate with IP SPEF	80
Figure 4.11:	After back-annotate with IP SPEF	80
Figure 4.12:	Top-level delta delay histogram	81
Figure 4.13:	Delay calculation	85
Figure 4.14:	Delay noise analysis	86

Figure 4.15:	Coupling capacitance, delta delay and adjacent length correlation	87
Figure 4.16:	Coupling capacitance vs Delta delay	88
Figure 4.17:	Delay Noise before noise prevention insertion	91
Figure 4.18:	Delay Noise After noise Prevention Insertion	92

LIST OF ABBREVIATION

CCS	Composite Current Source
CCSN	Common Channel Signaling Network
CTS	clock tree synthesis
DEF	Design Exchange Format
DRC	Design Rule Constraints
ECO	Engineering Change Order
EDA	Electronic Design Automation
GUI	Graphical User Interface
HDL	Hardware Description Language
IC	Integrated Circuit
ILM	Interface Logic Model
IP	Intellectual Property
MHz	Megahertz
MIPS	Microprocessor without Interlocked Pipeline Stages
MW	Milkyway
nm	Nanometer
ns	Nanosecond
pF	Picofarad
ps	Picosecond
RC	Resistive-Capacitive

RTL	Register Transfer Level
SDC	Synopsys Design Constraints
SI	Signal Integrity
SoC	System on Chip
SPEF	Standard Parasitic Exchange Format
SPICE	Simulation Program with Integrated Circuit Emphasis
STA	Static Timing Analysis
μm	Micrometer
VLSI	Very Large Scale Integration

LIST OF PUBLICATION

Shamsul Anuar, M., Asrulnizam, A. M., Chih Chiang, T., (2011) "A Noise and Signal Integrity Verification Flow for Hierarchical Design". 2011 International Conference on Computer Applications and Industrial Electronics (ICCAIE 2011), 4-7 December 2011, Penang, Malaysia. pp. 250-255

KAJIAN TENTANG HUBUNGAN ANTARA DELTA LENGAH DAN PANJANG WAYAR SELARI BERSEBELAHAN DALAM PROSES TEKNOLOGI 45 NANOMETER

ABSTRAK

Reka bentuk hierarki adalah merangkumi rangka kerja lengkap bermula dari *Register Transfer Level* (RTL), sintesis, penempatan dan aliran, penutupan masa dan pelbagai analisis lain sebelum tanda-tamat dipenuhi. Walau bagaimanapun, keadaan geometri yang semakin kecil dan peningkatkan ketumpatan sambungan wayar telah menyebabkan integriti isyarat menjadi isu utama bagi reka bentuk berteknologi mikrometer. Pepijat yang disebabkan oleh gangguan dan integriti isyarat yang dikesan pasca pemprosesan silikon boleh dielakkan dan diperbaiki pada peringkat awal kitar mereka bentuk litar bersepadu. Tujuan kajian ini adalah untuk mewujudkan satu ukuran pencegahan untuk wayar bersebelahan yang boleh bergerak secara selari bagi teknologi 45 nanometer (nm). Ini adalah untuk memastikan bahawa reka bentuk yang kompleks boleh dihantar ke pasaran dengan analisis yang tepat, cepat, dipercayai dan menyediakan penyelesaian untuk tanda-tamat. Pendekatan yang dijalankan adalah dengan melakukan kajian tentang hubungan antara delta lengah dan wayar selari bersebelahan dalam proses teknologi 45 nm dan menyediakan satu ukuran pencegahan untuk menghadkan jarak wayar bersebelahan boleh dibariskan secara selari. Rekaan ini diteroka secara menyeluruh untuk mengkaji hubungan di antara lengah hingar dan wayar bersebelahan yang dibariskan secara selari. Korelasi ini diterjemahkan kepada satu persamaan untuk menganggar lengah hingar yang terhasil dengan ukuruan tertentu

dari wayar selari yang bersebelahan. Kajian kes dibentangkan untuk menunjukkan kaedah yang dicadangkan dapat mengelakkan penumbuhan gandingan kapasitor yang besar pada wayar bersebelahan dan kelewatan isyarat terhasil berpunca dari pemangsa dominan dalam reka bentuk hierarki dengan menghadkan jarak wayar bersebelahan boleh dibariskan secara selari tidak lebih dari 30 mikrometer (um). Lengah hingar setiap pemangsa dikurangkan ke maksima 20ps dengan had yang ditetapkan. Kebolehpercayaan persamaan ini diuji dan penambahbaikan lengah hingar sehingga 32.63 % dapat dilihat. Pada akhirnya, hingar silang dapat dikurangkan secara ketara dengan menggunakan ukuran pencegahan untuk wayar bersebelahan yang diperolehi dari kajian tentang hubungan delta hingar dan wayar selari yang bersebelahan dalam proses teknologi 45 nm.

STUDY OF THE RELATIONSHIP BETWEEN DELTA DELAY AND ADJACENT PARALLEL WIRE LENGTH IN 45 NANOMETER PROCESS TECHNOLOGY

ABSTRACT

Hierarchical design spans the complete framework of a design flow from Register Transfer Level (RTL), synthesis, place and route, timing closure and various other analyses before sign-off. Finer geometries and increasing interconnect density however have resulted signal integrity becoming the key issue for Deep Sub-Micron design. Post silicon bug due to noise and signal integrity can be prevented and fixed at early stage of the IC design cycle. The purpose of this research is to establish a preventive measurement for adjacent wire that can travel in parallel for 45nm technology. The intention is to ensure that a complex design can be delivered to the market with accurate, fast and trusted analysis and provide sign-off solution. Main approach is to conduct the relationship study between delta delay and adjacent parallel wire in 45 nanometer (nm) process technology and provide a preventive measurement to limit the adjacent wire can travel in parallel. The design is explored thoroughly to study the relationship between delay noise and adjacent parallel wire. The correlation is translated into an equation to estimate the delay noise produced with a certain length of adjacent parallel wire. Case study presented demonstrates the proposed methodology can prevent large coupling capacitance on adjacent wire and noise delay arise due to dominant aggressors in hierarchical design that by limiting adjacent wire can travel in parallel within 30um. Delay noise of each aggressor reduced to 20ps max with the limit

provided. The reliability of this equation tested and seen finite delay noise improvement of 32.63%. Ultimately, the crosstalk noise is significantly reduced by applying the preventive measurement of adjacent parallel wire length derived from the correlation study between the delta delay, coupling capacitance and adjacent parallel wire length in 45nm technology.

CHAPTER 1

INTRODUCTION

1.0 Introduction

Hierarchical analysis has become a key to achieve cycle time goals in designing a complex multimillion gate Integrated Circuit (IC)s. A hierarchical design methodology provides a "divide and conquer" approach for large design. By dividing the design into multiple blocks, designers can work on the blocks from RTL through physical implementation in parallel, which will save overall runtime. Converge the design in such a tight schedule requires a huge effort in meeting those requirements in term of timing and noise closure, signal integrity, and advanced physical design methodology for DFM. These requirements may vary according to the complexities of the design, circuit density and the process technology (Aragones, X. and Rubio, A., 2003). The runtime should be taken into consideration for the continue shortening of the design cycle and rapid growth of the chip manufacturing.

Interface logic model is introduced in the design to solve this runtime issue (Shu-Xin Xu, Li min Dong, Xiao-Hong Peng, 2010). An interface logic modeling (ILM) is a circuit representing the interface logic of a block. This model gives accurate timing information of a block. Using ILMs in place of the one or more blocks of a

design enhances capacity and reduce runtime for top-level optimization. Improper circuit planning however will cause runtime delay in fixing those violations that can be avoided in the first place.

Interconnect has become more dominant factor as the manufacturing process technology scaled down (Becer, M., Vaidyanathan, R., Oh, C. and Panda, R., 2003). Finer geometries and increasing interconnect density have resulted crosstalk noise and delay have become a critical issue in hierarchical analysis (Rajagopal, K.A., et al., 2006). The geometries of the wire throughout the process scale down were not as significant as the transistor sizing. Furthermore, the wire size was decreased and the space between the wires also reduced. Coupling capacitance that exists between wires will induces crosstalk, and this crosstalk can cause functional and temporal problem. In spite of having a better performance of extraction tools, it takes considerable amount of computer resources to evaluate properly the quality of the signal in the design (Zhou, S., Zhu, Y., Hu, Y., Graham, R., Hutton, M. and Cheng, C-K., 2006), which is incompatible with "industrial cost" of chip design. A proper management of signal integrity is desirable so that a quick noise convergence can be achieved while meeting the timing, area, power and other constraints. This study will focus on the relationship of delta delay and adjacent parallel wire length in 45 nm process technology and provide early stage prevention through routing guide that can enhance the noise convergence.

1.1 Problem Statements

As the development of VLSI technology steps into deep-submicron level, it becomes more complicated for physical design. A ‘divide and conquer” approach for large design was introduce through hierarchical design (Shu-Xin Xu, Li Min Dong, Xiao-Hong Peng, 2010). Hierarchical design approach spans the complete framework from Register Transfer Level (RTL), synthesis, place and route, timing closure and various other analyses before signing off. Post detail route analysis such as signal integrity (SI) has become bottle neck for large flat design. Through the years, numerous techniques and ideas for crosstalk noise prevention have been proposed to mitigate crosstalk noise. The proposed solutions however, failed to eliminate crosstalk noise completely. The design usually needs several rounds of manual fixes before signing off. Among the solutions proposed is Noise prevention through incremental placement (Ren H. X., Pan David Z., Villarrubia Paul G., 2004), Gate sizing based on estimated noise (Bhattacharya K. and Ranganathan N., 2009) and Crosstalk noise modeling using lumped model (Lu C., Chen H., and Malgorzata Marek-Sadowska, 2010). Their analyses depend on the accuracy of their noise model. Noise prevention through noise modeling was not as accurate as real RC data. A finer solution was proposed where the coupled line delay was taken into consideration during routing (Samanta T., Khatun S., Rahaman H., 2011). This noise aware routing guide however was inserted during global routing not details routing. Thus, initiating a crosstalk noise aware detail routing in hierarchical design makes logical sense.

The Interface Logic Modeling (ILM) is introduced to the hierarchical design to enhance capacity and reduces runtime for top-level optimization. The current research aims to integrate a coupled line delay aware routing guide during detail routing stage for each lower hierarchy block. The principle aim is to eliminate unintentional switching, slowdown or speedup when the block is analyzed in the context of top-level. The crosstalk induced causes glitches or delay noise which may propagate to a node or a latch, giving functional failures or potential setup and hold time failures. The idea behind the routing guide is to add in all possible crosstalk noise preventions and before detail routing and generate a coupled line delay and wire length relationship post detail routing stage.

1.2 The Research Objectives

The analysis on the signal integrity is done at the post detail routing stage and some of the violations seen in the report is not same as the initial prediction. This is due to the inaccuracy of the extraction data from the physical hierarchy. Therefore, the main objectives of this research are:

i- To establish a preventive measurement for adjacent wire that can travel in parallel for 45nm technology.

ii- To enhance preventive steps in reducing the signal integrity violations at the initial stage.

1.3 Project Contributions

This work provides the relationship study of delta delay and the adjacent parallel wire length in 45nm process technology. A preventive measurement to allow adjacent wire to travel in parallel is obtained from this relationship study. This preventive measurement is useful to eliminate undesired crosstalk in physical design flow as early noise prevention, thus the handshaking between the top-level and lower hierarchy is reduced. This prevention measurement could be useful for designers to achieve signal integrity sign-off quality faster and yet achieves acceptable accuracy.

1.4 Scope of Project

The idea of this research is to materialize signal integrity management and improve the methodology to overcome the crosstalk noise in a noisy design. The scope of this study is adopts from the following four techniques:

i- Pessimistic block closure approach.

ii- Block isolation using power and ground shielding.

iii- Shielding such as bus net that are likely to experience noise problems from long parallel neighboring nets.

iv- Slew optimization with driver sizing (net with weakly driven makes it susceptible to noise).

v- Relation study of delta delay, coupling capacitance and adjacent wire to limit the distance parallel wire can travel.

1.5 Structure of Thesis

This thesis is organized into five chapters as follows. This thesis report starts with the introduction or outline of this research. It gives background information about the subject area and consists of problem statement, research objectives, and the scope of this research. Chapter 2 is all about the discussion of the previous work on the subject. Multiple noise prevention and fixes were review in order to invest in the research.

Chapter 3 consists of the methodology of this research. The approaches to obtain the result were illustrated clearly starting from RTL until post detail route analysis.

Chapter 4 presents the overall results, starting with the early noise prevention methodology that can be invested in the early stage of the design cycle, and followed by the results illustrate the robust repair methodology to address noise problem in the design.

Chapter 5 outlines the conclusions and recommendations of the future works. This chapter concludes the overall research findings especially on the noise preventions

and repair methodology and point out recommendations that can be implemented in the future.

CHAPTER 2

LITERATURE REVIEW

2.0 Introduction

A proper and a complete methodology are very important to analyze, avoid, and resolve the issues in a tight project schedule. In this chapter, the basic concept of signal integrity and hierarchical design is clearly explained. The existing crosstalk avoidance technique in hierarchical design is explored and described.

2.1 Basic Concept of Signal Integrity and Crosstalk Noise

Signal integrity in IC design expresses the ability of an electrical signal of a net to carry information and resist the effect of high-frequency electromagnetic interference from nearby signals. Crosstalk noise is an undesirable electrical interaction between two or more physically adjacent nets due to capacitive cross-coupling. Two terms are used when analyzing a net for crosstalk noise which is an aggressor and a victim. A victim is a net that receives undesirable cross-coupling effect from adjacent ones. The nets that are cross-coupled to a victim are called aggressors. Crosstalk can manifest itself in two ways; functional noise and delay noise.

There are few electrical parameters that determine the magnitude of the crosstalk effects:

i- Coupling capacitance between interconnects – longer adjacent nets that travel in parallel contribute to higher coupling capacitance.

ii- Driver strength of the victim and aggressor net – weaker drive strength on the victim net causes the net to be more susceptible to noise.

iii- The switching directions either rising or falling.

iv- The combination of effects from multiple aggressor nets on a single victim net.

2.1.1 Functional Noise

A functional noise occurs when a noise is injected to a quiet victim net which causes a glitch as shown in Figure 2.1.

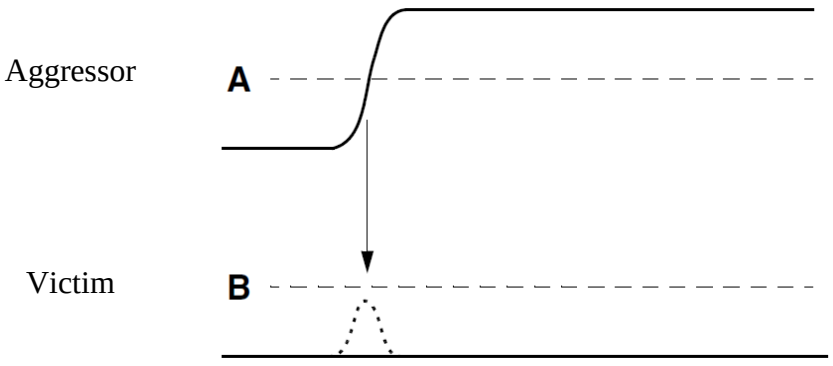

Figure 2.1: Functional noise (Synopsys Inc, 2010)

If the glitch propagates through the circuit and finally gets latched on to a register element (flip-flop or latch), the circuit alters, and a functional failure happens. If the transition on A occurs at an early time, it induces an upward bump or a glitch on net B before the transition on B, which has no effect on the timing of signal B. A sufficiently large bump can cause a change in the logic value of a net, which can propagate down the timing path.

2.1.2 Delay Noise

A delay noise occurs when the victim nets and aggressor nets are switching simultaneously, causes the transition delay of the victim net to be altered. Figure 2.2 illustrates the delay noise between the victim and aggressor net.

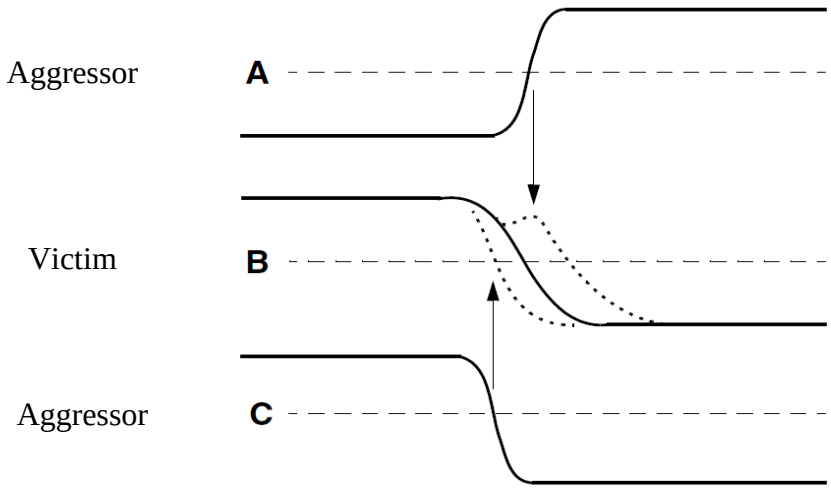

Figure 2.2: Delay noise (Synopsys Inc, 2010)

Depending on the direction of the transitions, the delays added will cause the potential setup or hold time failures. If the transition on A occurs at about the same time as the transition on B, it could cause the transition on B to occur later as shown in the, possibly contributing to a setup violation; or it could cause the transition to occur earlier, possibly contributing to a hold violation.

2.2 Hierarchical Design Flow

Design sizes, Electronic Design Automation (EDA) tool capacity, and runtime are the main reasons the hierarchical design flow was introduced in the design cycle (You Y., Peng H. and Yang Y., 2005). Hierarchical design flow allows each of an individual block being implemented separately and concurrently as shown in Figure 2.3.

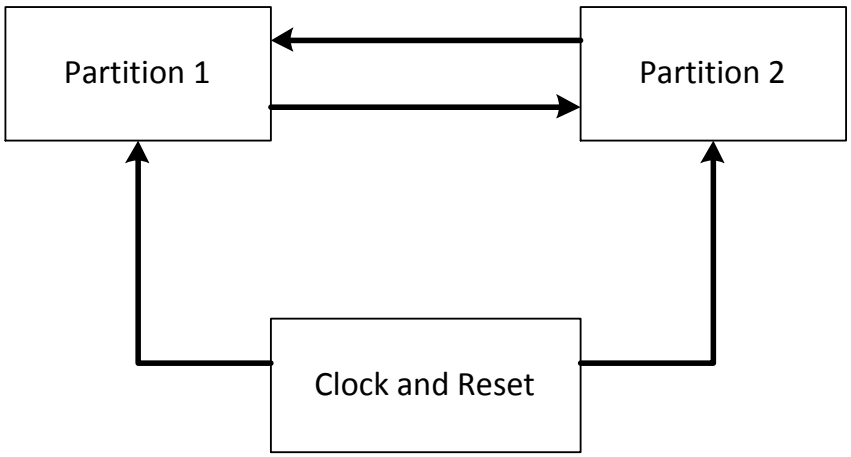

Figure 2.3: Hierarchical partition blocks

Hierarchical design flow can be implemented through two approaches: top-down approach and bottom-up approach. In top-down approach, a design is partitioned and a *.def* file is export during global placement. *Def* file has the physical information such as the position of the input and output pins, and the area of the partitioned blocks. All the partitioned blocks will go through the placement, Clock Tree Synthesis (CTS) and detail routing base on the constraint given by *.def* file.

In contrast, bottom-up approach start with a lower hierarchy design and propagate up to the top-level. The integration of the bottom-up approach will be using Interface Logic Model (ILM) flow. An ILM is a structural model of a circuit that is modeled as a smaller circuit representing the interface logic of the block. ILMs usage in place of the one or more blocks of a design, it enhances capacity and reduces runtime for top-level optimization. Using the hierarchical design including ILM, the runtime of the place optimization stage, clock optimization stage and route optimization stage is reduced to 28.8%, 27.7% and 43% relatively, meanwhile the boundary timing become more optimal which can also prove the timing accuracy of ILM (Shu-Xin Xu, Li min Dong, Xiao-Hong Peng, 2010). In this research, bottom-up approach is implemented to imitate industrial methodology.

2.2.1 Interface Logic Model

Signal integrity, timing and noise closure have become more challenging as the development of VLSI technology steps into deep-submicron level. A methodology

which can improve the runtime and productivity was introduced in physical design flow (Shu-Xin Xu, Li Min Dong, Xiao-Hong Peng, 2010). Interface Logic Model is implemented in the whole physical design flow to solve this problem. ILMs are used in the EDA tool to reduce the number of design objects and memory requirements when the tool performs top-level optimization on large designs.

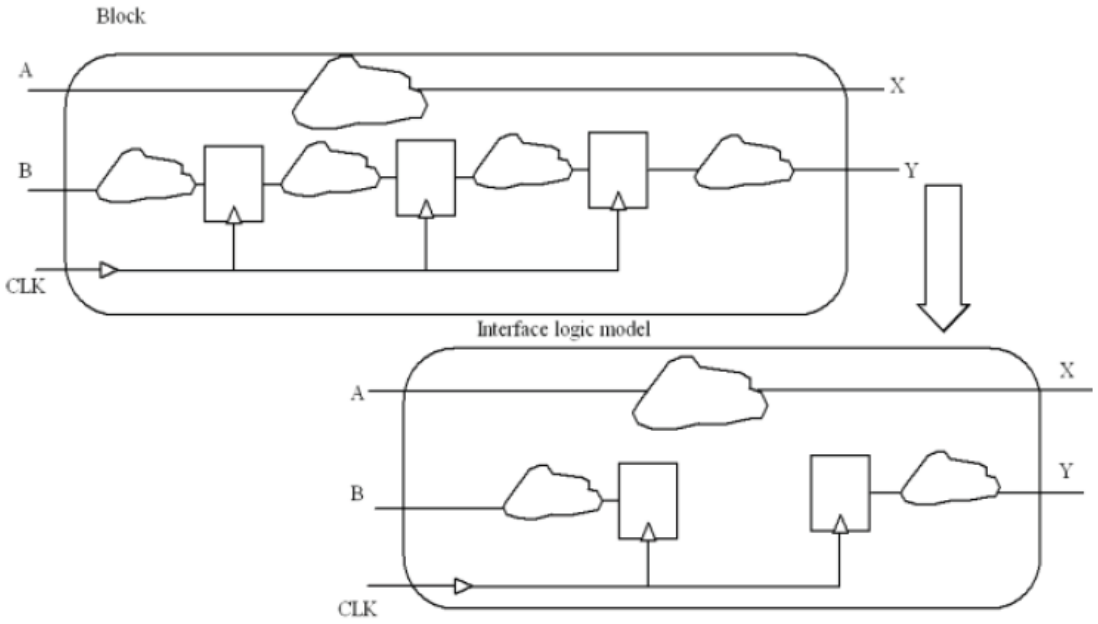

Figure 2.4: A block and it's interface logic model

Figure 2.4 shows a simple case of a block and its interface logic model. In an interface logic model, the gate-level netlist for a block is modeled by another gate-level netlist that contains only the interface logic of a block and possibly logic that associate with the interface logic, while all other logic is removed. ILMs preserve interface logic without modifying it. The model does not abstract the design but instead discards only what is not required for modeling boundary timing. Any sub-blocks in the hierarchy that

affects the boundary timing is retained. Compare with other abstracted type model such as ETM, the timing information is more accurate and the generating time is much shorter (Shu-Xin Xu, Li min Dong, Xiao-Hong Peng, 2010). Therefore, ILMs provide highly accurate timing representations. ILMs can be used in a hierarchical signal integrity flow. In this flow, the ILMs are shielded at the top-level to prevent crosstalk between the ILM nets and top-level nets.

2.3 Signal Integrity Management in a Design Flow

A design is considered to have signal integrity check clean only when there is no coupling noise large enough to cause a functional or timing error. Pessimistic block closure approach and block shielding helps to converge hierarchical sign-off more quickly, however it will not eliminate crosstalk delay and noise entirely. A proper SI management in physical design flow thus is needed to have more stable design in term of timing and noise.

When there are severe constraints on the design cycle time or design resources, a design team may have spent huge effort going through iterative exercise to analyze and fix every noise problem that is uncovered. Therefore, the steps in the SI management methodology are carefully chosen to realize quick design convergence wherein a noise-free design is obtained while meeting the timing, area, power and other constraints (Becer M., Vaidyanathan R., Oh C. and Panda R., 2003).

The underlying causes for both problems are the same; weak victim drivers, strong aggressors, large coupling, light loading and etc (Becer M., Vaidyanathan R., Oh C. and Panda R., 2003). There is a very high degree of correlation between occurrences of these two problems for the same net. Likewise, there is a strong correlation between the magnitude of functional noise glitch and the change in delay due to noise for a net. These correlations suggest that fixing one problem should often alleviate the other problem as well, if not completely eliminate.

The observation from previous research suggests an effective SI management strategy wherein the delay noise problems are addressed only after all the functional noise problems are addressed (Becer M., Vaidyanathan R., Oh C. and Panda R., 2003). Since nets are shared by many paths, a large number of delay violations will be reported out and it will not be easy to manage such a large number of violations. It is more convenient to address the problem initially for the shorter list of violators in the functional noise category. The number of the delay noise violations will drastically decreased after the functional failures are corrected.

A methodology was proposed wherein functional failures are analyzed and repaired first at pre-route and post-route stages, and the delay noise analysis and repair are done only in the post-routing stage after all the functional noise violations have been repaired. Figure 2.5 shows SI management methodology for System-On-Chip (SoC) designs.

As is clear from the flow diagram in Figure 2.5, noise analysis and repair is done in 3 phases. Section 3: an early prevention phase, section 4: a post route functional repair phase, and section 5: post route noise aware timing analysis and repair phases.

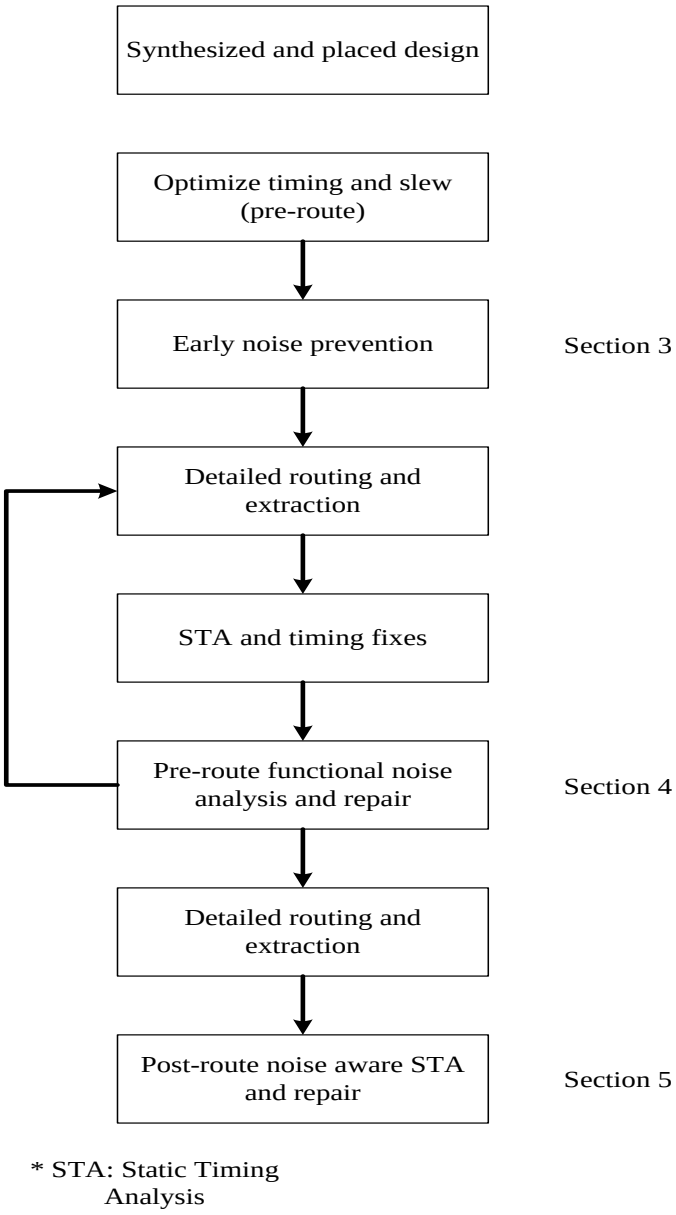

Figure 2.5: SI management methodology for SoC designs - Block level, platform level, and chip level flow (Becer M., Vaidyanathan R., Oh C. and Panda R., 2003)

2.3.1 Early Noise Prevention

As the design complexities increases, it is becoming more risky to address noise violations with repairs alone. Early noise prevention is desire to be invested in early stage of the design as illustrated in Figure 2.5 to prevent potential noise problem in the design. There is numerous number of design techniques can be applied for this purpose. These techniques can be applied to all nets or selected noise prone nets.

Noise prevention methodology adopts the following four techniques (Becer M., Vaidyanathan R., Oh C. and Panda R., 2003); the first three are being related to physical design and the last technique is related to pre-route circuit optimization:

i- Limiting the distance neighboring nets can travel in parallel:

- This prevents long parallel runs which create large coupling to dominant aggressors.

ii- Shielding:

- This technique is applied for structured routing topology, such as bus nets that are likely to experience noise problems from long parallel neighboring nets.

iii- Routing with extra spacing:

- This technique is also applied for structured routing topology, such as bus nets.

iv- Pre-route optimization:

- Slow slew rate at the receiving ends of a net indicates that the net is weakly driven or highly resistive, which makes the net susceptible to noise. With driver sizing or buffer insertion, slew rate at the receiver inputs is improved. Although applying slew optimization globally results in stronger aggressor drivers, its benefit on overall noise due to the prevention of unacceptably weak victim drivers is greater.

2.3.1(a) Pessimistic Block Closure

A pessimistic approach was applied on the interface path to bind the block from crosstalk delay impact at the top-level. A pessimistic transition value was set on the input pins. All the nets on the interface paths are considered independently with other nets inside the block to ensure all the coupling interaction between internal and external nets are always considered. Looking back at the pessimistic approach for block closure, if the budgeted timing is reasonable the blocks somewhat is immune to any top-level parameter changes. But, this approach can increase the violations seen in the block due to pessimistic assumptions (Rajagopal KA et al, 2006). Since the budgeting problem is very difficult, obtaining reasonable budgeting results may takes a long time.

2.3.1(b) Budgeting Free Design and Border Moving

Budgeting free design and border moving techniques were proposed in hierarchical design to eliminate budget timing dependency (Nakamura Y. C., Tagata M., Okamoto T, Shigeyoshi, Yoshikawa K, 2006). All the connections between hierarchical blocks are directly connected to flip-flop. In general, the design was constraint by the functional level. By having the flip-flop on the border, the border may be easily moved so that the timing constraints from input/output of the blocks to flip-flop are not necessary. This approach may only suitable for smaller designs that only have 2 level of hierarchy.

2.3.1(c) Block Shielding

The easiest way to implement block shielding was to enforce spacing between top and block route (Kose S., Salman E. and Friedman E.G., 2009),. Although spacing reduce coupling, but it does not entirely eliminate the occurrence of the crosstalk at the edge of the block. Therefore, block shielding comes in handy where the block is shielded for all metal layers. Figure 2.6 shows the illustration of block shielding in a design which using 90 nm technology. If shielding is not possible in all layers, preferred routing layers on each side of the block must be shielded because those layers are more likely to have a top-level net running parallel to the edge of the block. Preferred direction shielding will ensure that there is no coupling between top and block nets routed in preferred direction (Rajagopal KA, 2006).

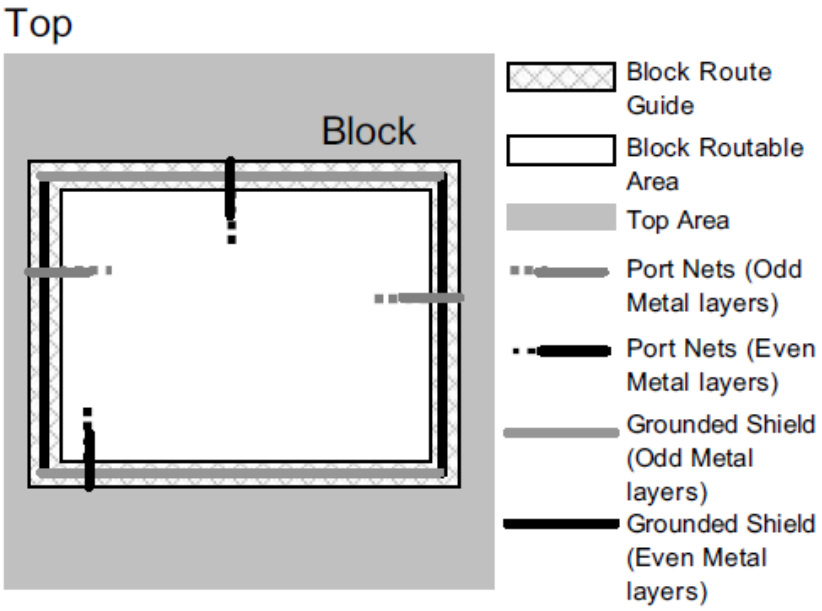

Figure 2.6: Block shielding (Rajagopal KA et al, 2006)

2.3.1(d) Coupled Line Delay Tree Construction

Numerous researches had been looking for an algorithm to optimize crosstalk aware routing tree, however only a small number of work address the problem thoroughly. A coupled line delay model was proposed for on-chip interconnects during global routing (Samanta T., Khatun S., Rahaman H., 2011). Crosstalk aware delay tree constructions proposed was employed by a cut and joins strategy which consider the effect of self-inductance, capacitance and resistance of a metal interconnect, and coupling capacitance and mutual inductance between multiple parallel, closely spaced lines. This proposal is capable of producing crosstalk-aware delay measure in submicron range design.

Decision for choosing new tracks for broken edges of a net are guided by the coupling values and the coupled line delay tree is constructed with optimized coupling parameters to reduced maximum delay at the sink terminal of the aggressor net. An example for assigning different tracks to a larger victim net is illustrated in Figure 2.7.

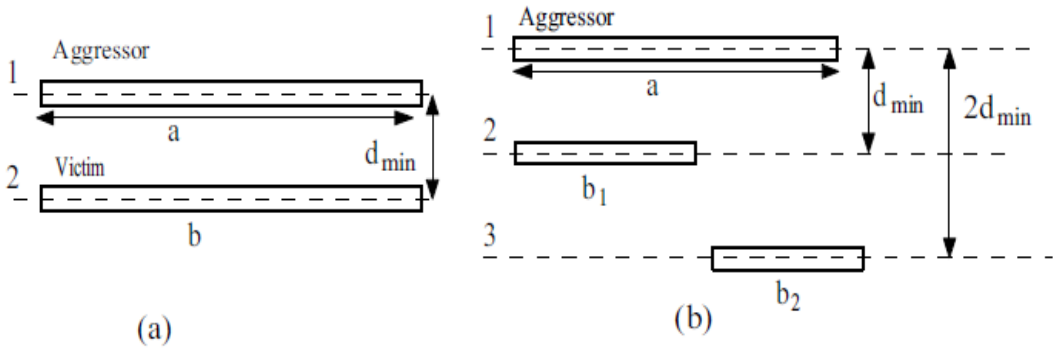

Figure 2.7: (a) Victim net placed on a single track (b) Victim net broken into parts

Aggressor net of length ‘a’ is placed initially in parallel with a victim net of length ‘b’. To reduce crosstalk effect between these two nets. Victim net is broken into parts and assigned to two different traces 2 and 3 (Samanta T., Khatun S., Rahaman H., 2011). This is a favorable noise prevention steps that can be include in the initial stage of the physical design flow. However, this method was constrained by via to via layout design rules. As the net broken into two or more parts, it took more routing layer and vias to ensure the victim net fully routed. Having the same via place closely together will cause the design to violate the design rules. To ensure the design still abide the layout design rule, a scenic routing might be seen just to connect the broken nets, thus create more delay onto the net.

2.3.1(e) Crosstalk Aware Incremental Placement

Another research invests into cell placement as one of the early noise prevention method. Placement determines the overall routing congestion, which correlates with the coupling capacitance, which in turn correlates with the crosstalk noise, placement shall be a good level to do early noise mitigation (Ren H. X., Pan David Z., Villarrubia Paul G., 2004). This research uses the coupling capacitance map to guide placement and use 2-π model (Cong J., Pan D. Z. and Srinivas P. V., 2001) and incorporate it into a concept of crosstalk noise map to guide placement directly. The 2-π model is an analytic model which takes into consideration of many first-order parameters such as the coupling capacitance, driver and wire resistance.

This prevention method needs to go through 2 incremental placements for noise reduction; noise aware cell inflation and local refinement (Ren H. X., Pan David Z., Villarrubia Paul G., 2004). The noise aware cell inflation is implemented to reduce the congestion in the hot spots region. This hotspot was identified earlier using noise map. Most popular congestion reduction is to allocate whitespace in the congested region. The first step will spread cells out from the noise region. Next, cells were moved around during local refinement to ease the congestion on those noise regions. The objective of this step is to optimize those noise regions using original cell size while keeping the placement order for other regions. The effectiveness of this prevention method is strongly dependent on the accuracy of the coupling capacitance estimation.

Thus, having the coupling capacitance estimated from global router is not relatively accurate simply because there are multiple possible local routing solutions.

2.3.2 Timing Window Shifting

Functional noise analysis and repair stage in section 4 based on Figure 2.5 is timing window shifting technique. Another earlier research conducted has proven that a timing window shifting method considering multiple aggressors can reduce delay degradation (Jung S., Zang N., Park E. and Kim J., 2008). Delay degradation are caused by multi-aggressor can be minimized by LW pushing and FW pulling as illustrated in Figure 2.8 and Figure 2.9. This crosstalk avoiding method is to remove the overlapped area between timing window of aggressor and victim or minimize it and then reduce the effect of crosstalk by shifting timing window.

Research result has proved that average 4.75% efficiency progress comparing with existing crosstalk avoidance method (Jung S., Zang N., Park E. and Kim J., 2008). Adjusting timing windows considering multi aggressor can reduce the crosstalk effect, however the functionality of the design might also been altered due to timing window adjustment.

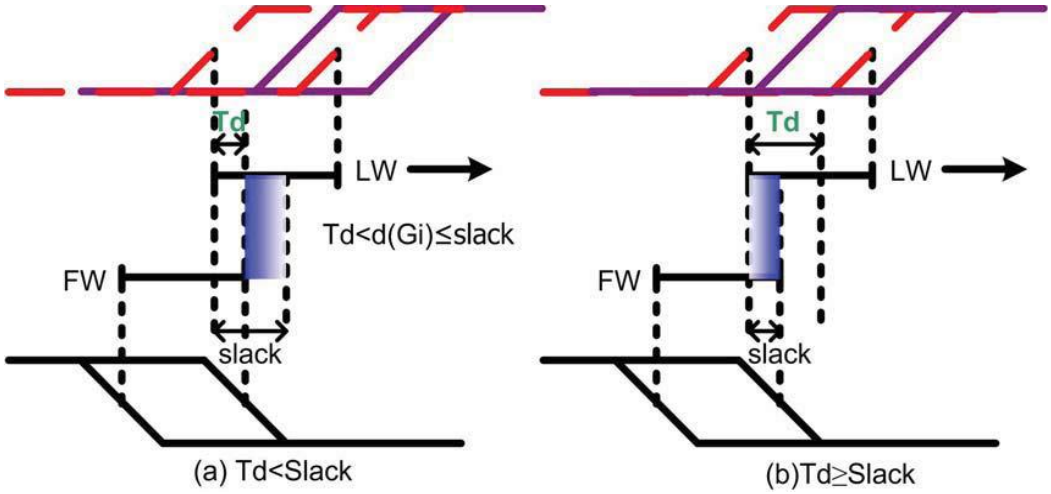

Figure 2.8: LW pushing (Jung S., Zang N., Park E. and Kim J., 2008)

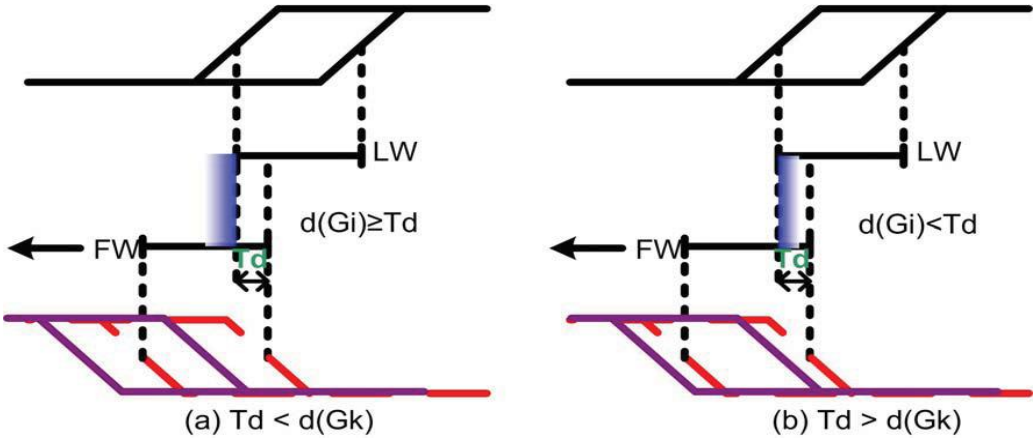

Figure 2.9: FW pulling (Jung S., Zang N., Park E. and Kim J., 2008)

2.3.3 Repair Methodology Engineering Change Order (ECO)

Section 5 in Figure 2.5 is mainly focus on post detail route fixes. After detail routing, the fail nets were gone through a repair methodology ECO including driver sizing, buffering, then double spacing and shielding. These repair methodology does not in any particular order in which of this options to be used. It suggested that routing