First Semester Examination
Academic Session 2018/2019

December 2018/January 2019

EEE505 – Advanced Analog Integrated Circuit Design

Duration : 3 hours

Please check that this examination paper consists of SIX (6) pages of printed material before you begin the examination.

Instructions : Answer **FIVE (5)** questions. Answer TWO (2) questions in Part A and TWO (2) questions from Part B and ONE (1) question from any section.

Use two-book answers for **Part A** and **Part B**.

All questions carry the same marks

Part A :

1. For the circuit shown in Figure 1 below, assume that all transistors are operating in the saturation region. Calculate the following using these parameters:
   $K'_n = \mu_n C_{ox} = 200\ \mu A/V^2$, $V_t = 0.4$ V, $\lambda = 0.1\ V^{-1}$

   a) Output current, I_{out} (5 marks)

   b) Minimum output voltage, $V_{out,min}$ (5 marks)

   c) Output resistance, R_{0ut} 10 marks)

   Note: For part (a) and (b) the λ effect can be neglected. BUT you need to use λ for calculating part (c).

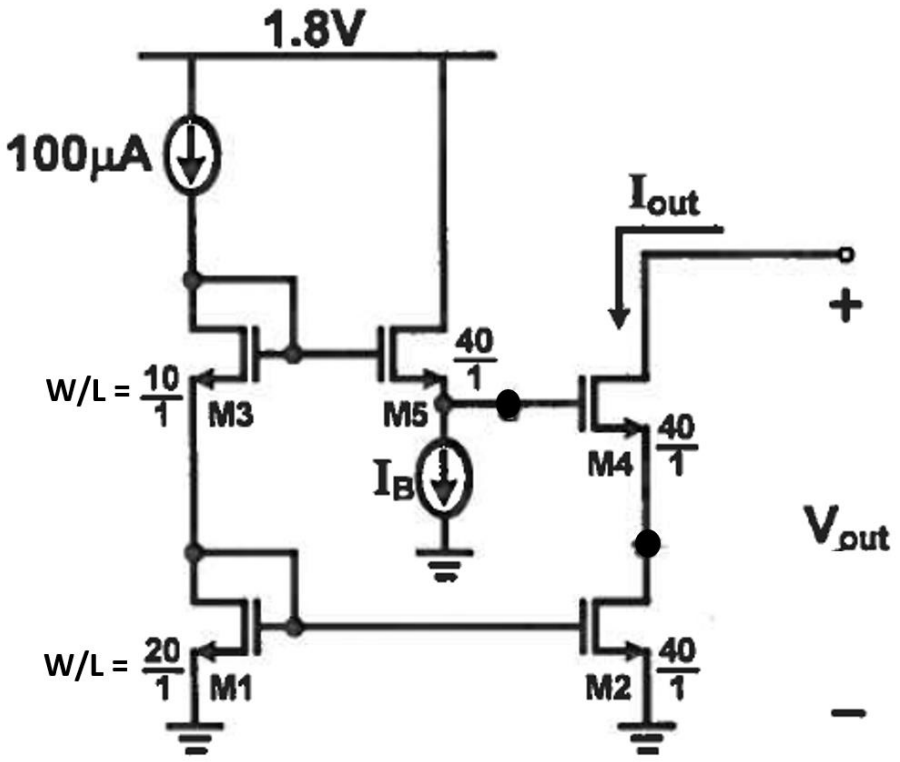

Figure 1.

2. For an active-loaded MOS differential amplifier shown in Figure 2, assume that for all transistors, W/L = 7.2 µm/0.36 µm, $\mu_n C_{ox}$ = 387 µA/V^2, $\mu_p C_{ox}$ = 86 µA/V^2, $|V'_{An}|$ = 5 V/ µm, $|V'_{Ap}|$ = 6 V/ µm, the bias current *I* = 0.2 mA and Rss = 25 kΩ.

   a) Determine the <u>value</u> of differential-mode gain, A_{dm}. (Note: you may need to find the overdrive voltage, g_m and r_0 for each transistor)

   (15 marks)

   b) Given the common-mode gain, A_{cm} = - 1/(2.g_m.Rss), determine the CMRR ($\frac{|A_{dm}|}{|A_{cm}|}$).

   (5 marks)

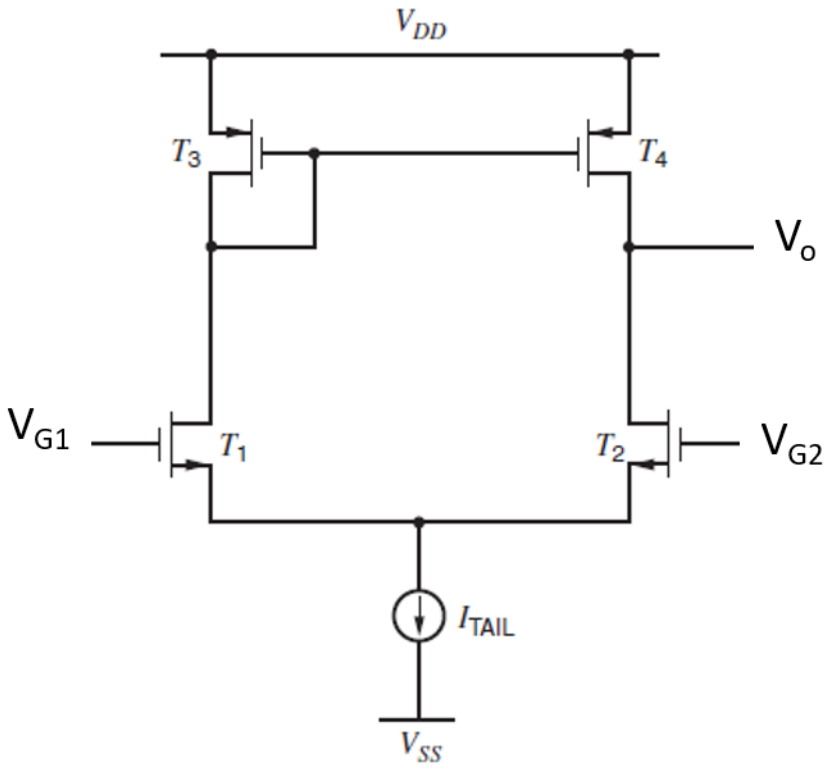

Figure 2.

3. Figure 3 refers to a folded cascode operational transconductance amplifier (OTA) with all transistors operate at the overdrive voltage of 0.2 V.

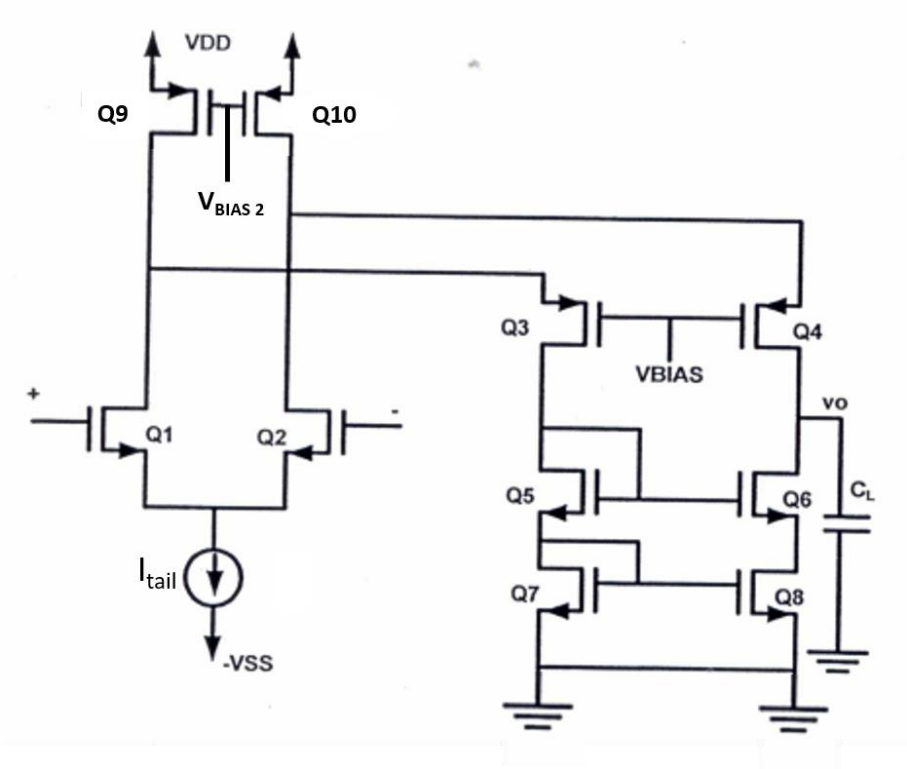

Figure 3.

a) Find the expression for output resistance, R_o (5 marks)

b) Find the expression for A_V. (5 marks)

c) Find the expression for peak-to-peak output voltage swing. (10 marks)

Part B :

4. (a) Figure 4 depicts the switched capacitor resistor circuit. By referring to the figure:

(i) Derive the input equivalent resistance of the circuit in Figure 4.

(7 marks)

(ii) Calculate the equivalent resistance if the clock frequency is 0.5 MHz and *C* is 2 pF.

(3 marks)

(iii) What is the operation of MOSFET whereby the behaviour of V_{GS} is similar as V_{BE} of bandgap device? Together with switched capacitor resistor, design a PTAT current generator. The final equation must be included together with the design.

(10 marks)

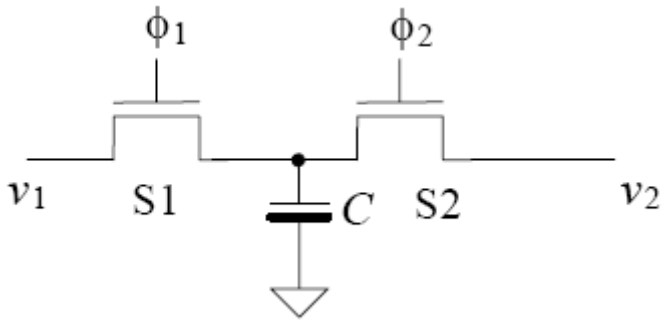

Figure 4

5. (a) Design DAC schematic and derive out the mathematical model equation. The model is based on current steering-resistor string approach. Draw the schematic of the DAC. Explain the functions of all the components in the schematic.

(12 marks)

(b) Extend the model up to 8-bit. Explain your model.

(8 marks)

6. (a) Figure 6 shows the biasing circuitries for a typical current steering DAC.

(i) Explain the function of the operational amplifier.

(2 marks)

(ii) What is the value of resistance R, if **I** is 1 mA and VREF = 1.2 V?

(2 marks)

(iii) Assuming VDD = 3.6 V and M1 is in saturation, W/L = 24/2, Vtp = -1, Kp = 40 μA/V^2 , calculate the required VSG.

(6 marks)

(b) Draw the basic 8-bit DAC which must include the biasing circuitries and the DAC resistor string. (10 pts)

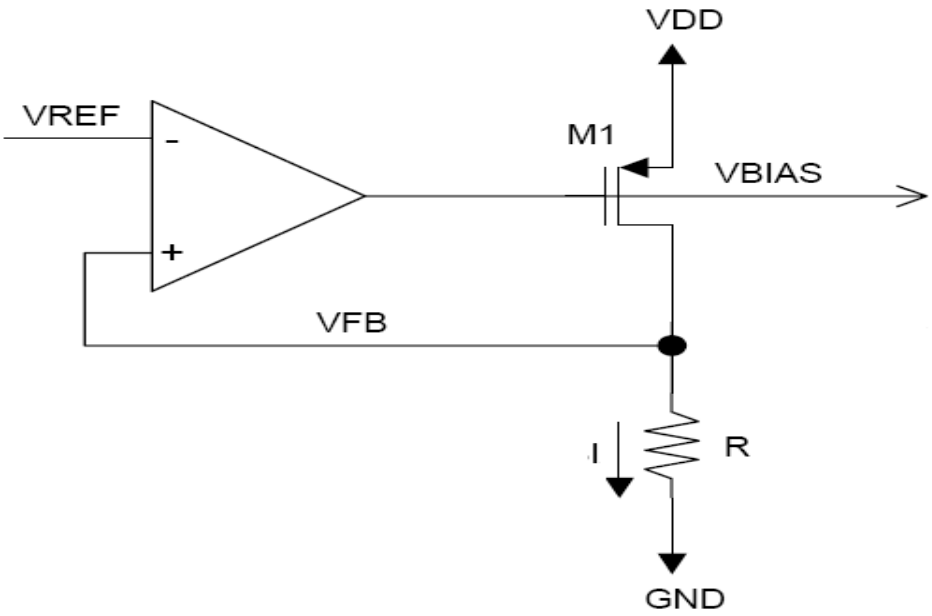

Figure 6

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