First Semester Examination
Academic Session 2018/2019

December 2018/January 2019

EEE445 – DESIGN OF INTEGRATED ANALOG CIRCUITS
(REKABENTUK LITAR ANALOG BERSEPADU)

Duration : 3 hours
(Masa : 3 jam)

Please check that this examination paper consists of TEN (10) pages of printed material before you begin the examination.

[Sila pastikan bahawa kertas peperiksaan ini mengandungi SEPULUH (10) muka surat yang bercetak sebelum anda memulakan peperiksaan ini.]

Instructions: This question paper consists of **FIVE (5)** questions. Answer **ALL** questions. All questions carry the same marks.

[***Arahan:*** *Kertas soalan ini mengandungi **LIMA (5)** soalan. Jawab **SEMUA** soalan. Semua soalan membawa jumlah markah yang sama.]*

In the event of any discrepancies, the English version shall be used.

[Sekiranya terdapat sebarang percanggahan pada soalan peperiksaan, versi Bahasa Inggeris hendaklah digunapakai.]

1. (a) Given Figure 1(a), derive the expression to relate I_{out} with I_{REF}. Neglect the channel-length modulation ($\lambda = 0$) effect for both transistors M_1 and M_2.

Diberi Rajah 1(a), terbitkan persamaan untuk mengaitkan I_{out} dengan I_{REF}. Abaikan kesan pemodulatan panjang saluran ($\lambda = 0$) bagi kedua-dua transistor M_1 dan M_2.

(20 marks/*markah*)

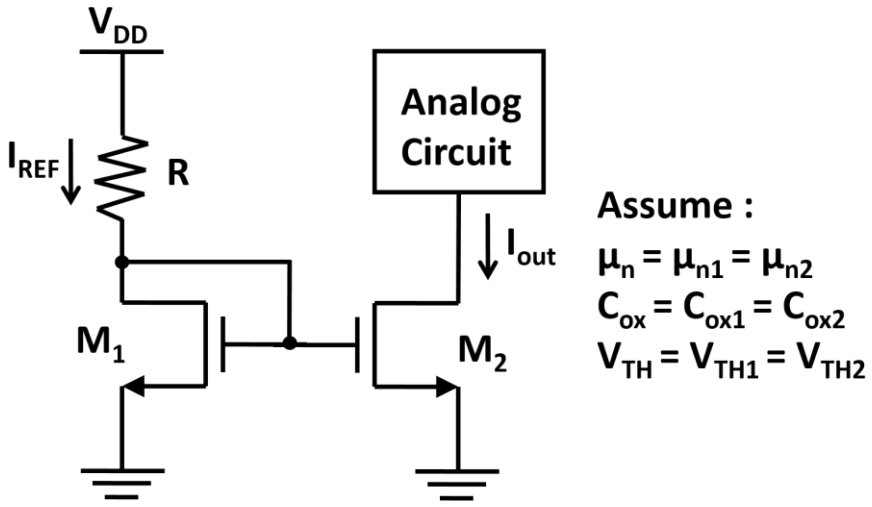

Figure 1(a)

Rajah 1(a)

(b) Referring to Figure 1(a) and the derived expression in question 1 (a), neglect the channel-length modulation ($\lambda = 0$) effect for both transistors M_1 and M_2. Calculate the required parameters in (i), (ii), (iii) and (iv). Given:

Merujuk kepada Rajah 1(a) dan persamaan yang telah diterbitkan di soalan 1 (a), abaikan kesan pemodulatan panjang saluran ($\lambda = 0$) bagi kedua-dua transistor M_1 dan M_2. Kirakan parameter-parameter di (i), (ii), (iii) dan (iv). Diberi:

$I_{REF} = 40\ \mu A,\ \mu_n C_{ox} = 120\ \mu A/V^2,\ V_{TH} = 0.3\ V,\ L_1 = L_2 = 0.2\ \mu m,$
$W_1 = 2\ \mu m,\ V_A' = 20\ V/\mu m$

(i) Transistor M_2 channel width (W_2) so that I_{out} = 20 µA.
Lebar saluran (W_2) transistor M_2 supaya I_{out} = 20 µA.

(10 marks/*markah*)

(ii) Output resistance (r_{02}) of current source.

Rintangan keluaran (r_{02}) *sumber arus.*

(10 marks/*markah*)

(iii) Lowest possible of output voltage (V_{out}) to keep M_2 operating in saturation mode.

Nilai terendah yang mungkin untuk voltan keluaran (V_{out}) untuk memastikan transistor M_2 beroperasi di dalam mod tepu.

(15 marks/*markah*)

(iv) Change of I_{out} (ΔI_{out}) if the change of V_{out} (ΔV_{out}) is + 1 V.

Perubahan I_{out} (ΔI_{out}) jika perubahan V_{out} (ΔV_{out}) ialah + 1 V.

(15 marks/*markah*)

(c) Figure 1(b) shows a complex design of analog circuits with single current mirror. If all of the transistors are operating in saturation mode, determine drain current (I_D) of each transistor i.e. M_2 to M_5 with respect to the reference current (I_{REF}). Neglect the channel-length modulation ($\lambda = 0$) effect for all the transistors.

Rajah 1(b) menunjukkan reka bentuk kompleks litar-litar analog dengan satu cermin arus. Jika kesemua transistor beroperasi di dalam mod tepu,tentukan arus salir (I_D) *untuk setiap transistor* M_2 *sehingga* M_5 *berpandukan arus rujukan (*I_{REF}*). Abaikan kesan pemodulatan panjang saluran (*$\lambda = 0$*) untuk kesemua transistor.*

(30 marks/*markah*)

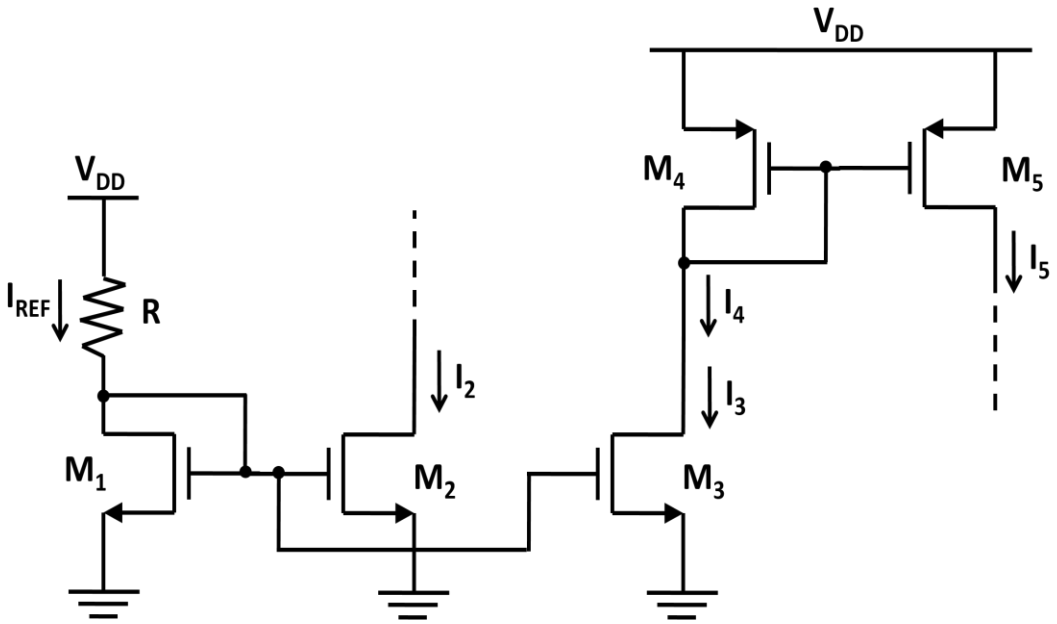

Figure 1(b)

Rajah 1(b)

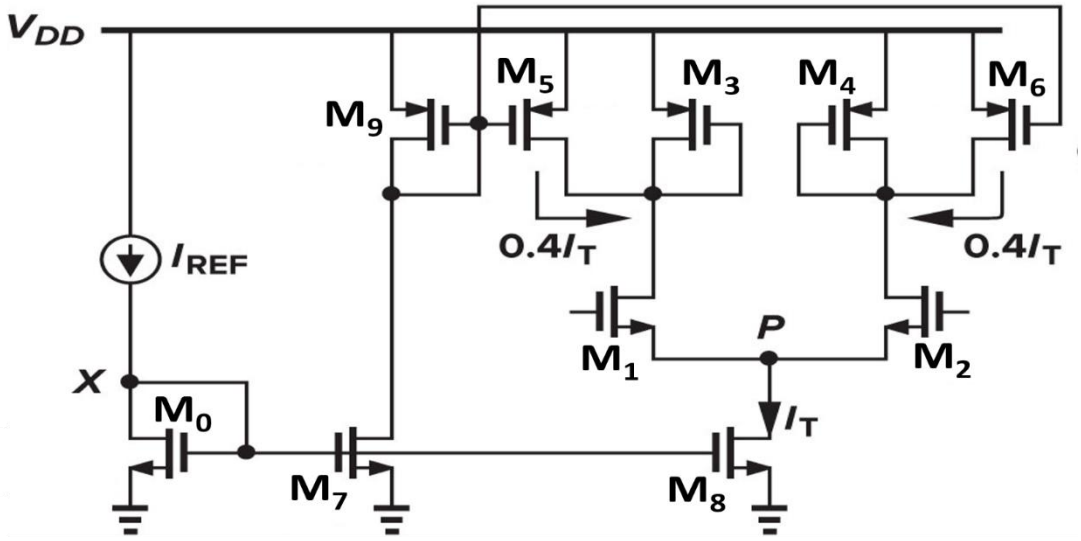

Figure 2

Rajah 2

2. Given a differential amplifier with its corresponding current mirror as in Figure 2. By neglecting the channel-length modulation (λ = 0) effect for all the transistors, analyze the circuits and give your answer to the following questions. Given:

Diberi sebuah penguatkuasa kebezaan dengan cermin arus seperti pada Rajah 2. Dengan mengabaikan kesan pemodulatan panjang saluran (λ = 0) untuk kesemua transistor, analisakan litar-litar tersebut dan jawab soalan-soalan berikut. Diberi :

$$\mu_n = 294\ cm^2/V.s,\ \mu_p = 98\ cm^2/V.s,\ L = 0.13\ \mu m,\ C_{ox} = 13\ fF/um^2,$$
$$V_{eff,M0} = 0.101\ V,\ (W/L)_0 = (2/0.13)\ \mu/\mu$$

(a) What is the drain current I_D required for transistor M_0?
Apakah arus salir I_D yang diperlukan untuk transistor M_0?

(25 marks/*markah*)

(b) Suppose if the tail current I_T is 150 µA, what are the drain currents required for the transistors M_7 and M_9.

Diberi arus ekor I_T adalah 150 µA, apakah arus-arus salir yang diperlukan untuk transistor-transistor M_7 dan M_9.

(25 marks/*markah*)

(c) Find widths for transistors M_7, M_8 and M_9. Explain differences between sizes of pMOS and nMOS transistors.

Cari kelebaran-kelebaran bagi transistor M_7, M_8 dan M_9. Terangkan perbezaan di antara saiz transistor pMOS dan nMOS.

(50 marks/*markah*)

3. (a) Draw a simple resistor divider with gain = 0.7 followed by an amplifier (Gain =1) and low pass filter (fc = 1 MHz). (R_1 = 45 kΩ, R_2 = 100 k Ω, R_{LP} = 100 Ω).

Lukiskan satu pembahagi perintang mudah dengan gandaan = 0.7 dan diikuti dengan satu penguat (gandaan = 1) dan penuras laluan-rendah (fc = 1 MHz). (R_1 = 45 kΩ, R_2 = 100 k Ω, R_{LP} = 100 Ω).

(10 marks/*markah*)

(b) Find the noise density at low frequencies by assuming the low pass filter has no effect.

Carikan ketumpatan hingar pada frekuensi-frekuensi rendah dengan menganggap penuras laluan-rendah tidak memberi kesan kepada hingar tersebut.

(50 marks/*markah*)

(c) Given a wafer cost is MYR 10600, the wafer diameter is 12-inch, estimated one die cost is MYR 16 and the die size is 69 mm^2. With the details of the information of an Integrated Circuit (IC) design project, estimate the wafer yield.

Diberikan kos wafer ialah RM 10600, diameter wafer ialah 12 inci, anggaran kos untuk satu dadu ialah RM 16 dan luas untuk dadu litar bersepadu tersebut ialah 69 mm^2. Dengan maklumat yang terperinci untuk satu projek rekabentuk litar bersepadu, kirakan hasil wafer.

(40 marks/*markah*)

4.

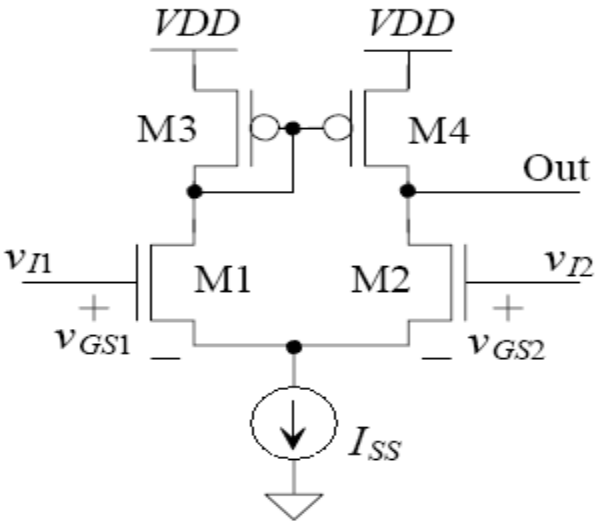

Figure 4. Differential Amplifier

Rajah 4 Penguat Kebezaan

(a) (i) Derive the maximum voltage on the gate of M1.
Terbitkan voltan maksimum bagi get M1.

(50 marks/*markah*)

(ii) Assume that W/L of M1 and M2 is 10/2, $\mu_n.C_{ox}$ = 120 μA/V^2 and I_{SS} = 40 μA. If V_{I2} = 2.5 V (common mode voltage), calculate the maximum and minimum voltage on the gate of M1 that ensures neither M1 nor M2 shut off.

Sekiranya W/L bagi M1 dan M2 ialah 10/2, $\mu_n.C_{ox}$ = 120 μA/V^2 dan I_{SS} = 40 μA. Jika V_{I2} = 2.5 V, kirakan voltan maksimum dan minimum bagi get M1 supaya M1 dan M2 tidak tutup.

(20 marks/*markah*)

(b) (i) What is the first order differential mode gain?
Apakah tertib pertama gandaan mod kebezaan?

(15 marks/*markah*)

(ii) Calculate the differential mode gain if λ_n = 0.01 V^{-1} and λ_p = 0.0125 V^{-1}
Kira gandaan mod kebezaan apabila λ_n = 0.01 V^{-1} dan λ_p = 0.0125 V^{-1}

(15 marks/*markah*)

5. (a) (i) Derive the transition frequency f_T of a transistor.
Terbitkan frekuensi alihan f_T untuk transistor.

(40 marks/*markah*)

(ii) Based on the given parameter associated to transistor (C_{gs} = 0.1 pF, g_m = 0.02 A/V, C_{gd} = 0.01 pF and C_{db} = 0.001 pF) in Figure 5, calculate the transition frequency.

Berdasarkan parameter yang diberikan untuk transistor bagi Rajah 5 di bawah (C_{gs} = 0.1 pF, g_m = 0.02 A/V, C_{gd} = 0.01 pF and C_{db} = 0.001 pF), Kirakan alihan frekuensi.

(10 marks/*markah*)

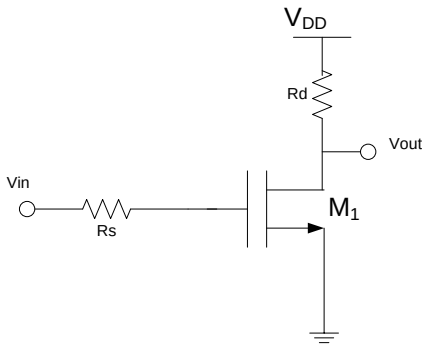

Figure 5

Rajah 5

(b) The transfer function of above circuit (Figure 5) is,

Rangkap pindah untuk litar pada Rajah 5 ialah,

$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-g_m R_D}{(1+\frac{s}{\omega_{in}})(1+\frac{s}{\omega_{out}})}$$

.

(i) Determine the expression for input pole and calculate the value if Rs = 50 Ω, C_{gs} = 0.2 pF, g_m = 0.025 A/V, Rd = 600 Ω, C_{gd} = 0.01 pF and C_{db} = 0.001 pF

Tentukan ungkapan untuk kutub masukan dan kirakan nilainya jika Rs = 50 Ω, C_{gs} = 0.2 pF*,* g_m *= 0.025 A/V, Rd = 600 Ω,* C_{gd} *= 0.01 pF dan* C_{db} *= 0.001 pF*

(25 marks/*markah*)

(ii) Determine the expression for output pole and calculate the value if Rs = 50 Ω, C_{gs} = 0.2 pF, g_m = 0.025 A/V, Rd = 600 Ω, C_{gd} = 0.01 pF and C_{db} = 0.001 pF

Tentukan ungkapan untuk kutub keluaran dan kirakan nilainya jika Rs = 50 Ω, C_{gs} *= 0.2 pF,* g_m *= 0.025 A/V, Rd = 600 Ω,* C_{gd} *= 0.01 pF dan* C_{db} *= 0.001 pF*

(25 marks/*markah*)