ANALYTICAL MODELLING OF BREAKDOWN EFFECT IN GRAPHENE NANORIBBON FIELD EFFECT TRANSISTOR

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ANALYTICAL MODELLING OF BREAKDOWN EFFECT IN GRAPHENE NANORIBBON FIELD EFFECT TRANSISTOR

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

θ angle in radians

L_d Length of velocity saturation region

α Ionization coefficient

V_{gs} Gate-source voltage

V_{th} Transistor threshold voltage

V_{sat} Drain saturation voltage

V_{gs} Drain-source voltage

I_D Drain current

L Channel length

L_E Effective channel length

BV Breakdown voltage

t_f Front gate oxide thickness

t_b Back gate oxide thickness

t_{si} Silicon channel thickness

F Electric field strength

q Charge magnitude

E_t Ionization threshold energy

x Lateral distance

$M(x)$ Multiplication factor

α_n Ionization coefficient of electrons

α_p Ionization coefficient of holes

I_{sub} Substrate current

a Graphene lattice constant

m_h Hole effective mass

m_e Electron effective mass

m_0 Free electron mass

I_{on} On current of FET

I_{off} Off current of FET

V_{tn} N-channel threshold voltage

V_{tp} P-channel threshold voltage

f Frequency

E_g Bandgap energy

$\bar{h}$ Reduced Plank's Constant

W_g GNR's width

υ_F Fermi Velocity

μ_{FE} Field effect mobility

g_m Transconductance

V_s Drain-Source voltage

C_g Gate capacitance

t_{ox} Gate oxide thickness

ε_{ox} Oxide dielectric constant

C_q Quantum capacitance

C_{ox} Oxide capacitance

ϕ Surface potential

V_g Gate voltage

N Doping concentration

n Carrier concentration

V_{bi} Built-in voltage

V_{FB} Flat band voltage

λ_E Energy mean free path

λ_m Momentum mean free path

τ_E Energy mean free time

τ_m Momentum mean free time

V_T Thermal voltage

ε_g Graphene dielectric constant

t_g Graphene nanoribbon thickness

V_{sub} Substrate voltage

Q Charge

ϕ_{ch} Surface potential at the centre of the channel

n_{2D} 2D carrier concentration

$f(E - E_F)$ Fermi Dirac distribution function

K Boltzmann Constant

T Temperature

E_{Fs} Source Fermi Energy

E_{Fd} Drain Fermi Energy

ξ Lateral electric field

ρ_m mass density of graphene

$\upsilon_p h$ Sound velocity in 2D graphene

D Acoustic deformation potential

υ_g Group velocity in graphene

υ_{sat} Saturation velocity of carriers

ω_{op} Optical phonon frequency

N_{op} Occupation number

LIST OF ABBREVIATION

LVSR Length of Velcity Saturation Region

FET Field Effect Transistor

GNR Graphene Nanoribbon

CNT Carbon Nanotube

Sat Saturation

MOSFET Metal Oxide Field Effect Transistor

BJT Bipolar Junction Transistor

CMOS Complementary Metal Oxide Field Effect Transistor

PDP Power Delay Product

ITRS International Roadmap for Semiconductor Technology

GNRFET Graphene Nanoribbon Field Effect Transistor

SG Single Gate

DG Double Gate

APD Avalanche Photo Diode

HEMT High Electron Mobility Transistor

2D Two-Dimensional

1D One-Dimensional

RTL Resistor Transistor Logic

BL Bilayer

SL single Layer

3D Three-Dimensional

ES Equilibrium State

LB Lucky Ballistic

LD Lucky Drift

CNTFET Carbon Nanotube Field Effect Transistor

PEMODELAN ANALITIKAL KESAN PECAH RUNTUH TRANSISTOR KESAN MEDAN NANORIBBON GRAPHENE

ABSTRAK

Sejak tahun 2004, aplikasi graphene sebagai saluran transistor telah menjadi tumpuan kerana kelebihan dari segi berskala luar biasa dan mempunyai mobiliti pembawa yang tinggi. Permodelan kesan voltan runtuh (BV) terhadap transistor medan elektrik graphene nanoribbon (GNRFET) diperlukan untuk mengkaji had voltan operasi untuk transistor. Walau bagaimanapun, sehingga kini tiada kajian yan terperinci mengenai pendekatan analisis dan pemodelan pada kesan BV untuk transistor yang berasaskan graphene. Oleh itu, tujuan projek ini adalah untuk mewujudkan model separuh analisis untuk medan elektrik sisi, panjang halaju kawasan ketepuan (LVSR) ,pekali pengionan (α), dan voltan runtuh transistor medan nanoribbon graphene (GNRFET). Metodologi projek ini di mana mengaplikasikan undang-undang Gauss di kawasan saliran dan punca untuk menerbitkan persamaan potensi permukaan dan medan elektrik sisi. Setelah itu,LVSR dihitungkan sebagai penyelesaian untuk potensi permukaan pada keadaan tepu. Pengionan pekali dimodelkan dan dihitungkan dengan menerbitkan persamaan kebarangkalian perlanggaran dalam mod balistik dan hanyut dengan berdasarkan teori hanyutan bertuah pengionan. Tenaga ambang pengionan dihitungkan dengan menggunakan simulasi dan persamaan empirikal yang diterbitkan daripada analitikal separuh.Akhirnya keadaan pecahan runtuhan digunakan untuk menghitungkan BV sisi. Hasil daripadakajian ini, model analisis dan separa analisis yang mudah telah dicadangkan untuk LVSR, α, dan BV, yang boleh digunakan di dalam mereka bentuk dan pengoptimuman peranti semikonduktor dan penderia

yang berasaskan graphene. Aplikasi penggunaan persamaan yang dicadangkan BV telah dikaji dengan keadaan situasi yang berbeza iaitu panjang saluran, bekalan voltan,ketebalan oksida, lebar GNR dan voltan get. Keputusan simulasi menunjukkan voltan operasi FET boleh serendah 0.25 V untuk mengelakkan pecah runtuh. Walaubagaimanapun, selepas pengoptimuman ia boleh dicapai sehingga 1.5 V.

ANALYTICAL MODELLING OF BREAKDOWN EFFECT IN GRAPHENE NANORIBBON FIELD EFFECT TRANSISTOR

ABSTRACT

Since 2004, graphene as transistor channel has drawn huge amount of attention due to its extraordinary scalability and high carrier mobility. In order to open required bandgap, its nanoribbon form is used in transistors. Breakdown effect modelling of the graphene nanoribbon field effect transistors (GNRFET) is needed to investigate the limits on operating voltage of the transistor. However, until now there is no study in analytical approach and modelling of the breakdown voltage (BV) effects on the graphene-based transistors. Thus, in this project, semi-analytical models for lateral electric field, length of velocity saturation region (LVSR), ionization coefficient (α), and breakdown voltage (BV) of single- and double-gate graphene nanoribbon field effect transistors (GNRFET) are proposed. As the methodology, the application of Gauss's law at drain and source regions is employed in order to derive surface potential and lateral electric field equations. Then, LVSR is calculated as a solution of surface potential at saturation condition. The ionization coefficient is modelled and calculated by deriving equations for probability of collisions in ballistic and drift modes based on lucky drift theory of ionization. Then the threshold energy of ionization is computed using simulation and an empirical equation is derived semi-analytically. Finally avalanche breakdown condition is employed to calculate the lateral BV. As a result of this research, simple analytical and semi-analytical models are proposed for the LVSR, α, and BV, which could be used in design and optimization of semiconductor devices and sensors. The proposed equations is used to examine the BV at

different situations of various channel lengths, supply voltages, oxide thickness, GNR widths, and gate voltages. Simulation results show the operating voltage of FETs could be as low as 0.25 V in order to prevent breakdown. However, after optimizations it can be reached to 1.5 V.

CHAPTER 1

INTRODUCTION

1.1 Overview

In this section, firstly, a brief background is presented to explain the issues connected with CMOS scaling and breakdown voltage. Secondly, the research objectives, scope, plan, and a brief methodology of this project are expressed.

1.2 Background

Metal oxide field effect transistor (MOSFET) as shown in Fig. 1.1 has been the most used semiconducting device for low power logic circuits, power MOSFETs and analogue applications. The key advantages of MOSFET compared to previous counterparts such as resistor-transistor logic (RTL) and bipolar-junction transistor (BJT) are its low power consumption and high input impedance due to isolation of gate from channel. However, high delay of CMOS (Complementary MOS) used in digital applications has been always an issue compared to high switching frequency of for example BJT logics.

For decades there has been a lot of improvements in lowering power and delay in MOSFETs by changing the gate dielectric, altering the structure and using different layers, adding several gates leading to double-gate, triple gate and even surrounding gate MOSFETs to control the channel better, and obviously employing different channel material such as GaAs instead of silicon to increase the carrier velocity.

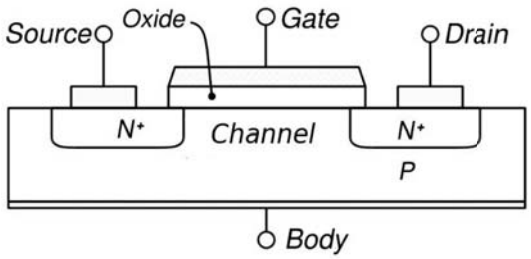

Figure 1.1: Conventional MOSFET with isolated gate from channel using oxide. Each FET consists of four main parts, drain, source, gate and channel. Gate is responsible to control conductivity of the channel and establish current flow between drain and source.

Alternatively, shrinking transistor sizes has been one of the most significant solutions for improving power-delay product (PDP). Reducing the channel length, results in lowering the channel resistance and delay. In addition, it causes the gate capacitance, which is the most important factor in logic gates' delay, to reduce (*International roadmap for semiconductor thechnology (ITRS)*, 2013). Having said that, there are limitations, such as short channel effects, preventing scaling down to nanoscale dimensions and reaching desired characteristics.

When the channel length is comparable to the depletion region of the source and drain the device is called a short channel device. In short channel devices, short channel effect arises that limits the device performance.

Therefore researchers have been trying to introduce new materials with higher mobility and scalability. In 2004, Geim and Nikolove (Novoselov et al., 2004) managed to produce stable graphene- one atom thick layer of graphite at room temperature-and measure its mobility. As it was expected from previous theoretical studies, high carrier mobility was measured in graphene, which is a promise for future nanoelectronic devices. In addition to very high carrier velocity, it shows very high conductance, and tunable bandgap. However the main issue with graphene is its zero bandgap which makes it a very poor semiconducting material for application of FETs. Further studies on opening bandgap in graphene, resulted in introduction of Carbon Nanotube (CNT) and graphene nanoribbon (GNR). Fig. 1.2 shows typical samples of

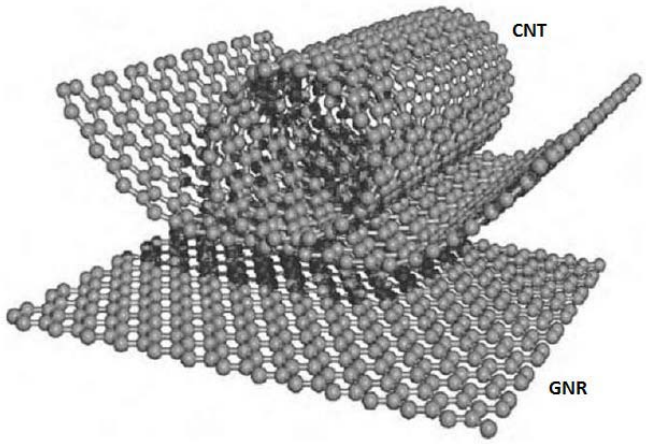

Figure 1.2: Graphene in form of a tube is called carbon nanotube (CNT). Narrow sheet of graphene which is unzipped CNT is known as graphene nanoribbon (GNR)

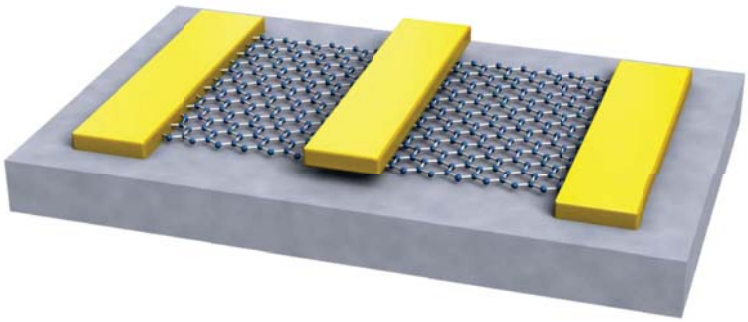

Figure 1.3: Typical GNRFET with top gate and Au drain and source contacts. Graphene nanoribbon is used in channel to decrease the transistor switching time.

GNR and CNT.

Graphene nanoribbons are strips of graphene with narrow width normally less than 50 nm indicating notable electrical properties such as high mobility, high conductance and small bandgap (Novoselov et al., 2004). Recently, GNR has been introduced as an alternative material for the next generation of MOSFETs (Schwierz, 2010). Fig. 1.3 shows a typical graphene nanoribbon FET (GNRFET) with a top gate. Using graphene with thickness as low as possible, the adverse short channel effects in silicon-based MOSFETs could be solved. Therefore, the dimensions of the transistors could be scaled down extremely, which results in low propagation delay down to 0.025 ps (Sako et al., 2011).

However the benefits of GNR come with cost. Firstly, the bandgap opened in GNR is still not enough to secure a satisfactory I_{on}/I_{off} and in narrow ribbons, edge effects suppress the mobility to some values even less than that of silicon counterpart. Secondly, Fabrication of GNR is still a difficult and not accurate task (Schwierz, 2010). Despite great improvement in fabrication process of GNR, it is still not mature enough to be used in mass production and industry. However the research is still vastly going on in this field hoping to find solutions for these issues.

Due to difficulties in fabrication of GNR, many researchers take advantage of analytical modelling and computer simulation to extract details about properties of GNR and possibility of making applicable FETs using GNR. As a result, there are several models for properties of GNR and CNT in the literature. However, since graphene as channel material was introduced recently, there are still many unanswered questions to be explored on these materials. As an example, there has been no attempt to study the breakdown mechanism and ionization process of GNR analytically or experimentally.

Lateral breakdown, which will be the focus of this thesis, is a mechanism limiting the maximum voltage that can be tolerated before the beginning of large current flow between the drain and source in a FET. Prior to calculate the lateral breakdown voltage, impact ionization rate must be computed. Eqn. 1.1 shows the relation of impact ionization and breakdown voltage (Yang et al., 2005).

$$1 = \int_0^{L_d} \alpha dx \tag{1.1}$$

,where L_d is the length of saturation velocity region- a portion of channel between pinch-off point and drain- and α is the impact ionization which is the number of electron-hole pairs created by a mobile carrier travelling a unit of distance along the lateral electric field (Rubel et al., 2011).

When a sufficient electric field is applied between drain and source, mobile carriers gain enough energy to create electron hole pairs by colliding to lattice atoms resulting in impact ionization (Wong, 2000; Kim et al., 1996). This process (impact ionisation) defines the current which flows in the depletion region when a large electric field is applied.

In this thesis, a study on effects of lateral breakdown voltage of GNR-based FETs is conducted. As a results of this thesis, several analytical models are proposed for breakdown mechanism and safe operating voltage of typical devices is calculated analytically. In addition, future studies on design and optimization of related devices such as power FETs or avalanche photo diodes (APDs) could use the proposed approach here.

1.3 Problem statement

Increasing the drain-source voltage (V_{ds}) in FETs causes the drain-source current (I_{ds}) to increase. However, there is a limit (breakdown voltage (BV)) in increasing V_{ds}. After that limit, the device does not function properly and either it conducts high amount of current or cut the current both being a failure in a circuit. Therefore, it is necessary to identify BV of any new material in the devices in order to limit the operating voltage. While in carbon-based FETs, which is the most important device in carbon-based digital and analogue circuits, there is shortage of research on breakdown voltage. Therefore, it was a motivation for us to examine the breakdown and ionization mechanisms in GNRFETs. In this project, an analytical approach is presented to calculate maximum operating voltage of GNRFETs.

1.4 Research limitations and assumptions

As fabrication of carbon-based devices requires sophisticated equipments such as advanced and accurate CVD (Chemical vapour deposition) machine, and precise photo lithography, fabrica-

tion is not possible with the available equipments in our university. Therefore, our research is limited to analytical models and computer simulations only. We only address lateral breakdown and ionization. In addition, among variety of devices such as bilayer-GNRFET, CNT-FET, we limit this project to mono-layer GNRFET for simplicity to make sure that we can achieve our objectives. However, both single-gate and double-gate FETs are modelled and breakdown voltage is calculated.

1.5 Research objectives

i. Objective 1

   To propose analytical models for lateral electric field and length of velocity saturation region of GNR-based FETs

ii. Objective 2

   To propose an analytical model for ionization coefficient and breakdown voltage of GNR-based FETs

iii. Objective 3

   To simulate GNR-based FETs in terms of breakdown voltage and calculate the maximum operating voltage of the typical GNRFETs at different conditions

1.6 Research Methodology

The modelling in this project is divided into three different sections. The first section deals with surface potential, lateral electric field, and length of velocity saturation region. The secondly, section provides models for ionization coefficient, and in the last section the model for breakdown voltage is provided.

1.6.1 Length of saturation velocity region

Surface potential will be modelled using application of Gauss law at drain and source regions of graphene nanoribbon channel. As Fig. 1.4 shows, the models are derived using one-dimensional approach for simplicity. Firstly, we start by applying Gauss's Law inside the channel to obtain Poison's Equation. Then surface potential is resulted by solving the Poison's Equation. By taking derivation, lateral electric field can be obtained. In addition, using the surface potential expression, the length of velocity saturation region is achieved.

1.6.2 Impact ionization coefficient

Impact ionization model can be derived based on general lucky drift theory reported in (Fawcett et al., 1970) and successfully used for semiconductors with parabolic bandstructure such as Si, GaAs etc (Rubel et al., 2011). In this method, it is assumed that a carrier can reach threshold energy in two ways. First it reaches threshold energy through a ballistic motion. Secondly, the carrier first undergos some collisions, then reaches the threshold energy. Therefore, the motion of electron is modelled in both drift and ballistic modes. First, an expression for characteristic length being the distance carriers travel before reaching threshold energy having no collision is derived. Then the probability of having no collision travelling characteristic length in both ballistic and drift modes is formulated. Adding two probabilities gives the total probability of reaching threshold energy. It is worth to mention that due to unusual properties of GNRs, significant modification must be made to the previous models, which are discussed in the relevant section.

1.6.3 Breakdown mechanism

Finally, the breakdown voltage is modelled. The model relies on Fullop's integral, which has been used many times for calculation of BV in silicon-based transistors (Yang et al., 2005). In

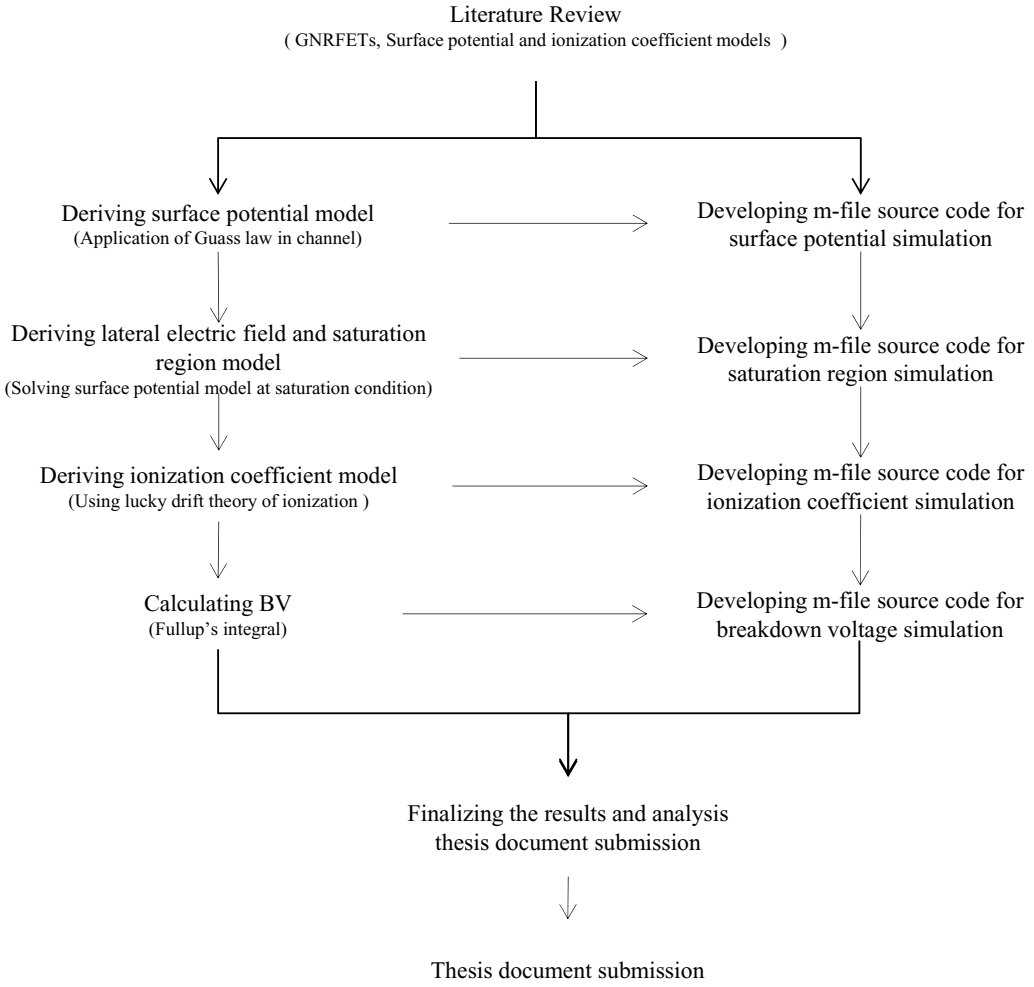

Figure 1.4: Flow chart used to conduct this project.

this method, firstly multiplication factor is calculated and then by equating the multiplication factor to infinity (avalanche breakdown condition), *BV* is calculated. The drain source voltage is increased until the avalanche condition is satisfied. The obtained V_{ds} is called breakdown voltage resulting in infinite multiplication factor. In summary, a flow chart shown in Fig. 1.4 is used to conduct this project.

1.7 Thesis organisation

This thesis is organized as follows. Chapter 2 provides the basic concepts regarding the length of saturation velocity region, ionization mechanism and lateral breakdown voltage. Furthermore useful equations and definitions will be provided there. In addition, more information will

be given focusing on the advantages and disadvantages of graphene, application of graphene in FETs and required equations and properties used in this thesis. Chapter 3 will review literature in three sections, surface potential models, ionization coefficient models and graphene-based transistors. In continue the methodology to conduct this research is presented in three sections of chapter 4 consisting three types of analytical models. The next chapter presents the simulation results based on the proposed models at different values of structural parameters. A comparison between double-gate (DG) and single-gate (SG) will be conducted as well. Chapter 5 presents a summary of this thesis, outlines the achieved results and recommends possible future works.

CHAPTER 2

BASIC CONCEPT OF FIELD EFFECT TRANSISTORS

2.1 Overview

In this chapter first the basic concept of FETs is introduced. In addition, in three subsections, the concepts related to the length of saturation velocity region, impact ionization and lateral breakdown are discussed. Finally, graphene is introduced as a candidate for transistor channel and its properties related to FET are studied.

2.2 Field effect transistors (FET) and its issues

A FET, shown in (Fig. 2.1), is simply a device consisting of a gate, a channel region **which** connects the source and drain junctions, and a barrier which separates the channel from the gate. By controlling the channel conductivity in FETs the drain current increases or decreases. The channel conductivity varies by changing the applied voltage between gate and source. A threshold voltage V_t is defined in FETs as the minimum voltage of gate-source to form a conducting channel between drain and source.

There are three main regions in each voltage transfer characteristic, cut-off, linear and saturation. In cut-off state, where $V_{gs} < V_{th}$ no conducting channel is formed and therefore no current flows. In the linear region, $V_{gs} > V_{th}$ and $V_{ds} < V_{sat}$, where V_{sat} is the drain saturation voltage. In this region as V_{gs} increases, the current increases too almost linearly respect to V_{gs}. The last is saturation region (see Fig. 2.2), where as V_{ds} increases current increases slightly.

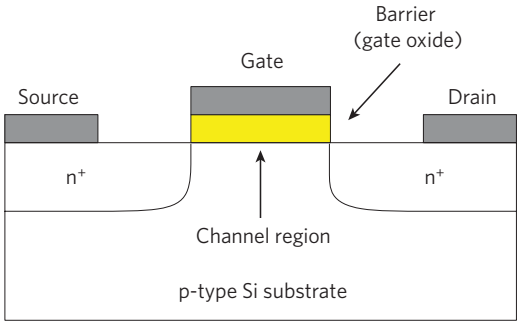

Figure 2.1: Conventional FETs. Schematic cross section of an n-type bulk silicon FET. (Extracted from (Schwierz, 2010))

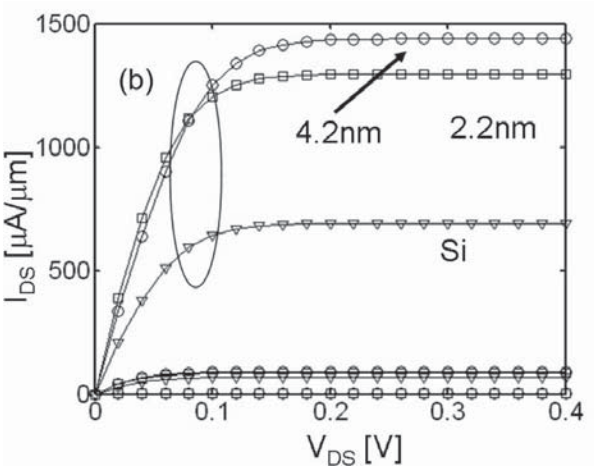

Figure 2.2: FET transfer characteristics showing I_D against the gate-source voltage, V_{gs}. Increasing V_{ds} causes the current to increase. However, after a certain V_{ds}, which is called saturation voltage (V_{th}) a saturation point is reached and the current does not increase as V_{ds} increases.

In this region carriers' speed reaches velocity saturation υ_{sat} and does not exceed that due to collisions, which deviate carriers from lateral direction and reduces their velocity.

2.3 Length of velocity saturation region

The effective channel length is one of the most important parameters of MOSFETs showing the portion of the channel that contribute to the properties of the MOS such as current-voltage (I-V) characteristic. In order to calculate effective channel length, which is $L_E = L - L_d$, the length of the drain region L_d has to be computed. The L_d controls the lateral drain breakdown voltage (Wong, 2000), substrate current, hot-electron generation (Arora and Sharma, 1991), and drain current at the drain region (Gildenblat et al., 2006). In a FET, if the applied drain

voltage is higher than the drain saturation voltage, the electric field near the drain junction will be higher than the critical field strength, which results in carrier velocity saturation. In addition, high electric field near the drain junction causes impact ionization (Wong and Poon, 1997). Saturation region is defined as the region between pinch-off point and drain (see Fig. 2.3).

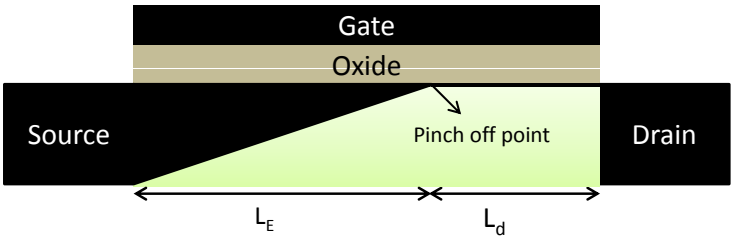

Figure 2.3: Length of velocity saturation region L_d and pinch off point. At high electric field, carriers velocity reaches a saturation velocity and current saturates. Impact ionization occurs in the region between pinch-off and drain.

As reported in (Wong, 2000; Singh, 2005) the length of this region is used along with Fulop's Integral to calculate breakdown voltage (BV) in FETs. In high power devices, a drift region is normally formed outside the gate area to increase the breakdown voltage and length of saturation region is approximated to the length of drift region (Kim et al., 2010; Dang, 1977). Fig. 2.4 shows a schematic view of a typical power device. In this figure, the length of velocity saturation region L_d and the effective channel L_E separated by pinch-off point are shown.

2.4 Impact ionization

As the feature size of integrated MOS devices decreases further, the high electric field near the drain region becomes more crucial and poses a limit on the device operations, notably by a large gate current, substrate current and substantial threshold voltage shift, hot electron generation and drain breakdown caused by the impact ionization in the high field region near the drain. The key parameters for describing these mechanisms are the impact ionization rate

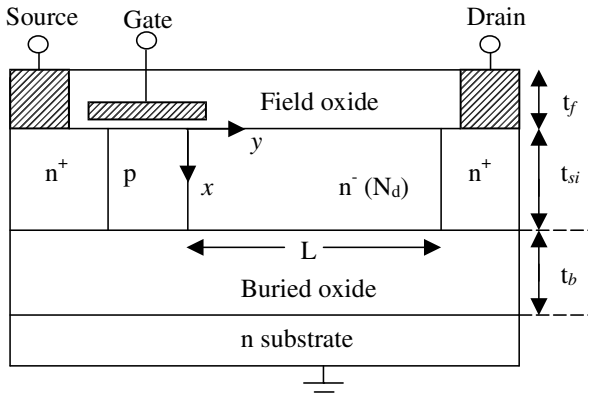

Figure 2.4: A typical power transistor with drift region outside gate area. The t_f, t_b, t_{si} are front oxide, back oxide, channel thickness respectively and L is the length of drift region or L_d. In conventional power devices, increasing drift region length (L) causes the breakdown voltage to increase. (Figure has been extracted from (Yang et al., 2005))

and the length of velocity saturation region.

The definition of impact ionization is the number of electron-hole pairs created by a mobile carrier travelling unit of distance through the depletion region along the direction of the electric field (Rubel et al., 2011). According to several previous works such as (Rubel et al., 2011), the electrons and holes impact ionization coefficients are strongly dependant on the electric field strength. It can be formulated as the inverse of the average distance travelled by a carrier prior to the ionization event and it is given by $\alpha = P(F,E_t)/l_0$, where $P(F,E_t)$ is the probability that electron reaches threshold energy E_t defined as minimum energy required to free an electron (Ridley, 1983). In this equation, α is the impact ionization coefficient of GNR, F is the electric field strength, and $l_0 = E_t/qF$ is the distance travelled by carrier prior to impact ionization assuming no collision is possible.

Impact ionization is an important charge generation mechanism. It occurs in many semiconductor/devices and it may either considered as beneficial characteristic of the device or it can result in unwanted parasitic effects (Maes et al., 1990). For example, it is exploited in avalanche photo diodes (APD).

An avalanche photodiode (APD) is light-sensitive electron device employing the photo-electric effect to interpret the intensity of the light to electricity. Applying high reverse bias (typically 100-200 V in silicon) results in a gain (roughly 100) caused by impact ionization and avalanche phenomenon.

2.5 Lateral breakdown

One the most important and unique properties of power devices is their capabilities to resist high voltages and currents (Wong, 2000; Dang, 1977). In design of transistors used for digital applications, reducing power consumption and increasing the performance are two important objectives. One of the most influential parameter in reducing power is lowering the supply voltage (Su et al., 2008). In contrast, in power devices, such as transistors used to derive electric motors, the operating voltage is much higher than that of digital applications. Therefore, high breakdown voltage is required. Based on the application, the BV could be varied from around 20 up to 30 V for voltage regulators used in power supply circuits in order to supply voltage for processors to over 5000 V for devices, which is employed in power transmission lines (Wong, 2000). However, in nanotransistors, this voltage decreases down to even less than 2V (Su et al., 2008).

Tolerating high voltages without showing high and uncontrolled current flow in a semi-conducting device is ruled by the avalanche breakdown related to the lateral electric field in the device (Krizaj et al., 1996). Normally high electric field is seen inside the structure of the device or at the edges (Kim et al., 1996). Therefore, the device is optimized to tolerate high drain-source voltages while the on-state voltage drop must be kept as low as possible in order to reduce the power dissipation (Kim et al., 1996).

2.5.1 Multiplication coefficient and ionization integral

The condition for occurring avalanche breakdown is met if the rate of the impact ionization becomes infinite. If the electric field is increased enough, it reaches a certain level, where the carriers could be accelerated and finally gain enough energy to generate electron-hole pairs by colliding to lattice atoms. According to definition of the impact ionization coefficient, any hole creates $[\alpha_p\, dx]$ pairs of electron-hole by travelling dx in the depletion region. Concurrently, the electron does the same and creates $[\alpha_n dx]$ pairs travelling the distance dx. Therefore, $M(x)$, which is known as the multiplication coefficient, defined as the number of electron-hole pairs generate by a single electron-hole pairs firstly created at a distance x from the source junction, is written by (Baliga, 2008) as

$$M(x) = 1 + \int_0^x \alpha_n M(x)dx + \int_x^{L_d} \alpha_p M(x)dx \tag{2.1}$$

, where can be written by (Baliga, 2008) as

$$M(x) = M(0)exp\left(\int_0^x (\alpha_n - \alpha_p)\, dx\right) \tag{2.2}$$

, where $M(0)$ is the total number of electron-hole pairs at the edge of the depletion region, and α_n and α_p are ionization coefficients of electrons and holes respectively. Applying this equation in 2.1 and taking $x = 0$ gives a solution of $M(0)$ (Baliga, 2008).

$$M(0) = \left(1 - \int_0^{L_d} \alpha_p exp\left(\int_0^x (\alpha_n - \alpha_p)\, dx\right) dx\right)^{-1} \tag{2.3}$$

Again Using this equation in 2.2 provides (Baliga, 2008)

$$M(x) = \frac{exp\,(\int_0^x (\alpha_n - \alpha_p)\, dx)}{1 - \int_0^{L_d} \alpha_p exp\,(\int_0^x (\alpha_n - \alpha_p)\, dx)\, dx} \tag{2.4}$$

This equation is useful for calculation of the total number of electron-hole pairs caused by the creation of a single electron-hole pair at a distance x from the junction provided that the lateral electric field strength and distribution (in transistors) is calculated.

The avalanche breakdown condition, which is met when the total number of generated electron-hole pairs in the depletion region is almost infinite, can be interpreted as the M almost equal to infinity. This condition is met by assuming the dominator of Eq. 2.4 to 0.

$$\int_0^{L_d} \alpha_p exp\left(\int_0^x (\alpha_n - \alpha_p)\, dx\right) dx = 1 \tag{2.5}$$

The left-hand side expression is referred as ionization integral. In the calculation of breakdown voltage and analysis of the power devices, it is common to find a voltage at which make the ionization integral equal to 1 (Yang et al., 2005). Considering equal coefficient for impact ionization of holes and electrons, the avalanche breakdown condition can be written as (Wong, 2000; Fulop, 1967)

$$\int_0^{L_d} \alpha dx = 1 \tag{2.6}$$

Using this equation, in order to find avalanche condition and breakdown voltage we need to calculate ionization coefficient α, and L_d. This matter will be addressed using semi-analytical approaches in the following chapters.

2.5.2 Avalanche breakdown

Electrons and holes that enters the depletion layer are swept out by the electric field within the depletion region, leading to acceleration of the carriers to high velocities until they reach saturation velocity. If the channel is made of silicon, the saturation drift velocity is about 1×10^7 m/s, which is attained at the electric field more than 1×10^5 cm^{-1} (Wong, 2000). If the electric field increases even more, the mobile carriers can obtain enough energy so that their

collision with lattice atoms could free an electron from the valence band and elevate that to the conduction band resulting in generation of an electron-hole pair (Yeom et al., 1996). Then the created electrons and holes, which are experiencing the electric field, contribute in further impact ionisation and produce even more pairs. As a result, it is said that impact ionisation is a self-progressive (multiplicative) phenomenon, leading excessive mobile carriers, which participate in flowing significant current between drain and source. As the MOSFET is not able to resist the applying higher voltages, due to a rapid increase in the current, the breakdown voltage is known as a limit for operating voltage of MOSFETs (Dang, 1977).

Fig. 2.5 shows breakdown mechanism due to impact ionisation process.

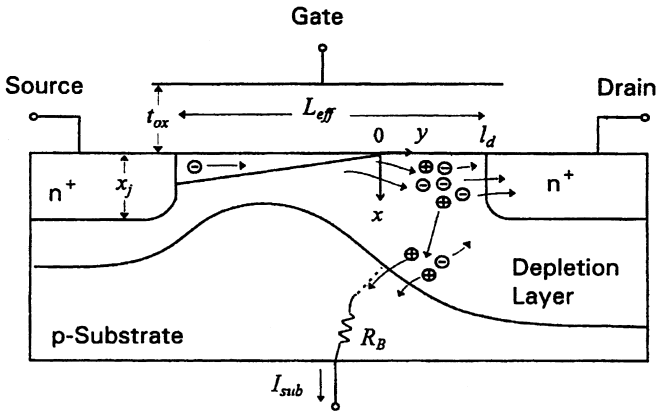

Figure 2.5: Avalanch breakdown and substrate current in a typical FET. Impact ionization results in substrate current, which is undesired characteristic in conventional FETs. (Extracted from (Wong, 2000)).

2.6 Down scaling problems

The performance and power consumption of digital logic relies on almost completely on the efficiency of a single device, which is the MOSFET. As mentioned before, for decades, scaling down the MOSFETs has been the most important action to the succeed in digital logic. This miniaturization has made it possible that the complexity of integrated circuits (ICs) doubles

each 18 months as shown in Fig. 2.6, resulting to essential progress in speed and decreases in power consumption and price per transistor. Nowadays, processors employing two billion FETs, many of them using gate lengths only 30 nm or less, are being produced (Fig. 2.6).

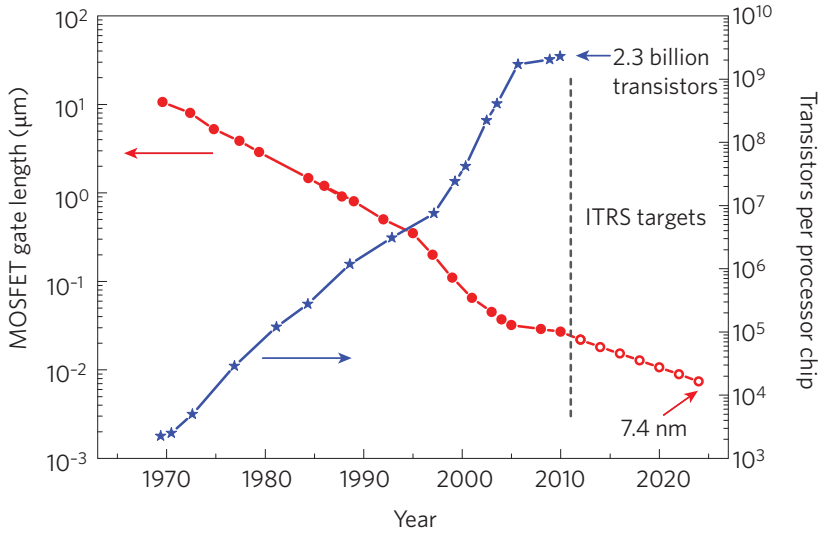

Figure 2.6: Trends in the number of transistors per digital chips and transistor channel. To keep up with this trends length of channel in transistors has been reduced. However, this shrinking cannot continue for too long, which is why new structures such double-gate FETs and new materials like graphene have been introduced hoping to reach even shorter length and higher processing speed. (Extracted from (Schwierz, 2010)

Moore's law has forecast the trend of silicon chips in the last forty years (Krautschneider et al., 1997). For more than four decades, silicon has been the most important CMOS technology of the today's information society. It is thought that silicon is going to be the dominant process for at least one more decade (Krautschneider et al., 1997). However, as transistor dimensions approach few nanometres the silicon transistors' behaviour becomes more uncertain making silicon improper technology for the future circuit's unless new solutions are found to address its issues (Shah and Yang, 1995).

For decades shrinking the dimensions of the channel, oxide thickness and operating voltage has been the most important key to improve the power consumption and performance of the FET devices specially in logic applications. However, this scaling cannot be continued forever

as it has been anticipated several times. After years of threshold voltage downscaling, leakage current has increased from $<10^{-10}$ amp/mm to $>10^{-7}$ amps/μm. Thus it is difficult to further lower the threshold voltage and therefore, the operating voltage cannot be reduced as well (Bohr, 2007).

Another issue arises from scaling the oxide thickness. Although reducing the oxide thickness results in device performance improvement and operating voltage decrease, due to leakage current, it is reaching the limits. Gate oxide in 65 nm technology of Intel FETs (SiO_2) is only 1.2 nm, which is equal to 5 layers of silicon atoms. This shows that downscaling is reaching the dimension of atoms. In other word, we are running out of atoms. Furthermore, there is a limit for increasing the doping concentration. As the doping concentration increases, the carrier velocity degrades due to increase in scattering.

Reducing channel length has been also another key approach to improve characteristics of FET devices. In high-performance applications, FETs must quickly respond to V_{gs} variations, requiring high-mobility and short channel. However, short channel length results in problems such as threshold voltage roll-off, and drain induced barrier lowering (DIBL) (Krautschneider et al., 1997).

Short channel problems (effects) is one of the most challenging issues in the nanoscale MOSFETs. When the channel length is comparable to the junction thickness, which is relevant in nano-transistors, the gate barrier height is lowered, which lead to decreasing the threshold voltage (V_{th}). In addition, if high voltages for drain junction is applied to a short channel transistor, the gate barrier height decreases even more, which causes the threshold voltage to decreases further. This issue is known as drain-induced barrier lowering (DIBL). Eventually, the MOSFET reaches a point called the punch-through, where the gate is totally unable to control the drain-source current flow.

Normally, two physical phenomenon are attributed to the short-channel effects, which are

1. The impairing the drift characteristics of the electron in the short channel
2. The threshold voltage changes because of channel length shortening

In other point of view, short-channel effects are distinguished into five different effects

1. Hot electrons
2. Velocity saturation
3. Surface scattering
4. Impact ionization
5. DIBL and punch-through

According to prediction of scaling theory (Bohr, 2007), in order to make a robust FET against short channel effects, a FET with a thin gate-controlled region (measured in the vertical direction) and a thin barrier must be designed. The fact that in graphene it is possible to have channels that are as thin as one atom layer is perhaps the most interesting properties of graphene for application in transistors (Schwierz, 2010).

Although there are reported devices with extremely thin channels, such as iii-v HEMTs with typical channel length of 10-15 nm and silicon-on-insulator MOSFETs using channel with thickness of less than 2 nm, the rough surface results in deteriorated mobility (Aberg and Hoyt, 2005). More importantly, a significant threshold voltage variation is seen in these devices because there is a fluctuation in body thickness of these devices and the same problem is expected to happen when the thickness of iii-v HEMT is reduced to only a few nanometres

(Schwierz, 2010). These issues are seen at thicknesses that are much greater than that of graphene.

Another important issue in the modern MOSFETs is the series resistance between the source and drain junctions, which is becoming more significant as the gate length is reduced (Krautschneider et al., 1997). Therefore, significant amount of research has been devoted to suppressing the short channel effects and optimizing the series resistance in modern transistors. As a result device engineers have been trying to find alternatives materials with better scalability and higher carrier velocity (Schwierz, 2010). So far graphene has been shown to have very high carrier velocity and scalability compared to silicon and other counterparts such as GaAs.

2.7 Carbon-based devices

As the end of silicon scaling has been predicted number of times due to technical reasons and scaling alone only results in fulfilling the needs of one generation, introducing a fundamentally new material based on essentially different physical properties compared to the silicon is of a great interest among the device engineers.

However, switching to a new material is challenging task to do. Because logic circuit fabrication needs complex processes and device fabrication plants are extremely expensive to implement. In addition, introducing new material requires the fabrication plants to be replaced or modified significantly, which costs a lot of money. Therefore there are objections among logic designers against introducing alternatives for silicon. However, the conditions is not the same for radiofrequency applications. This field is supported and dominated by defence applications. Because of need and advances in wireless communications, the military is wiling to spend great amount of money in research into new radiofrequency devices. In addition, radiofrequency chips are not as complex as the logic circuits are. Therefore, the readiness

for changing the device concept and introducing new devices is much more than that of logic circuits. As indications,it is seen that different materials and device types have been applied in radiofrequency electronics, including high-electron-mobility transistors (HEMTs) based on iii-v semiconductors such as GaAs and InP, silicon n-channel MOSFETs, and different types of bipolar transistors (Moore, 2003).

Graphene, as new material for transistor channel was first introduced for application of radiofrequency. It is hoped that by using graphene, which is one atom thick layer of graphite, it is possible to fabricate MOSFETs with extremely thin channels, which will make these devices able to be scaled to shorter channel lengths and lower delay without facing the short-channel issues that limits the operating frequency of the current silicon devices. Therefore, proposing new devices would be one of the most promising alternatives to improve silicon (Eiji and Takeda, 1997).

Graphene in its mono-layer form is a pure two-dimentional (2D) material. Its lattice comprises regular hexagons of carbon atoms. The graphene lattice constant, a, is 0.246 nm and the bond length of adjacent carbon atoms, L_b, 0.142 nm. The application of this material has been reported long time ago in (May, 1969) when it was not even called graphene. However, all the attempts to make stable graphne all failed. Therefore, for long time it was thought that graphene cannot be existed and stable at room temperature (May, 1969). However, it was experimentally shown to be stable at room temperature in 2004 paper by the Manchester group (Novoselov et al., 2004) to start the huge amount of research on this material.

2.7.1 Advantages of graphene-based electronics

In 2004 an extremely high carrier mobility ($\approx$ 10000 cm^2/V.s) of graphene has been experimentally and theoretically shown (Novoselov et al., 2004). However this property of graphene

needs to be discussed in more detail, which is given later in this chapter. Due to its high mobility, if graphene is applied as material of MOSFETs' channel, those devices could be considered as semi-ballistic transistors. Furthermore, extraordinary high conductance of graphene results in very high current and low delay in carbon-based transistors. The electron or hole transport in graphene occurs in the p-orbitals perpendicular to the surface, and the exceptional transport characteristics have been connected to a single spatially quantized sub-band populated by donor carriers with low effective mass of $m_e = 0.06 \times m_0$ or by light and heavy holes with masses of $m_h = 0.03 \times m_0$ and $m_h = 0.1 \times m_0$ (Eiji and Takeda, 1997). Mean-free path for carriers of $\lambda \approx 400nm$ at 300K, is another prospect of realizing ballistic devices, even at relaxed feature sizes compared to the state-of-the-art CMOS technology (Eiji and Takeda, 1997).

2.7.2 Disadvantages of graphene-based electronics

In the modern digital circuit, complementary MOS (CMOS) is the dominant technology. A CMOS technology apply both n and p type FETs in order to make low power circuits. The main idea is that at final states only one type is on and the other one is completely off so the path between VCC and GND is disconnected.

The major benefit of CMOS over other technologies is that in the final states, a number of the Transistors are in off state resulting in having no static current.This feature of silicon MOSFETs, makes silicon CMOS enable to offer exceptionally low static power consumption. Consequently, any possible successor to the current MOSFET, which is to be applied in CMOS-like logic circuit should have very good switching characteristic, as well as an I_{on}/I_{off}, in range of 10^4 to 10^7 (Aberg and Hoyt, 2005).

To do so, a bandgap of 0.4 eV or more is required in conventional FETs. In addition, to make CMOS circuits, n- and p-type FETs are required with $V_{tn} = -V_{tp}$ for a proper CMOS