A 0.8 – 2.4 GBPS DRIVER WITH ADJUSTABLE DE-EMPHASIS SCHEME FOR DDR3 MEMORY INTERFACE

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A 0.8 – 2.4 GBPS DRIVER WITH ADJUSTABLE DE-EMPHASIS SCHEME FOR DDR3 MEMORY INTERFACE

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LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
BER	Bit Error Rate
CM	Current-Mode
CML	Current-Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CTT	Center-Tap Termination
DAC	Digital-to-Analog Converter
DC	Direct Current
DDR	Double Data Rate
DFF	D Flip-Flop
DRAM	Dynamic Read Access Memory
EOS	Electrical Over-Stress
EQ	Equalization
FIR	Finite Impulse Response
FSM	Finite State Machine
Gbps	Giga bit per second
I / O	Input / Output
IC	Integrated Circuit
ICB	Impedance Calibration Block
ISI	Inter-Symbol Interference
JEDEC	Joint Electronic Device Engineering Council
LPF	Low-Pass Filter

MB	Motherboard
MCH	Memory Controller Hub
ODT	On-Die Termination
OP-AMP	Operational Amplifier
PCB	Printed-Circuit Board
PRBS	Pseudo Random Binary Sequencer
PVT	Process, Voltage and Temperature
RDRAM	Rambus Dynamic Read Access Memory
RX	Receiver
SDRAM	Synchronous Dynamic Read Access Memory
SST	Source-Series Terminated
TX	Driver
UI	Unit Interval
VM	Voltage-Mode

LIST OF SYMBOLS

Ω	Ohm
Ɛr	Relative Permittivity
ρ	Copper Resistivity
μ	Permeability
ΔT	Delay Interval
Δz	Length of Differential Section of a Conductor
C	Dielectric Capacitance
C_{GATE}	Gate capacitance
C_{LOAD}	Load Capacitance
C_{PKG}	Package Parasitic Capacitance
G	Dielectric Conductance
H	Dielectric Height
L	Series Inductance in Conductor
Len	Conductor Length
L_{PKG}	Package Parasitic Inductance
R	Series Resistance in Conductor
R_{EXT}	External On-board Resistance
R_{ground}	Ground Plane Resistance
R_{ODT_PD}	SDRAM On-Die Termination Pull-down Impedance
R_{ODT_PU}	SDRAM On-Die Termination Pull-up Impedance
R_{PD}	Driver Pull-down Impedance
R_{PU}	Driver Pull-up Impedance

R_{signal}	Conductor Resistance
R_S	Series Resistance in Motherboard
T	Conductor Thickness
VBIAS	Transistor Bias Voltage
VCC	Internal Core Supply
VDD	External Core Supply
V_{GS}	Transistor Gate-to-Source Voltage
V_{GD}	Transistor Gate-to-Drain Voltage
VIN	Input Voltage
V_{MAX}	Maximum V_{GS} or V_{GD} before Transistor Gate Destruction
VOUT	Output Voltage
VREF	Reference Voltage
VSS	Ground
W	Conductor Width

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PEMACU 0.8 – 2.4 GBPS DENGAN SKIM "DE-EMPHASIS" BOLEH LARAS BAGI ANTARAMUKA MEMORI DDR3

ABSTRAK

Keperluan lebar jalur memori untuk menaikkan prestasi sistem komputer telah mendorong evolusi memori sistem ke tahap penggunaan teknologi "Double Data Rate Synchronous Dynamic Read Access Memory (DDR SDRAM)". Kecenderungan untuk memaksimakan lebar jalur memori telah menyebabkan Gangguan Antara-Simbol (ISI) menjadi penting dan ia menjejaskan integriti isyarat bagi data yang dihantar. Dalam penyelidikan ini, seni bina pemacu dengan skim kawalan "de-emphasis" dan rintangan boleh laras adalah dicadangkan untuk kadar data dan kepadatan sistem memori DDR3 SDRAM yang tinggi. Pemacu yang dicadangkan dilaksanakan dengan menggunakan proses teknologi CMOS 45 nm. Rekabentuk dan pelaksanaan litar yang dicadangkan melibatkan reka bentuk seni bina pemacu, pengawal data, blok penentukuran rintangan dengan penjana rujukan serta rangka lantai untuk litar analog yang kritikal iaitu tiga segmen pemacu bagi simulasi pasca-rangka lantai untuk memastikan parasitik dalam rangka lantai tidak mempunyai kesan yang besar ke atas prestasi pemacu. Pemacu ini mempunyai 15 kaki "de-emphasis" yang membentuk 15 tahap voltan "de-emphasis" yang mampu mengurangkan ketar ISI yang disebabkan oleh frekuensi operasi yang tinggi. Selain itu, kepadatan sistem memori DDR3 yang tinggi boleh merosotkan ketar mata dan ketinggian mata dan hal ini menyebabkan kesukaran dalam pensampelan dan pemulihan data. Oleh itu, rintangan pemacu yang dicadangkan boleh diprogramkan antara 20, 30 dan 40 Ω untuk mengimbangi kesan perubahan "motherboard routing"

dalam sistem memori bagi memperbaik integriti isyarat. Simulasi pra dan pasca-rangka lantai telah menunjukkan pemacu yang dicadangkan mampu mengurangkan isyarat ketar mata pada 37.3, 37.2 dan 32.5% untuk rintangan 20, 30 dan 40 Ω dengan kod “de-emphasis” yang tertentu. Keputusan keseluruhan yang diperolehi melalui simulasi pra-rangka lantai dan pasca-rangka lantai telah menunjukkan persetujuan yang baik terhadap spesifikasi yang disasarkan.

A 0.8 – 2.4 GBPS DRIVER WITH ADJUSTABLE DE-EMPHASIS SCHEME FOR DDR3 MEMORY INTERFACE

ABSTRACT

The need for greater memory bandwidth to boost the computer system performance has driven system memory evolution to Double Data Rate Synchronous Dynamic Read Access Memory (DDR SDRAM) technologies. Trends to maximize memory bandwidth have caused Inter-Symbol Interference (ISI) become significant which degraded the signal integrity of transmitted data. In this research, a driver architecture with adjustable de-emphasis and impedance control scheme is proposed for high-data rate and high-density DDR3 SDRAM memory system. The proposed driver is implemented using 45 nm CMOS process technology. The designs and implementations of the proposed driver involve the design of driver architecture, data controller, impedance calibration block with reference generator as well as the layout for critical analog circuits i.e. three driver segments for post-layout simulations to ensure the parasitic in layout does not has significant effect on driver performances. The driver has 15 de-emphasis legs that can form 15 de-emphasis voltage levels that capable of reducing ISI-induced jitter at high operating frequency. Moreover, high density DDR3 memory system can deteriorate the far-end eye jitter and eye height that causes difficulties in data sampling and recovery. Thus, the driving impedance of the proposed driver can be programmed between 20, 30 and 40 Ω to compensate the variability of board routing effect in memory system and hence, improving signal integrity. The post-layout simulations show the proposed driver is capable of reducing 37.3, 37.2 and 32.5%

of signal eye jitter for 20, 30 and 40 Ω driving impedance with suitable de-emphasis code selected. The overall results obtained with pre-layout and post-layout show good agreement with the targeted specifications.

CHAPTER 1

INTRODUCTION

This chapter gives the introduction and the motivation behind this research. Moreover, the objectives, scopes and contributions of this research will be presented.

1.1 Background of Study

In modern computer systems, a computer processor performs any useful tasks by copying the corresponding applications from disk drive to system memory for processing and executing purposes. Figure 1.1 shows the connection between processor, system memory and memory controller. System memory consists of DRAM (Dynamic Read Access Memory) chips with memory controller is connected via the memory bus that comprises of data bus and address / command bus.

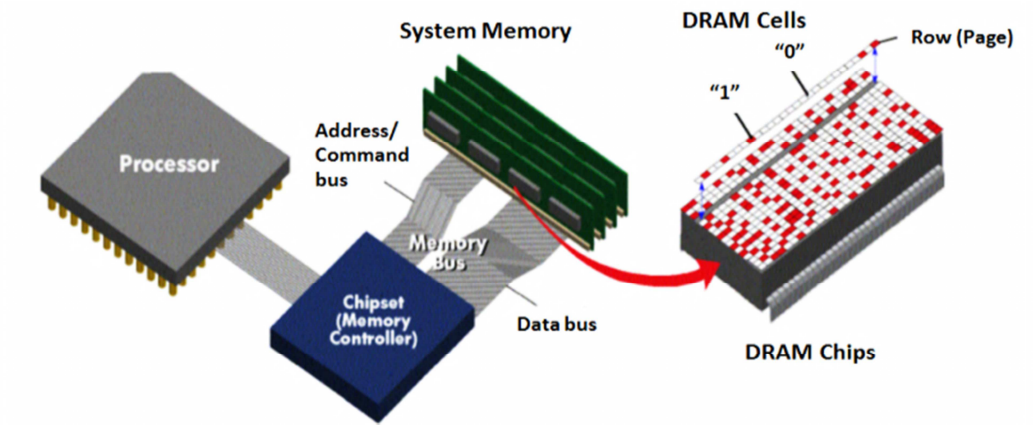


Figure 1.1: Communication of processor to system memory through a memory controller (Memory Technology Evolution, 2010).

In Figure 1.1, however, the read / write operations in system memory are asynchronous as these operations are executed without a memory bus clock. For instance, memory controller determines when to assert read command and expects data returned from system memory based on absolute number of memory clock cycles and this causes longer data transfer delays between memory controller and system memory (Campardo, Micheloni and Novosel, 2005). Therefore, JEDEC (Joint Electronic Device Engineering Council) developed the SDRAM (Synchronous DRAM) technology to reduce the absolute number of memory clock cycles needed for reading or writing data with the use of memory bus clock issued by memory controller to synchronize the operations in SDRAM chip (Memory Technology Evolution, 2010). This reduces processor-to-memory delay and simplifies the design of memory controller since it no longer needs to determine the number of memory clock cycles needed for reading or writing operations (Balch, 2003). Thus, SDRAM reduces delay during data transferring between memory controller and system memory to improve the bandwidth of system memory which improves the computer system performances (Jacob, Ng and Wang, 2007). In addition, the bandwidth of system memory is multiplication of the frequency of transferring data in memory bus and the number of data bits in memory bus. Thus, the bandwidth of system memory can be improved by increasing the frequency of transferring data in memory bus, number of data bits in memory bus or both of them (Balch, 2003). Moreover, the need for greater system memory bandwidth to boost computer system performance is increasing over the years. This has driven evolution of system memory from asynchronous DRAM to SDRAM, RDRAM (Rambus DRAM)

and eventually to DDR (Double Data Rate) SDRAM technologies with the increasing of memory bus frequency, as shown in Figure 1.2 (Memory Technology Evolution, 2010).

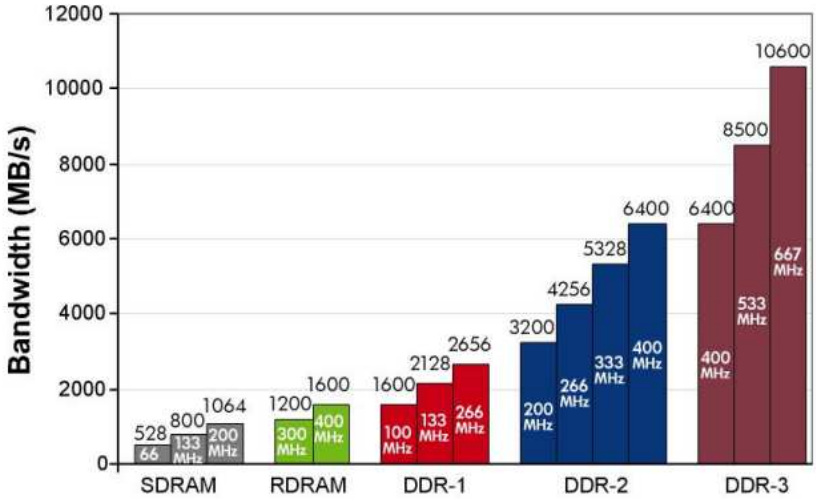


Figure 1.2: System memory evolution from SDRAM to DDR3 technology (Memory Technology Evolution, 2010).

The types of memory technology and their features are discussed as follows (Memory Technology Evolution, 2010):

(1) SDRAM Technology

SDRAM is a memory technology with 3.3 V signaling developed by JEDEC in the early 1990s which uses a memory bus clock issued by memory controller to synchronize the read and write operations in the memory chip. This reduces delay between memory controller and system memory to achieve higher system memory bandwidth as compared to DRAM.

(2) RDRAM (Rambus DRAM) Technology

RDRAM is a memory technology introduced in the late 1990s to achieve higher memory bandwidth than SDRAM with same signaling voltage at 3.3 V. However, the

cost of RDRAM is higher since it utilized high-speed serial link to transfer data between system memory and memory controller, which needs special memory bus design as compared to SDRAM chips.

(3) DDR1 (Double Data Rate 1) SDRAM Technology

DDR SDRAM has similar design with conventional SDRAM, but it has faster bandwidth and lower costs to replace RDRAM in computer system. DDR1 is the first generation of DDR SDRAM technology which uses 2.5 V low-voltage signaling as compared to 3.3 V in SDRAM. This improves heat dissipation due to lower power consumption. Moreover, DDR1 transfers data using both the rising and falling edges of each memory clock cycle without increasing the memory clock frequency. This effectively doubles the data rate as compared to SDRAM and RDRAM that transfers one data by only using the rising edge of memory clock cycle.

(4) DDR2 SDRAM Technology

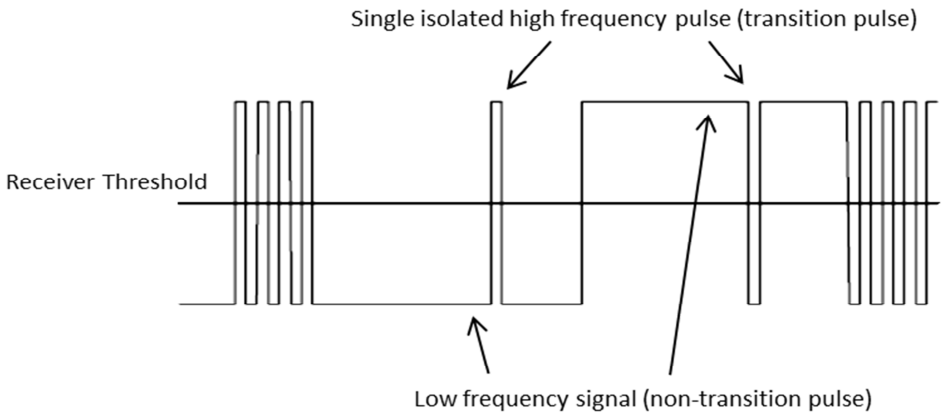
The DDR2 is the second-generation of DDR SDRAM technology. DDR2 achieves lower power consumption by using 1.8 V signaling and gives higher performance via faster clocks up to 400 MHz with memory bandwidth of 6400 MB / s.

(5) DDR3 SDRAM Technology

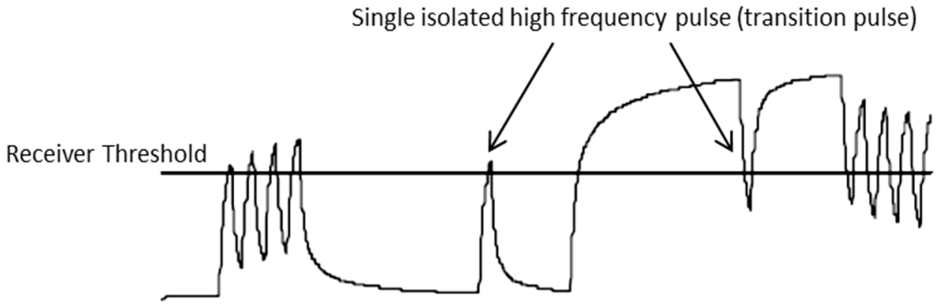
Besides, DDR3 is the third-generation of DDR SDRAM technology which further improves power consumption and memory bandwidth. As compared to DDR2, DDR3 with 1.5 V signaling has reduces the power consumption up to 30 % at same

memory clock frequency. Also, DDR3 can operate at memory clock frequency from 400 MHz to 1200 MHz (not shown in Figure 1.2) to achieve higher bandwidth from 6400 MB / s up to 19200 MB / s to boost the computer system performance.

As the system memory bandwidth increases with memory clock frequency, the major performance limiting factor in computer system with DDR3 memory is the ISI (Inter-Symbol Interference) at memory bus (Mishra et al., 2011). ISI is a phenomenon where a digital symbol on the memory channel is corrupted by its previous symbol traveling on the same channel (Dally and Poulton, 1997; Zhang et al., 2007).



(a)



(b)

Figure 1.3: ISI effect on a digital signal. (a) Original signal with isolated pulses, (b) Attenuation on isolated pulses at receiving-end (Dally and Poulton, 1997).

In high speed communication systems, ISI is most pronounced when a single isolated high frequency pulse is transmitted to transmission channel. In Figure 1.3 (a), there are two single isolated high frequency pulses. Due to ISI in lossy channel, un-attenuated low frequency signal (non-transition signal) before single isolated high frequency pulse can cause it to hardly reach the receiver threshold of the signal swing, resulting very low probability of correct detection as shown in Figure 1.3 (b) (Dally and Poulton, 1997).

Therefore, the impacts of ISI are difficulties in detection and recovery of corrupted symbol. As a consequence, the performance of computer system with DDR3 memory become bottleneck due to ISI impacts as the memory clock frequency is increasing to achieve greater memory bandwidth (Lee, Lee and Nam, 2010; Mishra et al., 2011; Nam, Dreps, Mandrekar and Nanju, 2010). Thus, the work in this research is dedicated to investigate the ISI at high frequency in computer system with DDR3 memory and propose the approaches to minimize the ISI impacts.

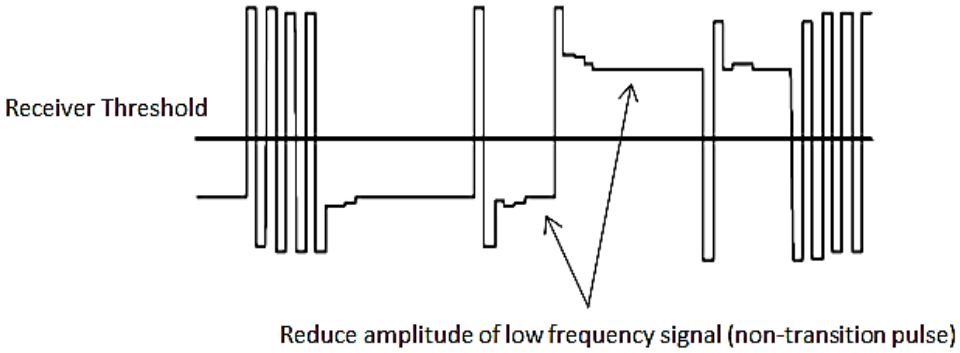
1.2 Problem Statements

Performance of modern computer system is increasingly restricted from greater memory bandwidth due to the existence of ISI on memory channel (Mishra et al., 2011). As a stream of digital symbol transmitted through a memory channel, a symbol can be corrupted by another symbol traveling on the channel at an earlier time. This inter-symbol interference occurs when the energy of earlier symbol being stored in the

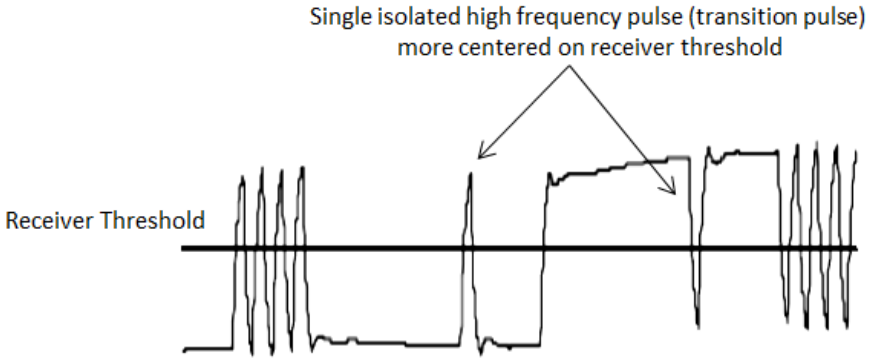
channel sums with the later unrelated symbol, resulting in later symbol corrupted (Dally and Poulton, 1998). ISI can be caused by signal reflection due to termination mismatches between memory channel with driver or receiver. Moreover, the existence of frequency-dependent skin-effect resistance in channel which combines with capacitances along memory channel can form a LPF (Low-Pass Filter) that attenuates high frequency components of a symbol. Thus, ISI happens when the attenuated high-frequency signal components in the lossy channel are overwhelmed by the un-attenuated low-frequency components (Heidar, Dessouky and Ragaie, 2007). This degrades signal noise margins and increases signal jitter which causes data detection and recovery at receiving-end become very challenging. A non-optimal option to minimize ISI is reducing the maximum frequency at which the memory can operate; but, this limits the memory bandwidth and computer performance. Therefore, ISI in lossy channels must be compensated to ensure received signal has good signal integrity for correct data detection and recovery to achieve low BER (Bit Error Rate) (Liu and Lin, 2004).

Driver de-emphasis techniques have been widely used for applications in chip-to-chip communication to compensate ISI and improve the received signal quality for correct clock and data recovery (Liu and Lin, 2004). As mentioned previously, skin-effect resistance in a lossy channel attenuates high frequency components of a signal and causes ISI. Thus, de-emphasis is a technique to attenuate low frequency components of a signal by a factor similar to high frequency attenuation in lossy channel so that all frequency components of a signal are attenuated by similar factor

after the lossy channel (Dally and Poulton, 1997). Figure 1.4 (a) shows a signal with amplitude of low frequency components (non-transition signal) is de-emphasized or reduced before transmitted to channel. In addition, Figure 1.4 (b) shows the received signal at receiver-end. It can be observed that the single isolated pulses and high-frequency segments are centered on the receiver threshold, providing adequate eye openings for data detection.



(a)



(b)

Figure 1.4: (a) Signal with de-emphasis applied to attenuate low frequency components, (b) Received signal with high frequency components are centered on the receiver threshold (Dally and Poulton, 1997).

Therefore, this work focuses on the circuit design, analysis and layout implementation of driver de-emphasis for DDR3 memory interface to overcome ISI at high data rates (i.e. high memory clock frequency) to achieve greater memory bandwidth and boost the performance of computer system with DDR3.

1.3 Research Objectives

The following objectives are set to this research:

(1) To design a driver with adjustable de-emphasis scheme to compensate ISI. Adjustable de-emphasis scheme provides a range of de-emphasis settings that can be selected to effectively compensate ISI.

(2) To design and integrate the adjustable impedance scheme into the proposed driver. Adjustable impedance scheme provides a range of output impedance that can be selected to adjust signal swing and improve signal noise margin.

1.4 Scope of Research

This research focuses on the design and implementation of de-emphasis driver for DDR3 SDRAM memory interface. The proposed driver is designed using 45 nm CMOS process technology. The implementation of the design is from schematic to layout. The software / tools used for the purpose of simulation are: Virtuoso Schematic Editor from Cadence, PRESTO simulator for pre and post-layout simulation and GeneSys Layout Editor from Eagleware for layout design.

1.5 Research Contribution

This research contributes to the knowledge in high-speed I / O design particularly in DDR3 memory system. The design and development of the proposed driver architecture is anticipated to be one of the pioneering attempts in providing new trend of designing a low power driver with adjustable de-emphasis to effectively reduce ISI-induced jitter and improve signal integrity. This research contributes to knowledge in the following specific areas:

(1) Contributes to the knowledge in the R & D (Research and Development) of high-speed I / O (Input / Output) design by presenting systematic circuit design like high-speed driver design, impedance control and output slew rate control technique. In addition, comprehensive design analysis and performance discussion on impedance matching and output slew rate across PVT (Process, Voltage and Temperature) variations are presented.

(2) Exhibits the critical issues and challenges behind the design and development of the proposed driver. As the CMOS semiconductor process continuously scaling down, CMOS device dimension becomes smaller and gate-oxide has becomes thinner. When these devices are used in designing driver for 1.5 V DDR3 memory interface, the high-voltage overstress on the gate oxide can lead to gate destruction since the CMOS devices are operating at voltage higher than their nominal voltage. Thus, special design techniques are demonstrated in this work to avoid device gate over-stressed and reliability issues.

(3) Contributes to the knowledge in memory industry by providing new methodology in the design of driver with adjustable de-emphasis for DDR3 SDRAM memory interface. Moreover, the adjustable de-emphasis scheme provides a range of de-emphasis level that allows the most suitable de-emphasis output to be selected to accurately compensate ISI losses for achieving large signal eye opening at far-end. Consequently, receiver architecture will be less complexity and more power efficient in DDR3 SDRAM memory.

1.6 Thesis Organization

This thesis contains five chapters and is organized as follows:

Chapter 1 gives the introduction and the motivation behind this research. This chapter also includes the research objectives and contribution to the knowledge of science and engineering.

Chapter 2 provides the overview of driver circuit design. Different types of driver architecture and their pros and cons are discussed. This chapter also discusses various techniques to overcome ISI impacts.

Chapter 3 discusses the design methodology and implementation of the proposed driver. Moreover, the circuit design of adjustable de-emphasis control and impedance control scheme is also presented.

Chapter 4 includes the pre- and post-layout simulation results of the proposed driver design. Detail analysis and discussion on the performance of the proposed design are given.

Chapter 5 concludes the findings of the work in this project. It also includes the future works that can be performed to further develop the research on driver circuit in SDRAM industry.

CHAPTER 2

LITERATURE REVIEW

This chapter focuses on the reviews of literatures for different types of driver circuit and discusses the basic operation, pro and con of each driver. Moreover, the equalization techniques to overcome ISI-induced jitter are presented. In addition, special design technique to avoid gate-oxide reliability issue in driver that is designed using thin gate transistor will be discussed. Lastly, slew rate control, impedance control and pad capacitance reduction technique that helps in improving driver performance also will be presented.

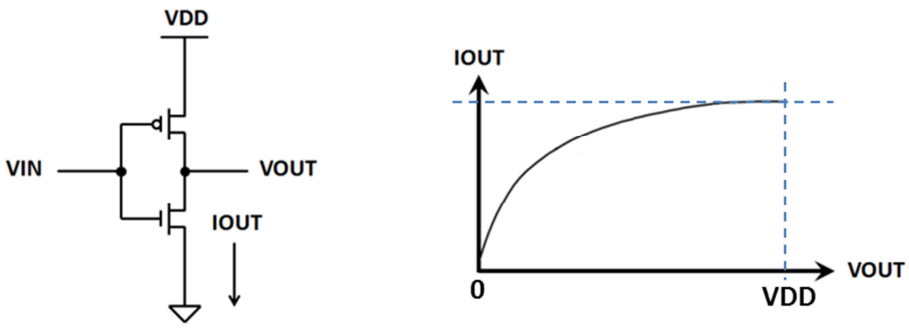
2.1 Driver Circuit

A driver can transmit information by converting data into either current or voltage form over a transmission line (Dally and Poulton, 1998). In this section, two basic types of driver circuit will be discussed, namely voltage-mode driver and current-mode driver.

2.1.1 Voltage-Mode Driver

The simplest voltage-mode driver is a push-pull driver implemented by using a simple CMOS inverter, as depicted in Figure 2.1 (a). Due to the ease of implementation

and low power consumption, push-pull drivers were popular in the early days of CMOS ICs (Dally and Poulton, 1998). They have very low output impedance and are implemented using large transistor operating in linear region. When the input VIN is switching from logic low to high, the PMOS transistor is turned-off and NMOS transistor is turned-on to pull the output node VOUT from VDD towards ground and vice versa. Figure 2.1 (b) shows the pull-down I-V characteristic (NMOS is activated). It can be noticed that the IOUT in non-linear when VOUT is pulled from VDD towards ground, which implies a non-constant output impedance (ΔVOUT / ΔIOUT) across operating voltages. This has caused signal reflection problem due to the impedance mismatched between push-pull driver and transmission line, especially at high operating frequency (Bartolini et al, 2007).



(a) (b)

Figure 2.1: (a) Push-pull driver circuit. (b) Non-linear I-V characteristic of push-pull driver.

On the other hands, source-series terminated (SST) driver is another voltage-mode driver developed to overcome signal reflection problems faced by conventional push-pull driver (Kossel et al., 2008). Figure 2.2 (a) shows the SST driver circuit. It has extra resistor R in series with the pull-up and pull-down segment to limit drain-to-

source voltage of transistors, thereby improving driver linearity. This is one of the important aspects in high speed I / O design since the output driver not only transmits data, but at the same time it also required to function as a terminator to self-terminate any reflected signals (Dally and Poulton, 1998; Kossel et al., 2008; Sang, Young and Man, 2008). Figure 2.2 (b) demonstrates the driver's linearity can be improved by increasing the series resistance value.

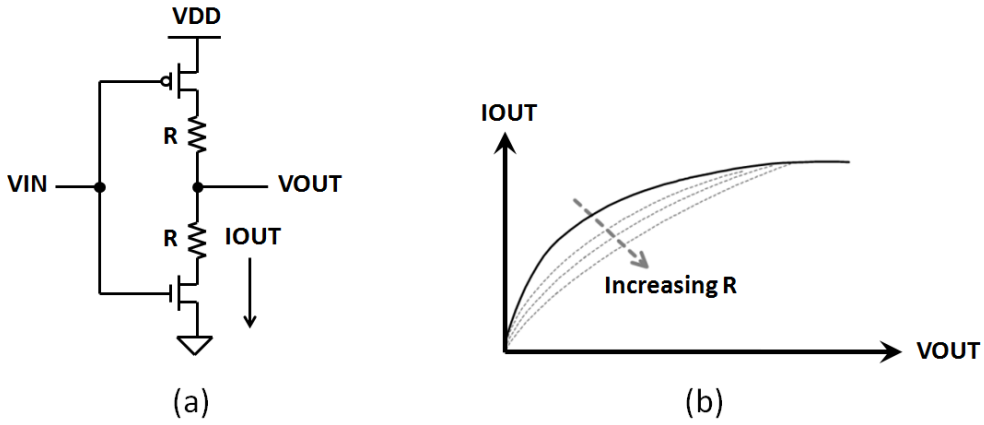


Figure 2.2: (a) SST driver circuit with series resistor in pull-up and pull-down segment. (b) I-V characteristic of SST driver improved by increasing series resistance R.

2.1.2 Current-Mode Driver

A differential current-mode driver connected with far-end resistive terminators is demonstrated in Figure 2.3. Since the impedance of tail current source is very large as compared to terminator R, the output impedance looking into VOUT and VOUTB is always can be approximated to R (Dally and Poulton, 1998; Li, Kwasnieski, Wang and Tao, 2005). The driver uses complementary inputs, V_{IN} and V_{INB} to ensure only one side of the differential pair in the driver is conducting at any given time. Therefore, from Figure 2.3, the differential inputs can control the current flow from tail current

source I_T to the desired side of the driver. For instance, when VIN is low and VINB is high, the tail current I_T is flowing from current source through switch M1 to both the near-end and far-end termination resistor R, creating a voltage VOUT = $\frac{1}{2}$ I_T R. The other side has no current flow since M2 is OFF and the output voltage VOUTB is equal to zero.

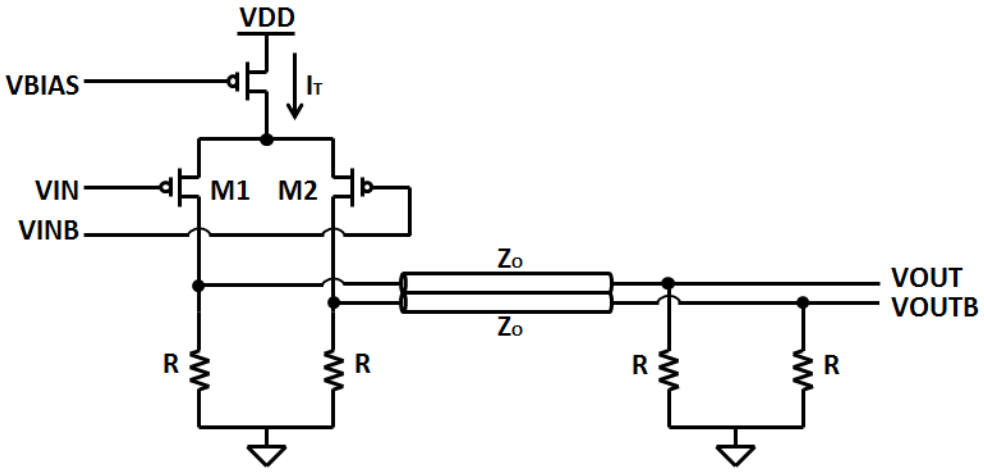


Figure 2.3: Differential current-mode driver with terminators at receiving-end.

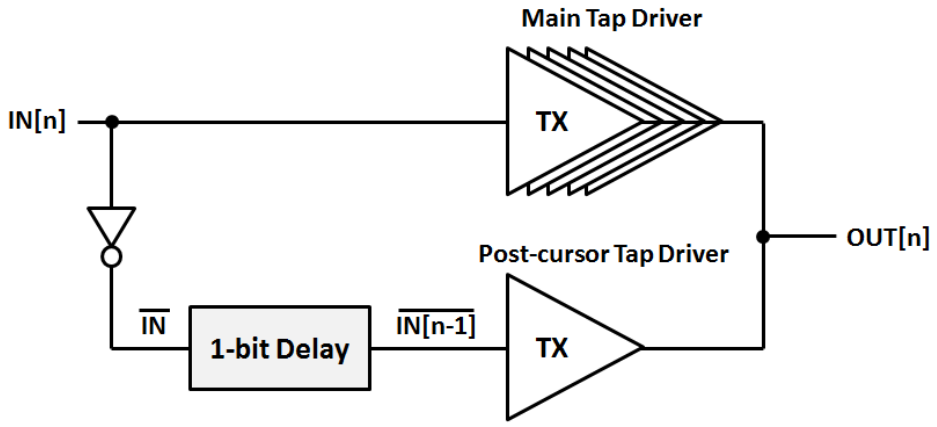
2.2 Equalization Techniques

Equalization techniques have been commonly used to reduce ISI-induced signal level loss and timing jitter by compensating frequency-dependent attenuation at high frequency (Liu and Lin, 2004). Equalization circuits are usually integrated with driver circuits or receiver circuits to reduce system cost. Thus, there are two types of equalization, i.e. receiver equalization and driver equalization (or driver de-emphasis) to compensate or equalize the high-frequency attenuations in a transmission channel. However, driver equalization is commonly done in communication systems due to the ease of circuit implementation. This is because equalization at driver allows the use of

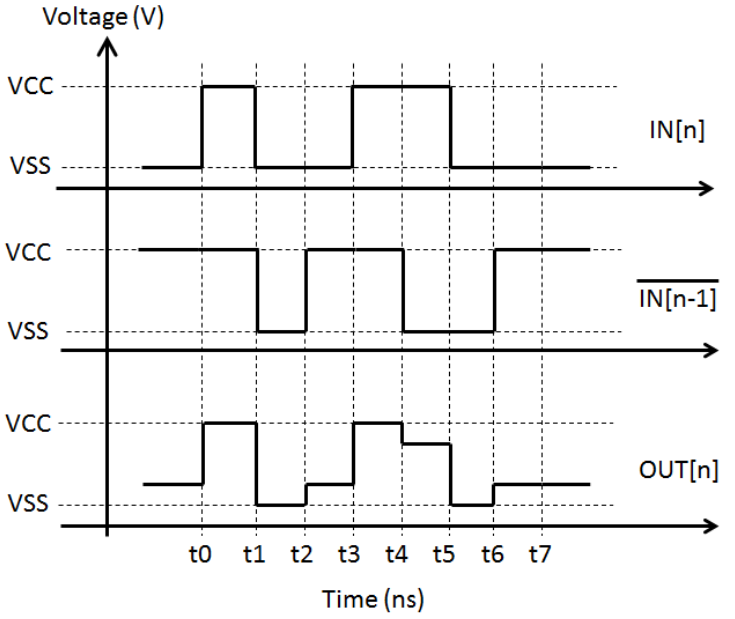
simple receiver, but equalization at receiver would require a high performance analog-to-digital converter (ADC) with high resolution which creates challenges in design and implementation (Dally and Poulton, 1998). Furthermore, de-emphasis technique in driver circuit is to de-emphasize the amplitude of low frequency components in the transmitted signal to equalize the attenuations of lossy channel on high frequency components. Driver equalization can be applied into two types of driver namely voltage-mode and current-mode driver that will be discussed in the following sub-sections.

2.2.1 Voltage-mode Driver De-emphasis

A basic voltage-mode de-emphasis structure is shown in Figure 2.4 (a). It consists of main tap driver and post-cursor tap driver. Both drivers can be constructed from an identical TX instance, with main tap driver has higher weightage as compared to post-cursor tap driver (Heidar et al., 2007; Kudoh, Fukaishi and Mizuno, 2003). For instance, in Figure 2.4 (a), main tap driver is constructed using five TX instance while post-cursor tap driver is constructed using one TX instance only. Thus, the output impedance of main tap driver is five times smaller than that in post-cursor tap driver. As both the output of main tap and post-cursor tap driver are connected together, the output OUT[n] is depending on the combination ratio of the two output impedances. Moreover, the input IN[n] is connected to main tap driver, while the inverted one bit delayed data $\overline{\mathrm{IN}[\mathrm{n}-1]}$ is connected to post-cursor tap driver.



(a)



(b)

Figure 2.4: (a) Basic de-emphasis structure constructed with main tap driver and post-cursor tap driver, (b) Timing diagram for de-emphasis operation .

Operations of de-emphasis can be illustrated in Figure 2.4 (b). When there is a transition in IN[n] from VSS to VCC at time = t0 and the $\overline{IN[n-1]}$ = VCC due to inverted one bit delayed from IN[n], both the main tap driver and post-cursor tap driver

transmit same data, resulting in full voltage swing to VCC. At time = t2, there is repeated bit (no transition) in IN[n] = VSS and $\overline{IN[n-1]}$ = VCC, the main tap driver should pull-down the OUT[n] to VSS while post-cursor tap driver should pull OUT[n] up to VCC. However, due to the fact that main tap driver has smaller output impedance resulted by five TX instance in parallel, the OUT[n] will be slightly higher than VSS, thereby reducing output swing to achieve de-emphasis on the output signal.

Besides, Zhang et al. (2007) proposed a voltage-mode de-emphasis driver to de-emphasize the low frequency signal components. This driver can reduce signal swing and ISI impacts, thereby improving both the power consumption and bandwidth of transmission line. As shown in Figure 2.5, this approach comprises of one-tap FIR filter with delay cell and one DAC implemented by one un-attenuated driver (P1 / N1) and one attenuated driver (P2 / N2). FIR filter checks the current and previous data to determine when to turn-on the un-attenuated driver in DAC. The attenuated driver is always turned-on with its output swing between Vpre and Gpre. If there is a transition, the tri-state un-attenuated driver is turned-on and provides full signal swing at node Dout. Otherwise, the output swing is limited at Vpre and Gpre to provide de-emphasis on low frequency signal components. However, the output impedance of this driver is not constant because the tri-state un-attenuated driver is only activated when there is transition and the mismatch between the output impedance and transmission line impedance can cause signal reflection problem.

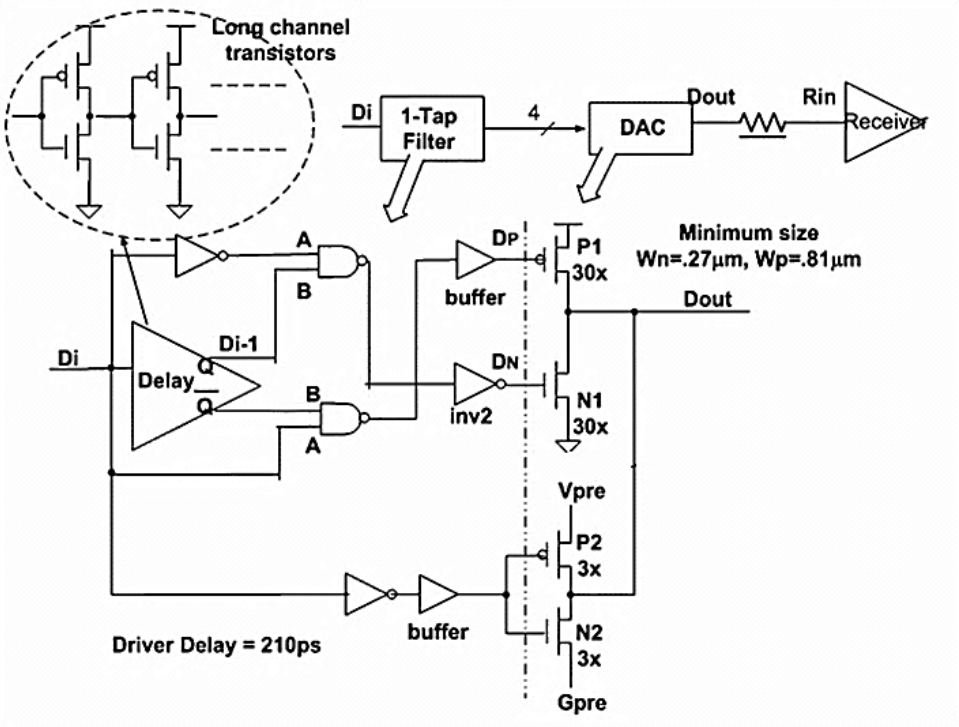


Figure 2.5: Voltage-mode driver de-emphasis circuit (Zhang et al., 2007).

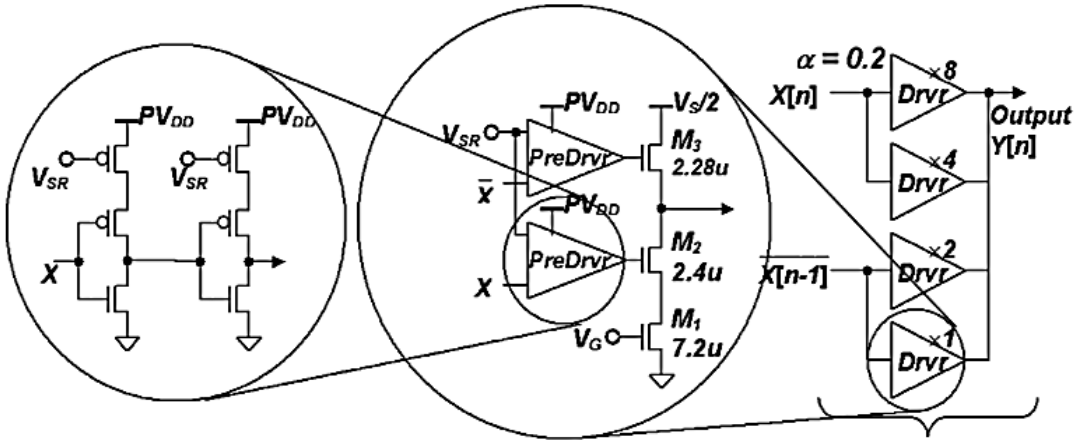
Therefore, to avoid output impedance mismatch; Wong, Hatamkhani, Mansuri and Yang (2004) introduced a two-tap de-emphasis voltage-mode driver with the output impedance matched to transmission line impedance, as shown in Figure 2.6 (a). The two-tap de-emphasis driver is implemented as a high-pass filter with the function below:

$$Y[n] = X[n] - \alpha X[n-1] \tag{2.1}$$

where Y[n] is output of driver, X[n] is input data of driver, X[n-1] is one-bit delayed-input data and α is de-emphasis ratio.

In this architecture, the de-emphasis driver is decomposed into four binary-weighted segments to drive an analog output Y[n] specified by equation (2.1). Depending on the digital input data, the output driver in each segment either pulls up or

down and thus, forming 16 possible outputs with 16 combination of pull-up and pull-down impedance. The advantage of this architecture is the driver achieves de-emphasis and maintains output impedance matching simultaneously with impedance control circuit in Figure 2.6 (b). This is because all segments are in parallel resulting in constant 50 Ω output impedance regardless of the de-emphasis ratio. In addition, this driver has slew rate control using pre-driver shown in Figure 2.6 (c) to improve timing performance. However, this driver has a fixed de-emphasis ratio which cannot precisely compensate the transmission losses if there are variations in transmission line fabrication. The effectiveness of driver de-emphasis can be improved by adjusting suitable de-emphasis ratio to compensate transmission losses. This can be achieved by current-mode driver since the de-emphasis ratio can be easily adjusted by controlling the biasing voltage of current sources.



(c) (b) (a)

Figure 2.6: (a) Voltage-mode driver with two-tap de-emphasis filter,

(b) Impedance control circuit, (c) Slew rate control circuit (Wong et al., 2004).

2.2.2 Current-mode Driver De-emphasis

Li et al. (2005) proposed a driver with multi-tap FIR (Finite Impulse Response) de-emphasis using CML (Current-mode Logic) driver. The driver is implemented using 5-tap FIR with the tap coefficients controlled by independent current sources. Figure 2.7 shows the 5-tap FIR pre-emphasis driver with two 50 Ω termination resistor. Due to the large impedance of current source, the output impedance is always be approximated to 50 Ω termination resistor regardless of the number of taps used. This good feature allows the use of multiple-tap to increase the effectiveness of driver pre-emphasis without facing significant output reflection problem. Moreover, the de-emphasis ratio can be easily controlled by adjusting the biasing voltage of current sources.

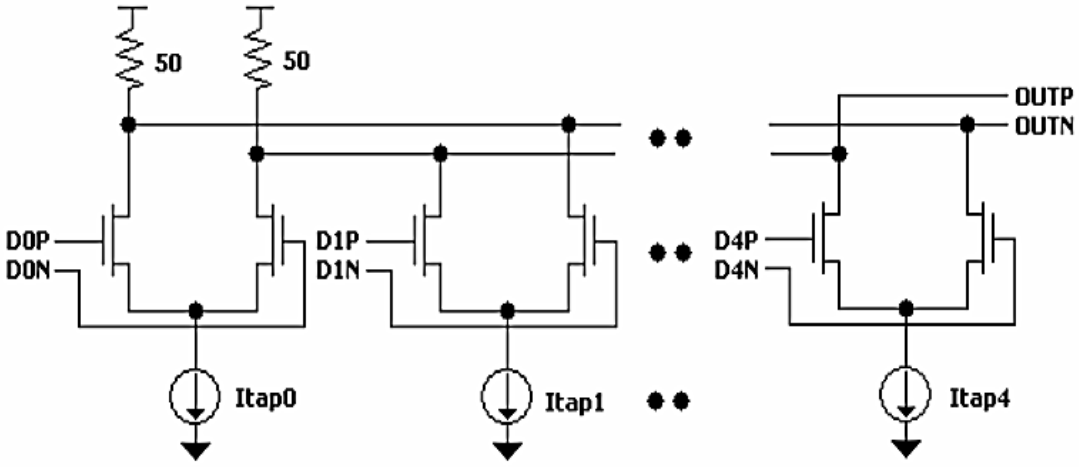


Figure 2.7: 5-tap FIR Current-mode de-emphasis driver (Li et al., 2005).

However, using independent current sources to control the tap weights has caused poor linearity as variations of transistor and channel length modulation effects can be different between current sources. Thus, Higashi et al. (2005) proposed a 5-tap FIR de-emphasis filter that can improve linearity by using a cascaded current mirror

scheme, as demonstrated in Figure 2.8. In this work, the de-emphasis filter provides overall amplitude or total current control using the block B with its gate bias voltage Vb2. Moreover, the ratio of de-emphasis is determined by the weight control through the block A1-A5, where each block consists of a parallel n-channel transistor array with bias voltage Vb1. The de-emphasis ratio is independent of total current from block B and can be controlled by varying the weight control signal in block A to precisely compensate for transmission line losses.

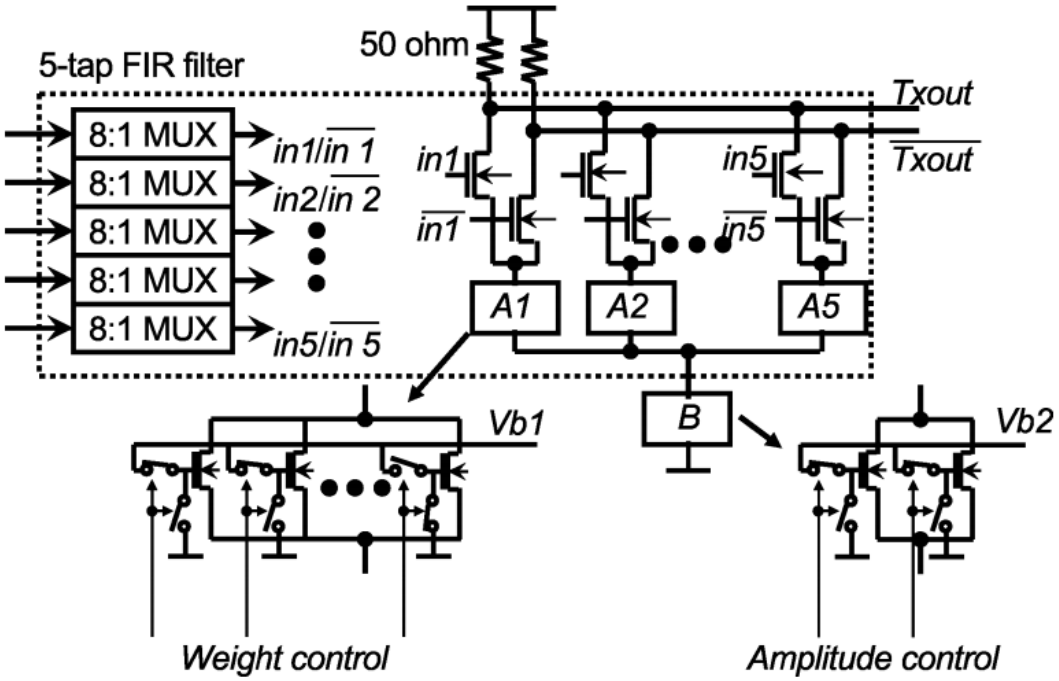


Figure 2.8: The 5-tap FIR Current-mode de-emphasis driver with cascaded current mirror scheme (Higashi et al., 2005).

Although the 5-tap FIR current-mode de-emphasis driver proposed by Higashi et al. (2005) provided good solution for ISI and reflection problem; but, the use of current-mode driver has several drawbacks. Current-mode driver has high static power

consumption due to the employment of current sources. Also, the symmetric error in the current mirror circuit has caused the driver output unable to achieve desired voltage level. Although this problem can be solved by supplying more current in the current mirror, but this solution increases the power consumption. Another solution is to increase the length of current mirror; however, the long channel transistor in current mirror is not area efficient (Heidar et al., 2007). Therefore, current-mode topology is not suitable in some low-power applications; but, it is very suitable in high performance signaling systems due to the flexibility in adjusting de-emphasis ratio in compensating ISI and the ease of output impedance control (output impedance is always be approximated to termination resistor).

2.3 High-voltage Gate-oxide Overstress Protection

As continuous scaling down of semiconductor process and core supply voltage, the device gate-oxide thickness becomes thinner and the core supply voltage has been reduced below 1.0 V to reduce the power consumption. Nevertheless, the on-board supply is still maintained above 1.0 V for applications like DDR2 (1.8 V) and DDR3 (1.5 V) (Ker, Chen and Tsai, 2006). In general, when the operating voltage of a CMOS transistor is higher than its nominal voltage, there are three problems occur. First, high drain-to-source voltage $|V_{DS}|$ can cause hot-electron effect that shortens the device lifespan (Chen, Choi and Hu, 1988). Second, very high drain-to-bulk voltage $|V_{DB}|$ can cause breakdown on the P-N junction between drain and bulk of a device (Scott, Dumin, Hughes, Dumin and Moore, 1996). Lastly, high gate-to-source voltage $|V_{GS}|$ and gate-to-drain voltage $|V_{GD}|$ can cause high-electrical overstress (EOS) across thin gate-oxide