ANALOG DESIGN IMPLEMENTATION OF USB2.0 On-The-Go ATTACH DETECTION PROTOCOL

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2013

ANALOG DESIGN IMPLEMENTATION OF USB2.0 On-The-Go ATTACH DETECTION PROTOCOL

by

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Thesis submitted in fulfillment of the requirements
for the degree of
Master of Science

April 2013

DECLARATION

I hereby declare that this work has been done by myself and no portion of the work contained in this report has been submitted in support of any application for any other degree or qualification of this or any other university or institute of learning.

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ACKNOWLEDGEMENT

Foremost, I would like to express my sincere gratitude to my project supervisor Dr. Arjuna Marzuki for his continuous support, guidance and encouragement throughout my Master study and research. Besides, he has always been generous in sharing his enormous knowledge with me and gave me a clear direction during this period. This research would not have been possible without his constructive suggestion.

I am also thankful for my Intel supervisor, Dr. Su Hsiao Wei for his technical support and guidance, which enable me to overcome most of the obstacles during this Master research project. In addition, I would also like to appreciate his time and patience for sitting down with me weekly in order to bring my technical knowledge up to the standard.

Not to forget Mr. Fong Tark Wooi who has been giving me motivating and inspiring advices which boost my morale in completing this project. Thank you for giving me courage from time to time and changing me into a more confident person.

Last but not least, a very special thanks to my best friend, Miss Foo Hwee Yun for helping me in improving my English language as well as my writing skill. This thesis would not have been possible without her unconditional help. Much appreciated.

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LIST OF ABBREVIATION

ADP	Attach Detection Protocol
CM	Current Mirror
CMOS	Complementary Metal Oxide Semiconductor
CTD	Charging Threshold Detection
EH	Embedded Host
EOS	End of Session
FF	Flip Flop
HIP	Hard Intellectual Property
HNP	Host Negotiation Protocol
HVP	High Voltage Protection
IC	Integrated Circuit
INV	Inverter
KVL	Kirchoff Voltage Law
LC	Logic Control
MCU	Main Controller Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUX	Multiplexer
NMOS	N type Metal Oxide Semiconductor
Op-Amp	Operational Amplifier
OPC	One Pulse Control
OTG	On The Go
PC	Personal Computer
PMOS	P type Metal Oxide Semiconductor
PVT	Process Voltage Temperature
RC	Resistance Capacitance
SC	Sourcing Control
SOC	System on Chip
SRP	Session Request Protocol
USB	Universal Serial Bus

LIST OF SYMBOLS

ΔV	Voltage different
μ_n	Electron mobility
A	Ampere
C	Capacitance
℃	Degree Celsius
C_{OTG}	Capacitance in OTG device
C_{OX}	Oxide capacitance
D-	Data Line -
D+	Data Line +
F	Farad
g_m	Transconductance
GND	Ground reference voltage
I_{ADP_SINK}	ADP sinking current
I_{ADP_SRC}	ADP source current
I_D	Transistor drain current
ID	Identification pin
I_{LKG}	Leakage current
L	Transistor length
Q	Charges
R	Resistance
R_{INT}	Internal resistance
R_{OTG}	Resistance in OTG device
R_{OUT}	Output resistance
τ	Time constant
T_{ADP_DSCHG}	ADP discharging time
T_{ADP_RISE}	ADP charging rise time
V	Voltage
V_{ADP_DSCHG}	ADP discharge voltage
V_{ADP_NOISE}	ADP noise voltage

V_{ADP_PRB}	ADP probe voltage
V_{ADP_SNS}	ADP sense voltage
V_b	Biasing voltage
V_{BUS}	USB bus voltage
V_{CC}	Supply voltage
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
V_{ON}	Transistor turn on voltage
$V_{OTG\_SSEND\_VLD}$	OTG session valid voltage
V_{REF}	Reference Voltage
V_{SRC_CTRL}	Sourcing control voltage
V_{TH}	Threshold voltage
W	Transistor width

PELAKSANAAN REKABENTUK ANALOG UNTUK PROTOKOL PENGESANAN USB2.0 On-The-Go

ABSTRAK

Berikutan teknologi yang canggih, telefon bimbit atau peralatan bimbit pada zaman ini telah disertakan dengan fungsi-fungsi canggih yang mempercepatkan penggunaan kuasa elektrik. Jadi, jangka hayat bateri telah menjadi kebimbangan kepada semua pengguna. Baru-baru ini, banyak usaha telah dibuat bertujuan untuk mengurangkan penggunaan kuasa elektrik serta untuk memanjangkan jangka hayat bateri, "USB 2.0 On-the-Go" merupakan sebahagiannya. Tetapi, selain spesifikasi teknikal, tiada perlaksanaan litar pernah diterbitkan. Tambahan lagi, dengan seni bina yang sedia ada di Intel, terdapatnya limitasi untuk menyokong peralatan yang berkapasitan tinggi. Litar yang baru telah dicadangkan dan direka menggunakan proses teknologi CMOS 45 nm disertai bekalan elektrik 1.8V. Fungsi litar-litar tersebut telah dimodelkan dan simulasi telah dibuat dengan menggunakan SPICE. Analisis telah dibuat dengan mengawasi keputusan simulasi transien disebabkan ADP merupakan perhatian utama dalam aras mengecas voltan. Rekabentuk yang dicadangkan telah disahkan dengan ujian kebolehpercayaan yang merupakan simulasi litar disertai PVT yang berlainan. Syarat PVT adalah dengan ±10% variasi dalam 1.8 V bekalan elektrik tipikal, lingkungan suhu daripada -40℃ hingga ke 110℃ dan 13 proses skews yang berlainan. Litar yang baru dicadangkan telah memenuhi fungsi-fungsi serta baik dalam variasi PVT yang telah disebutkan. Dengan variasi yang amat besar ini, bekalan arus masih dapat mengecapi spesifikasi yang diberikan, iaitu dari 1.1 mA hingga 1.65 mA. Jadi, hal ini dapat diputuskan bahawa rekabentuk litar ADP dapat memenuhi keperluan fungsi dan kebolehpercayaan.

ANALOG DESIGN IMPLEMENTATION OF USB2.0 On-The-Go

ATTACH DETECTION PROTOCOL

ABSTRACT

As the technology advancement, mobile phone or hand-held devices nowadays are equipped with extra features which accelerate the power consumption. Hence, battery life span is becoming a huge concern to all consumers. Recently, many efforts have been made to reduce power consumption as well as increase battery life span, USB2.0 On-the-Go is part of them. However, besides technical specification, there is no circuit implementation being published to date. Furthermore, with current architecture available in Intel, it has limitation on supporting high capacitance devices such as, Embedded Host. To solve the above problem, new circuitries is being proposed and designed under 45 nm CMOS process technology with 1.8 V standard power supply. The functionality of the circuits are being modeled and simulated by using SPICE simulator. Analysis are done by observing the transient simulation result as the ADP is more concerned on the charging voltage level and charging time. The proposed design is further verified by reliability test which simulates the circuit with PVT variations. The PVT conditions are ±10% variation on 1.8 V typical power supply, temperature ranges from -40℃ to 110℃ and 13 different process skews. It can be observed that the new proposed circuitries met the functionality which is described by the USB organization. Besides, the performance of the proposed circuitry is reasonably good under the above PVT variation. With such a huge PVT variation, current source is still able to meet the specification given, which is 1.1 mA to 1.65 mA. Hence, it can be concluded that the proposed design of ADP front-end circuitry met both functionality and reliability requirements.

CHAPTER 1
INTRODUCTION

1.1 Motivation

Over the past decades, demand and usage of mobile devices have been increasing dramatically. More features have been added into mobile devices to capture market share in such a highly competitive market. One of the features is USB2.0 OTG. As mobile devices comprise such a huge usage, the needs of communication between two devices hence increase. In a typical USB architecture, two slave devices are not able to communicate in the absence of host, for instance, a computer. However, with the implementation of USB2.0 OTG, two peripherals or slaves devices can be connected for communication or data transfer by using USB protocol without connecting to the host.

The Attach Detection Protocol (ADP) is introduced in USB2.0 OTG Specification Rev2.0 to detect the attachment of two peripheral devices in the absence of voltage supply, V_{BUS}. The entire concept behind this ADP is to capture the attachment of an external device by constantly measuring capacitance of the V_{BUS} line with minimum current. It turns off all unnecessary clocks associated to the USB, and even the entire USB system when there is no device attached. This is to prevent the battery from significantly draining out and avoid frequent recharging of the user's mobile device.

USB 2.0 On-The-Go Supplement (USB Implementer Forum Inc., 2010) provides important specification data for designing the ADP system; however, to the author's knowledge, other than the specification, there is no published information on how the circuit can be designed and implemented. The main goal of this research is to design the

analog front-end circuitry of ADP system with PVT variation tolerant. This research is also a collaboration project between Universiti Sains Malaysia and Intel Malaysia in order to have a better circuit development on the ADP system as well as to benefit the analog IC design sector/industry.

1.2 Problem Statements

Intel Malaysia Hard Intellectual Property (HIP) Department has some private and confidential documents that describe the implementation of the analog front-end ADP circuitry. However, it comes with limitations. The architecture proposed by Intel HIP does not support high capacitance USB application such as Embedded Host which has an input capacitance of 120 µF. Embedded Host or so called the "limited host" is usually the portable device which carries limited host capability to support certain peripherals with minimum sourcing current of 8 mA (EET Asia, 2008).

According to Sen and Chatterjee (2008), variation of process parameters is becoming increasingly serious with the aggressive scaling of technology node especially in the nanometer regime. Furthermore, the channel length of a transistor is at the sub-wavelength of light and sub-wavelength lithography will worsen the variation. Besides, it is tougher to control the 3σ variation of the process parameters within 10% (Borkar, Karnik & De, 2004). Other than that, variation on voltage and temperature always challenges the reliability of a circuit. Thus, variability of PVT in nanometer regime is a huge concern as it directly impacts the circuit's reliability and hence the manufacturing yields.

1.3 Research Objectives

The main objective of this research is to design an analog front-end ADP circuitry which can supports across various USB applications or appliances. On the other hand, the implementation idea from Intel HIP is only drafted in block diagram and this leads to difficulties in bench marking. Thus, each of the blocks will be re-modeled and simulated in order to compare and bench marking with the proposed design.

The second objective is to design an analog front-end ADP circuitry which can tolerate the PVT variations. With the aim of creating an Integrated Circuitry (IC) with well functional features and good reliability, PVT variation consideration is definitely is a must. On top of achieving the functionality given, this research also put a lot of efforts in getting the proposed design free of PVT variation to make sure that it will work well in all covered corners. The proposed design will be simulated across 13 different process corners, e.g. tttt, rsss, rfff, ssss, ffff, ffsf, fsff, rsfs, rssf, rffs, rfsf, rfffaf, rsssas; with temperature varies from -40℃ to 110℃ and voltage supply ranging from 1.69 to 1.98 V; ±10% variation from the typical supply of 1.8 V.

Last but not least, this research also aims to give readers from semiconductor industry a better understanding on the mechanism and how this system can be designed successfully with the current 45 nm CMOS technology. It is believed that this proposed solution will bring significant help to engineers and circuit designers to shorten product development cycle and to reduce the exposure to any potential risks and design issues.

1.4 Scope of Research

The circuit design simulation in this study is based on 45 nm CMOS process technology with 1.8V standard power supply. The PVT variations are ±10% of 1.8 V supply voltage, temperature ranges from -40℃ to 110℃, four different functional skews, namely ssss, ffff, ffsf, fsff, and nine different performance skews which are tttt, rsss, rfff, , rsfs, rssf, rffs, rfsf, rfffaf, rsssas. Besides, this research will be more focusing on the portion of analog front-end interfacing circuitry. However, some digital block like ADP probing control, trigger threshold and ADP monitoring control will also be created to validate the entire function. Last but not least, the application for the proposed design is mainly for USB2.0 OTG system.

1.5 Thesis Organization

This thesis has a total of six chapters. Chapter 1 covers mostly introduction, research motivation, problem statement, research objectives and scope of work. Background studies, basic operation of the ADP system and the potential issue with the current system will be discussed in Chapter 2. It is followed by the design methodology and theories, which would be discussed in Chapter 3. Chapter 4 shows all the modeling works, including modeling of the potential issues as well as the proposed solution by using HSPICE and PSPICE. Chapter 5 collects and tabulates all the physical simulation results for the proposed design. Lastly, Chapter 6 covers the conclusion as well as some future work to be done from this point.

CHAPTER 2
LITERATURE REVIEW

2.1 Background of USB 2.0 On-The-Go (OTG)

Universal Serial Bus, also known as USB, was invented in 1996. Originally it was one of those interfaces designed to connect the Personal Computer (PC) to peripherals. Nowadays, it has become a popular general-purpose PC interface and is widely used in all electronics devices. The original USB architecture consists of one host and one or more peripherals. The concept is to make the heavy loads process on the host and the peripherals to manage the simple one. It is because in the past, the role between host and peripherals are pretty clear cut; host owns powerful processing ability while peripherals are the devices to support external or additional functionality. In addition, there are few criteria to define a host (USB Implementer Forum Inc., 2010):

1. Able to supply 0.5 A at the voltage of approximate 5 V.
2. Able to support all the data transfer speed.
3. Able to support all the data flow type, e.g. isochronous, bulk, interrupt and etc.

As the technology advances, peripherals devices have become more powerful, especially for hand-held device. They have built-in processors, which manage to supply power and possess the host capability. Thus, this blurred the cutting edge between PC and peripherals. In addition, many peripherals nowadays are required to communicate or connect with other peripherals, for instance, connecting a camera to a printer; or connecting a smart phone to a Bluetooth headset. Hence, the USB organization has overcome this issue by adding the host capability to the peripherals.

In the past, when PC was used as a host, all peripherals also have to connect through the PC for host-peripheral and peripheral-peripheral communication. However, the peripheral devices that are given the host capability nowadays do not required to connect to other devices. It has its own targeted peripherals to be connected and this host is named as Targeted Host. There are two categories of Targeted Hosts; one of them is Embedded Host which provides one or more Standard-A receptacles. It will also have Standard-B receptacles if it supports peripheral capabilities. Another one is On-The-Go (OTG). OTG devices only uses single micro-AB receptacle to operate as a Targeted Host, or as a USB peripheral. In short, OTG enables point-to-point connection of two peripherals by adding host functions to one of them. It allows two devices to talk to each other without the presence of PC (Maxim, 2002).

Assume that there are two OTG peripherals devices connecting each other with a USB cable (having micro-A and micro-B plug at the respective end). By following the OTG architecture, the device with the micro-A plug will firstly be defined as the OTG-A device or namely Targeted Host and it is responsible to supply power. The other one will be the peripheral device. The role of host and peripheral are interchangeable using the Host Negotiation Protocol (HNP).

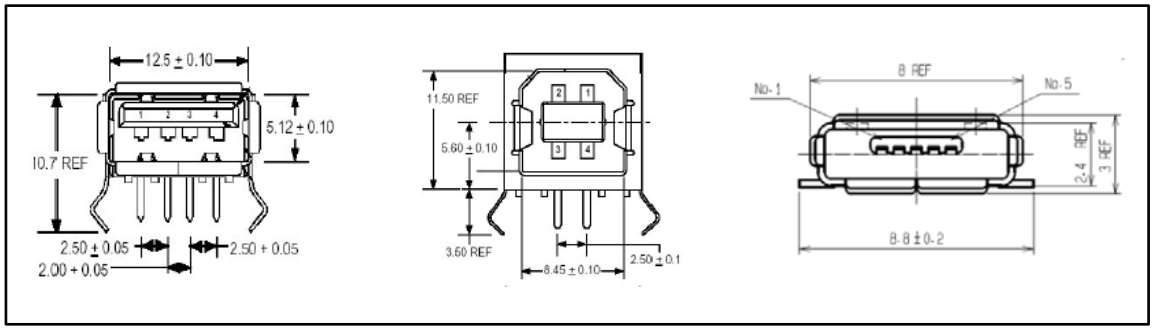

Figure 2.1 : From the left to the right are Standard-A Receptacle, Standard-B Receptacle, and Micro-AB Receptacle (Guo Yang Bin, n.d.)

The micro-A and micro-B plug is different from the Standard-A and Standard-B by 1 ID pin. The Standard-A/B plug contains 4 pins, which are VCC, GND, D+ and D-while the micro-A/B plug has additional an ID pin which is used to differentiate micro-A and micro-B plug. As shown in Figure 2.2, in micro-A plug, the ID is tied to the 0 V, GND and micro-B is left floating. As mentioned above, OTG-A device is responsible to power OTG-B device; hence, the purpose of this is to get the OTG-A device assigned as the power supplier from the connector once is being attached.

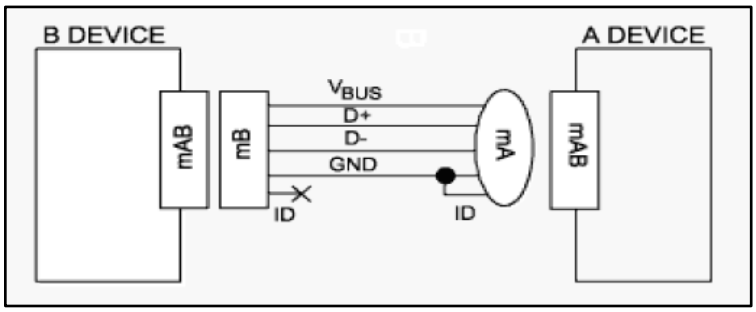

Figure 2.2 : Illustration of the ID Pin in Micro-A and Micro-B plug

In terms of powering the USB port, OTG is different from the traditional USB architecture which has a wall-powered USB port and consistently supply power to the downstream. As OTG devices are non-PC and mostly hand-held devices, battery life time is a premium. OTG devices do not afford to have a wall-powered USB port, thus it has three important protocols to govern the power supply as well as to ensure smooth connection for any scenarios. The three protocols are:

1. Session Request Protocol (SRP)
2. Host Negotiation Protocol (HNP)
3. Attach Detection Protocol (ADP)

Firstly, the Session Request Protocol (SRP) is used to "waken" the OTG-A device from the "sleep" mode. By default, when two OTG devices connect to each other with a USB cable, the OTG-A device will automatically start powering the OTG-B device. However, when there is no data activity or in the case that OTG-A device detects an "End of Session", it will stop the power supply and switch to sleep mode even with the cable attached. "Session" here simply means that the V_{BUS} line is powered in a period of time. Hence, if there is any activity from the OTG-B device which requires OTG-A device to re-provide the power supply, the SRP will take its role to "waken" the OTG-A device.

The second is the Host Negotiation Protocol (HNP), an OTG dual-role device which can function as both host and peripheral. When two OTG devices talk to each other, the role of host might be interchanged based on application needs or due to the wrong physical connection. The HNP here provides user with an easy solution by changing the role internally without bothering user to adjust the physical cable. However, even with the conveniences of interchangeable role, the powering devices always follow the micro-A plug. In other words, OTG-A device will always be the power provider despite being a host or a peripheral.

The third protocol, Attach Detection Protocol (ADP) has been introduced by USB organization in the year of 2010. This protocol allows a local device to detect attachment and detachment of a remote device with a minimum consumption of currents. ADP plays an important role in the USB system to conserve the battery life time with its ability to turn off power line, clocks, PLL even entire USB transceiver when there is no attachment of peripheral. Data gets transfer only when there is a connection with other device.

2.2 The Operation of Attach Detection Protocol (ADP)

The Attach Detection Protocol (ADP) architecture can be divided into two major parts, namely ADP Probing and ADP Sensing. In ADP Probing, the circuit is in charge of detecting the attached devices by checking the V_{BUS} capacitance value; whereas in ADP Sensing it senses the ADP probing activities on V_{BUS}. This is to make sure that the connections between two devices are still available after the "End of Session (EOS)".

ADP probing activity is not necessarily to be done by the host or OTG-A device. Both OTG-A and OTG-B devices can perform ADP probing activity as long as both are "local device". A local device is defined as an USB OTG ADP-enabled device. In order to enable local device to consistently detect remote device using ADP probing, it must have the following (USB Implementer Forum Inc., 2010):

1. Local device resistance of R_{OTG_VBUS}
2. Local device capacitance of C_{ADP_VBUS}
3. Local device noise of V_{ADP_NOISE}
4. Local device leakage of $I_{VBUS\_LKG\_SRC}$

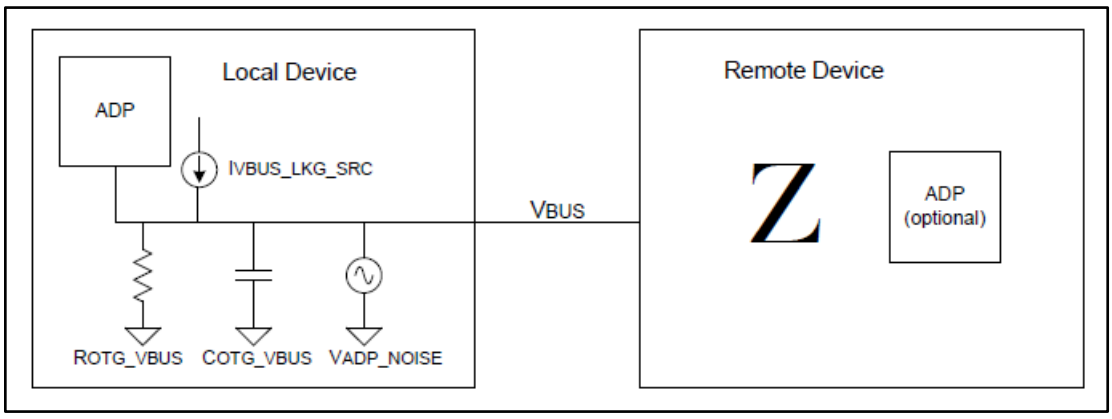

Figure 2.3 : Relationship between Local Device and Remote Device (USB Implementer Forum, 2010)

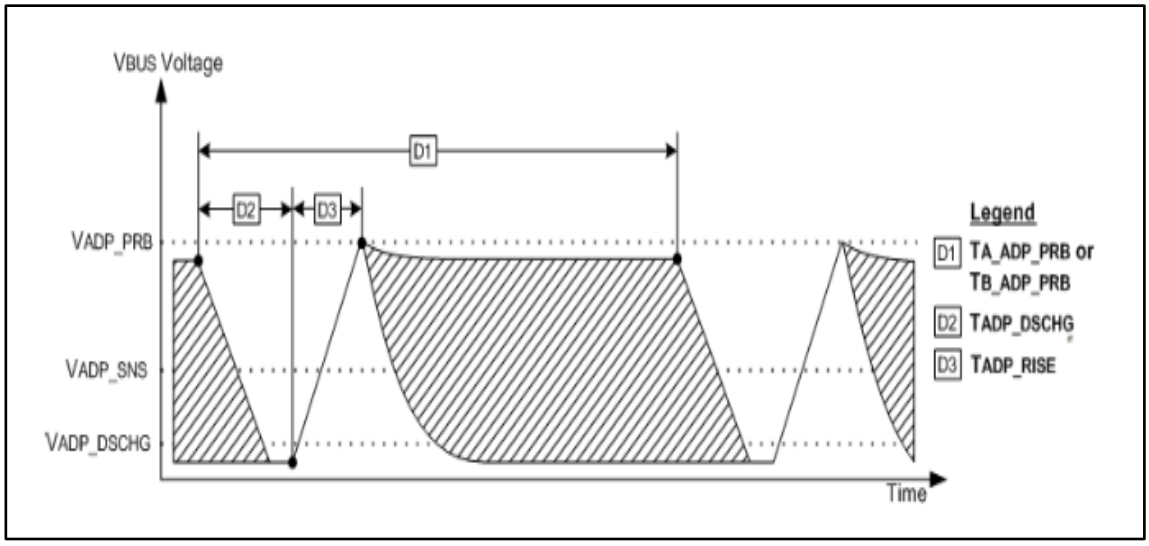

Figure 2.4 : Timing Diagram of ADP Probing Cycle (USB Implementer Forum, 2010)

Figure 2.4 shows the timing diagram of the ADP probing cycle. To measure the capacitance on the V_{BUS} line, the local devices will firstly discharge the V_{BUS} from V_{ADP_PRB} to V_{ADP_DSCHG} by turning on the current sink (I_{ADP_SINK}) for a fixed duration (T_{ADP_DSCHG}). This will ascertain the V_{BUS} line to fully discharge to V_{ADP_DSCHG} with all the combination of resistance, capacitance and leakage currents. Once the V_{BUS} line discharge below the V_{ADP_DSCHG}, the current sink (I_{ADP_SINK}) will be turned off followed by turning on the current source (I_{ADP_SRC}). I_{ADP_SRC} is responsible for charging of the V_{BUS} from V_{ADP_DSCHG} back to V_{ADP_PRB}.

Next, the rise time of V_{BUS} (T_{ADP_RISE}) will be measured. The measured rise time of V_{BUS} will be stored for reference. When a remote device is attached to a local device, the capacitance of the V_{BUS} line will be charged and hence the rise time of V_{BUS} (T_{ADP_RISE}). Thus by checking the T_{ADP_RISE}, the attachment status for two peripheral can be determined (USB Implementer Forum Inc., 2010).

When the V_{BUS} line goes below $V_{OTG\_SSEND\_VLD}$ min for a certain time, it can be either the EOS of the previous activity, or both devices get disconnected from each other. Hence, here comes in ADP Sensing to identify the connection. The ADP Sensing will need to detect two ADP Probing cycles from the host to make sure the host is still attached; otherwise it will detect it as a disconnection and the peripherals will start its own ADP Probing cycle.

2.3 Hardware Architecture of Attach Detection Protocol (ADP)

Figure 2.5 shows the block diagram of the ADP architecture which is taken from the USB 2.0 OTG Specification Revision 2.0 (USB Implementer Forum Inc., 2010). From this ADP architecture, simply it can be divided into two sections - analog front-end interfacing circuitry and digital back-end processing circuitry. The analog front-end interfacing circuitry is a piece of circuit that sits at the outer part of the Integrated Circuit (IC) and is used to connect the external world. It deals with the entire analog signals from the external, e.g. cable, power line and responsible to convert it into some meaningful digital data for the latter. The suggested circuitry consists of a current source and current sink for charging the V_{BUS} power line, and detection circuitry for ADP Probing and ADP Sensing.

On the other hand, the digital back-end processing circuitry which contains *ADP Probing Control*, *Time Interval Measurement*, *Trigger Threshold* and *ADP Monitoring Control* are mainly used to process received data and control ADP mechanism. Status and control signal will also be sent to the main controller for further action.

This research will be focusing on designing solutions to the existing problems and discussion of analog front-end interfacing circuitry. Some of the digital blocks like ADP Probing Control and ADP Monitoring Control will also be created to support and validate the function of proposed analog front-end circuitry.

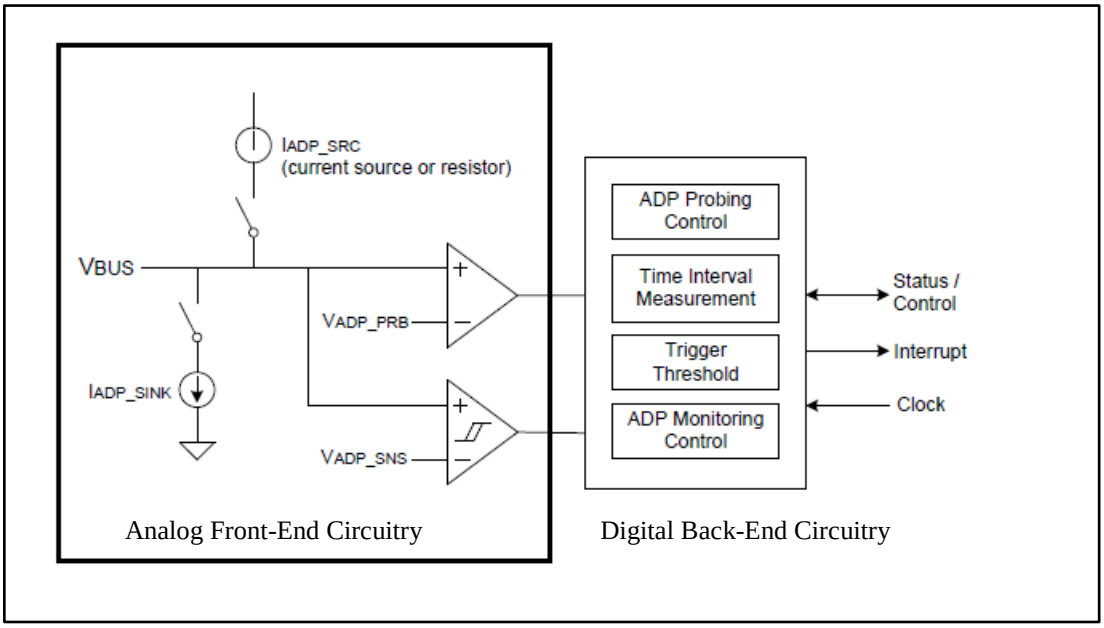

Figure 2.5 : Architecture of Attach Detection Protocol (ADP) (USB Implementer Forum, 2010)

2.4 Intel ADP Architecture for Analog Front-End Interfacing

Figure 2.6 shows Intel's concept of ADP architecture for analog front-end circuitry. The vertical rectangle on the left represents a local device in which its ADP circuitry is not able to tolerate any high voltage supply, 5 V; whereas the horizontal rectangular on the right illustrate a 5V-tolerant remote device. As shown in the block diagram, the suggested circuitry has similar essential blocks as the circuitry shown earlier on. However this newly suggested circuitry by Intel uses voltage source instead of current source. It is because voltage sources are well ready in the System-On-Chip (SOC) without the need of creating extra circuitries. Besides that, some additional switches are also added together with the local device. Its main purpose is to protect the non-5V tolerant ADP circuitry by creating some delays and avoid ADP circuitry to expose to the external while power line still remains in high voltage.

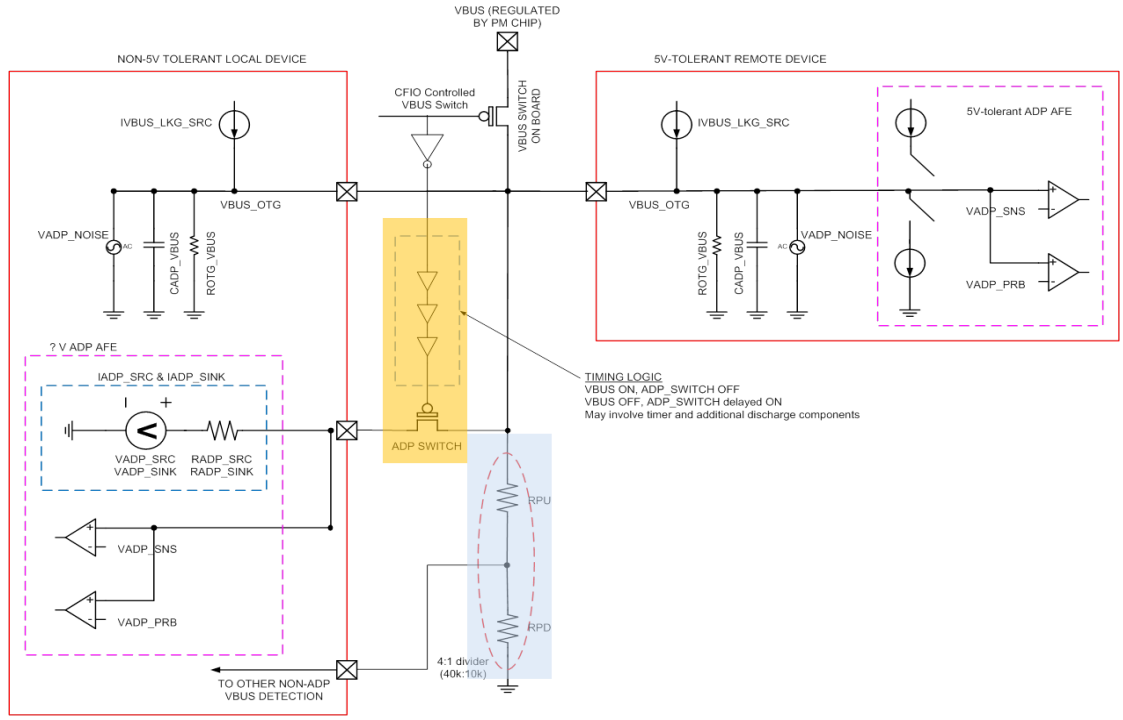

Figure 2.6 : Intel's Concept of ADP Architecture for Analog Front-End Circuitry (Intel Corp., 2011)

2.5 Background on RC Timing and Research Purpose

The Intel 1st revision ADP circuitry mentioned in Section 2.4 uses voltage source for V_{BUS} line charging. Even though it is the simplest way as it can be taken from any on-chip power source, there are some drawbacks of using voltage source compared to current source. One of the disadvantages is that it has a slower charging time. As the charging voltage approaches the voltage source, charges will transfer slower due to decrease in currents and hence contributes some delay to the total charging time. Figure 2.7 is a simple electronics circuit which demonstrates a capacitor charging by a voltage source. Figure 2.8 shows the charging transient response of a capacitor with respect to time.

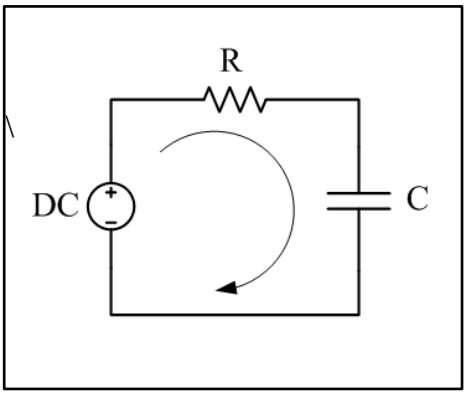

Figure 2.7 : Charging a Capacitor with Voltage Source

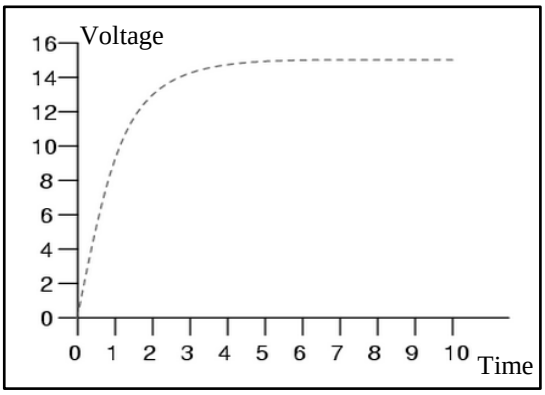

Figure 2.8 : Capacitor Transient Response

From the circuit diagram which is shown in Figure 2.7, a Kirchhoff's voltage law equation can be derived as:

$$-V_{DC} + iR + V_C = 0 \tag{2.1}$$

$$V_{DC} = iR + V_C \tag{2.2}$$

The total number of charge which a capacitor can store is equivalent to the capacitance of a capacitor multiply with the voltage applied. It can be written as:

$$Q = C\,V \tag{2.3}$$

$$V = \frac{Q}{C} \tag{2.4}$$

Substituting (2.4) into (2.2) producing (2.5):

$$V_{DC} = iR + \frac{Q}{C} \tag{2.5}$$

According to (2.5), as charging process continues, capacitor slowly gets charged up with the increasing value of Q. V_{DC} is a voltage source which will stay constant, and R is the internal resistance, will also be a constant. In order to balance the equation, the currents '*i*' has to be reduced. From (2.6), reducing the currents means reducing the number of charge transfer per time period, hence slower the charging time.

$$Q = It \tag{2.6}$$

(2.8) can be obtained by rewriting the (2.2):

$$V_{DC} - V_C = iR \tag{2.7}$$

$$\Delta V = iR \tag{2.8}$$

Furthermore, it can be looked at a different way given that the current '*i*' is directly proportional to the voltage difference between the source and charging capacitor. As capacitor gets charged up, the voltage different, ΔV, reduced and hence the charging current.

As a result, by using a current source, it will contribute to improve the charging time. It is due to the reason that, as mentioned previously, the current is directly proportional to the number of charges which get transferred into a capacitor. With a stable current source, currents manage to flow constantly without being affected by the changing voltage of a capacitor, thus the charging time will not get any delay.

On the other hand, there are some challenges in using a current source. The biggest challenge is to design a current source which is able to supply a constant current without affected by the surroundings or other factors. Designing a stable current source will be taken care in this research.

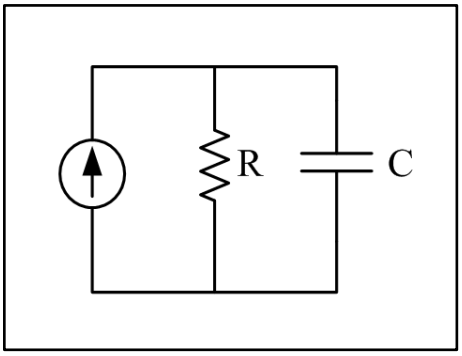

Figure 2.9 : Charging a Capacitor with Current Source

Another issue which can be seen from the Intel 1st revision design is the current mechanism does not support a wide range of USB application. The original purposes of ADP switch which is added off chip are to prevent external high voltage from entering the non-5V tolerant chip. The switch will only turn on when the V_{BUS} line voltage falls at the safety level. However, there is no mechanism in the ADP circuitry or on the board which allow the high voltage to be sunk. It is fully dependent on the natural discharge. One big issue with natural discharge is that the discharging rate is fully dependent on the

total RC value of the V_{BUS} line. (2.9) shows that time constant, τ, is multiplication of the resistance, R and capacitance, C. In the scenario of connecting two devices using a USB cable, resistance R will be the termination resistance which follows standards and has a constant value, while capacitance, C will depend on the type of USB devices. In this case, Intel 1st revision of ADP circuitry design will not be able to function normally if the local device attached to an Embedded Host. According to the specification (USB Implementer Forum Inc., 2010), an Embedded Host is having an internal capacitance of 120µF. With this large contribution of capacitance and the time constant, the natural discharge rate will be huge and the time used for discharging will exceed the specification given. Details modeling data will be presented in next chapter.

$$\tau = R\,C \tag{2.9}$$

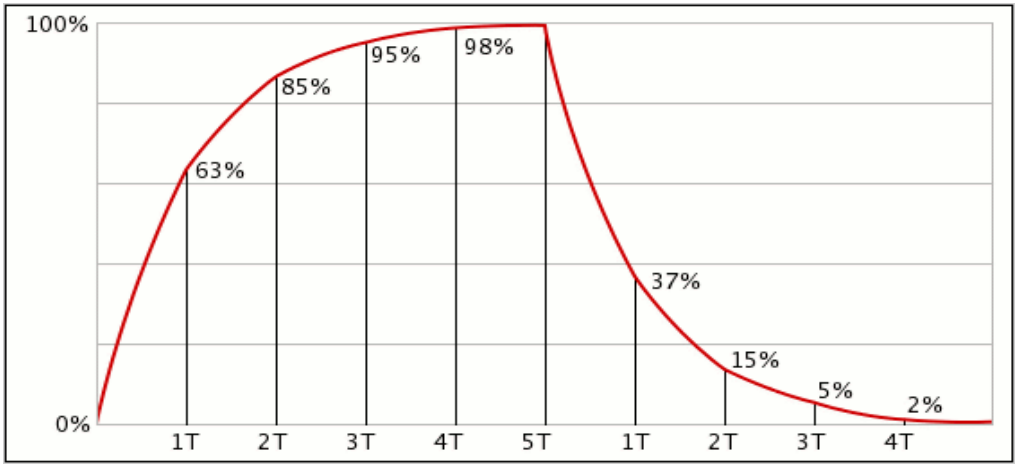

Figure 2.10 : Capacitor Charging Voltage versus the Time Constant (Donaldson, 2007)

In addition, no detection circuitry is used to ensure the external voltage level fall into the safety region. From Figure 2.6, it shows that only some buffers are added to prolong the time before turning on the ADP switches. Since the numbers of delay buffer is fixed, this will bring risk to the ADP circuitry when it is connected to a high capacitance device, e.g. Embedded Host. The long natural discharging time will destroy the ADP circuit, as the switches will be turned on before the V_{BUS} line is fully discharged.

As a result, one of the main objective of this research is to design an ADP analog front-end circuitry which can resolve the issues above as well as to support wide range of USB application, e.g Embedded Host. However, to this point, the issues and circuitries which have been discussed are purely conceptual, e.g. in block diagram and it is not in the transistors level. Besides, to the author's knowledge, there is no related information on transistors level implementation shared or published. Thus, the second objective is to design and develop the entire analog front-end ADP circuitry in the transistors level. This can benefit readers by shorten the development time and then help in the product cycle.

As technology advances, transistor is getting smaller. Small transistor which is in nanometer ranges behaves differently compare to the past. Small size transistor is more sensitive to all the surrounding changes like, Process, Voltage and Temperature (PVT). Hence, simply making the ADP circuitry functioning is no good enough; it must also be good in term of reliability. The third research purpose is to design the ADP circuitry in 45nm Intel's process technology as well as to ensure the proposed design can be functioning well across the all PVT variations.

2.6 Summary

In Chapter 2, operation of the ADP system is explained in detail at the beginning. It consists of a series of charging and discharging activities on the V_{BUS} supply line during EOS. The purpose of this is to detect the delta of capacitance on the V_{BUS} line. Next were the discussion on ADP architecture and the functionality of each block, e.g. V_{BUS} model, current source/sink, threshold detection circuitry and digital control logics. Last but not least with the current architecture's limitation and background study on the RC timings, it gave a better visualization on the research purpose.

With a good understanding on the current limitation and research purpose, more technical design will be discussed in the next chapter. Chapter 3 will begins with design methodology. This explains how this research is being conducted and how the proposed design was developed. Next is followed by technical discussion on each functional block as well as the design of the transistor level circuitries with calculation.

CHAPTER 3
DESIGN METHODOLOGY AND THEORIES

3.1 Design Methodology

This chapter explains the methodology on how this research is being conducted. The design methodology is illustrated as flow chart in Figure 3.1. The entire process begins with identifying problem statement by looking at the current design incapability. The involve parties are student, Intel technical supervisor as well as university academic supervisor. After the problem statement is defined and agreed by all the parties, modeling of the problem statement take place as to make sure the problem or limitation defined is reproducible and valid. If the modeling result is invalid or not repeatable, it is required to check the inaccuracy whether is caused by any computing environment or tools issue. The design flow has to restart from re-identifying the problem statement if the inaccuracy is not caused by the modeling process.

Once the problem statement is being defined and modeling is done with expected output, the design flow will proceed to proposing new circuit design. This step involves lots of study and technical design knowledge. Modeling of the proposed circuit is crucial before proceeding to implement the design at the transistor level. This is to ensure that circuit designer is implementing a functional solution. Next, implementing the proposed circuit design with real physical transistors after the proposed solution is functionally verified. Followed by, running circuit simulation on the transistor level and doing the circuit analysis on the simulated result. This is to make sure that the implementation matches with the modeling result which had been done previously. If unfortunately the

result doesn't match, circuit implementation needs to be reviewed and re-design to make sure that both are matched. After the results are matched, simulation with PVT variation will be conducted to make sure the circuit is reliable and able to meet the second objective of the research. If the variation is too huge and exceeds the specification given, the implementation of the circuitry has to be reviewed and re-designed. The design flow of this research ends once the simulated results meet the specification given by the USB2.0 OTG Supplement.

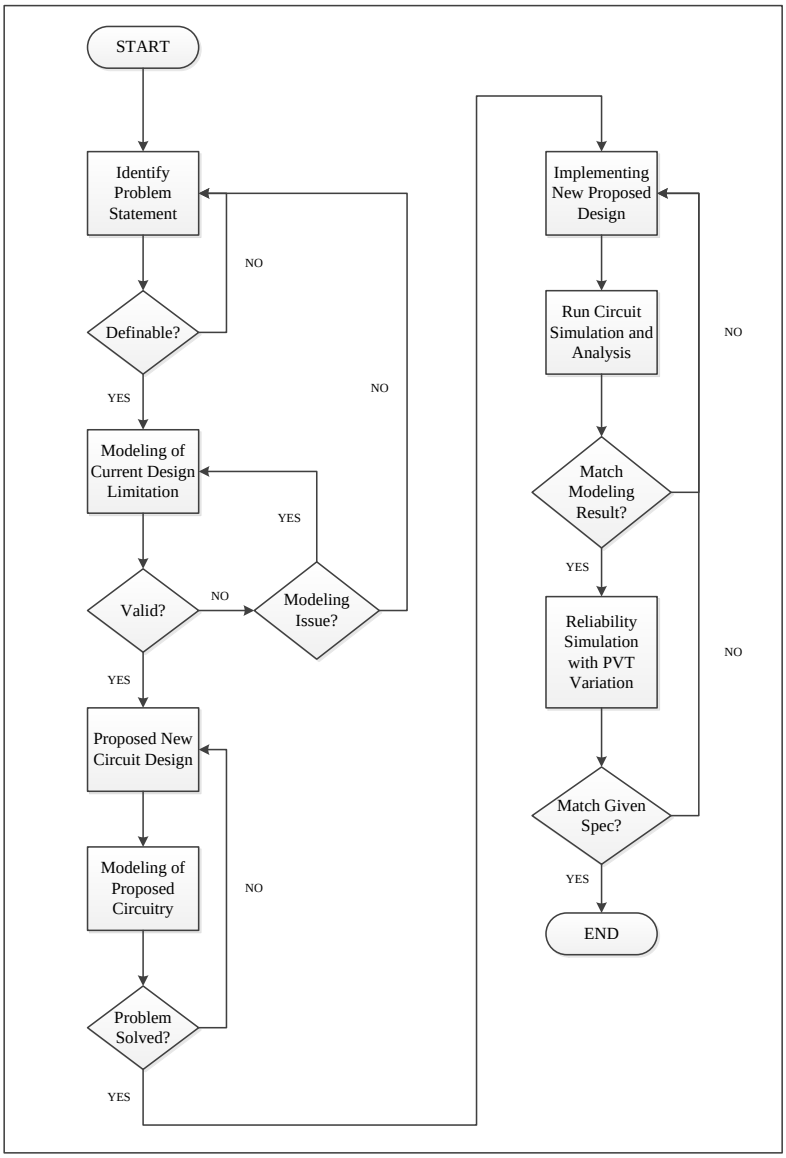

Figure 3.1 : Design Methodology Flow Chart

3.2 Design Theories

3.2.1 Current Source and Current Sink

The entire ADP mechanism is well explained in the Chapter 2. From the previous chapter, it can be seen that the whole ADP operation is heavily dependent on charging and discharging activities of the V_{BUS} power line. Thus, a good current source and sink is extremely crucial in playing its role to provide a better quality of charging and discharging. Besides, the rate of charging and discharging also directly affects the latency and hence the performance of the ADP circuitry. In short, in order to have a good ADP circuitry, a good current source and sink is a must.

There are plenty types of current sources to cater different applications. A simplest current source can be achieved by using a single transistor. Assuming biasing voltage V_b, power supply and V_{TH} is constant, a steady current flow, I_d, can be generated by biasing the transistor in a saturation region ($V_{DS} > V_{GS} - V_{TH}$). Figure 3.2 shows the I_d currents is generated from a single PMOS with V_b biasing voltage.

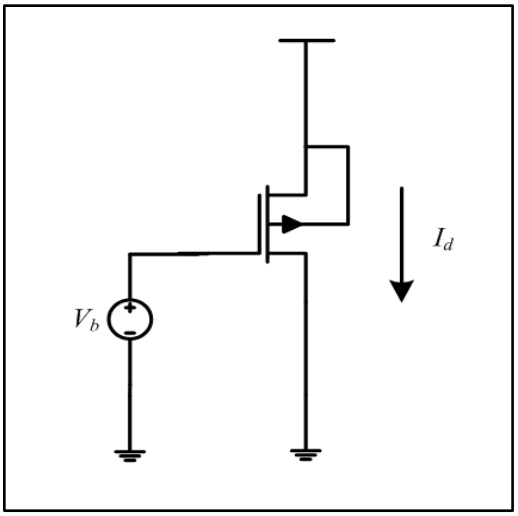

Figure 3.2 : Single MOSFET Current Source

The amount of current flows can be calculated by (3.1). This is one of the most fundamental and important equation for the MOS transistor, namely the I_d equation. This equation determines how much current can a transistor generates by adjusting the transistor size (W/L) and the biasing voltage (V_{GS}). Other parameters like mobility of electrons (μ_n), oxide capacitance (C_{OX}) and threshold voltage (V_{TH}) are fixed by technology process and have less flexibility to be controlled.

$$I_d = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2 \qquad (3.1)$$

Theoretically, a constant drain current, I_d, can be generated by using above formula with correct sizing and fixed biasing voltage. However, world is not perfect. There are many environment factors which can cause changes to the above parameters and make single transistor current source an unworkable one. In practice, the supply voltages will varies and hence the biasing voltage. This will affects the I_d currents as it is directly proportional to the bias voltage (V_{GS}). Figure 3.3 shows how the I_d currents change as the V_{GS} varies. Besides, process parameters are also heavily dependent on the process technology; variations will be even more severe in the small transistors.

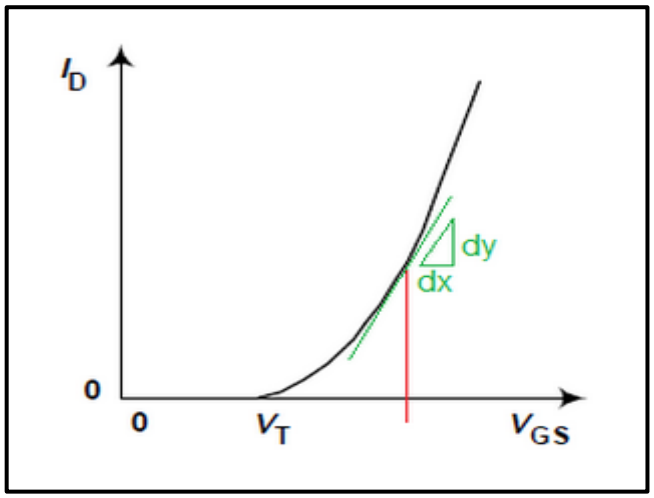

Figure 3.3 : Relationship between I_D versus V_{GS} (Fluxor, 2011)

Self-biased current source with current mirror is another basic architecture which can be found in most of the Electronics textbook. The advantage of this compared to the previous one is it uses self-biasing method instead of having an external voltage supply. However, this is purely for learning purposes and is unsuitable to be implemented in the Integrated Circuit (IC). This is because the potential variation which this circuitry is experiencing is about the same as the previous one. Although the biasing voltage, V_{GS} does not rely on any external voltage supply, it is directly dependent to the power supply, V_{CC}. Other than that, as charging process continues the voltage level at point V_A increases and hence causing the drain to source voltage, V_{DS} of MP_2 reduce. The reduction of V_{DS} will make MP_2 falling in the non-saturation region and provides unstable currents.

$$V_{GS} = |V_{CC} - V_B| \tag{3.2}$$

$$V_{DS} = |V_A - V_{CC}| \tag{3.3}$$

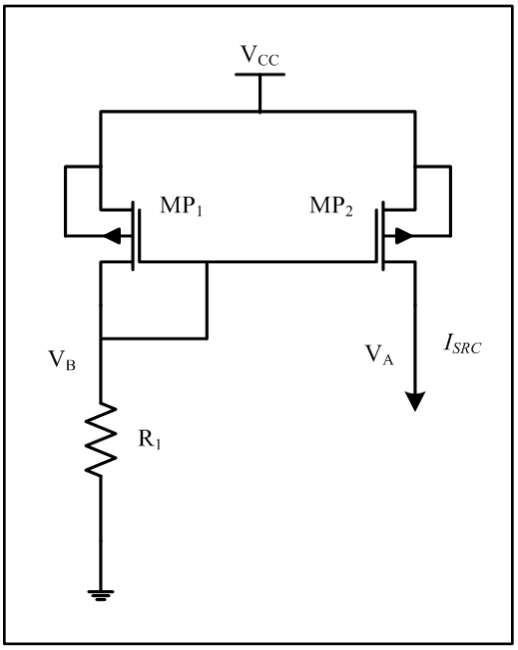

Figure 3.4 : Schematic of Self-Bias Current Source with Current Mirror (Kim, 2011)