# DESIGN OF 0.13-µm CMOS 3-STAGE CASCODE DC/DC BUCK CONVERTER FOR BATTERY OPERATED DEVICES

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# DESIGN OF 0.13-µm CMOS 3-STAGE CASCODE DC/DC BUCK CONVERTER FOR BATTERY OPERATED DEVICES

**by**

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## LIST OF ABBREVIATIONS

| | |
|---|---|
| BJT | Bipolar Junction Transistor |
| CCM | Continuous Conduction Mode |
| CMOS | Complementary Metal Oxide Semiconductor |
| CRM | Critical Conduction Mode |
| DC | Direct Current |
| DCM | Discontinuous Conduction Mode |
| EMI | Electromagnetic Interference |
| ICs | Integrated Circuits |
| Li-ion | Lithium Ion |
| NDR | N-type MOSFET Driver |
| PDR | P-type MOSFET Driver |
| PFM | Pulse Frequency Modulation |
| PTAT | Proportional to absolute temperature |
| PWM | Pulse Width Modulation |
| SiP | System in Package |
| SoC | System on Chip |
| SW | Switch |
| ZVS | Zero Voltage Switching |

## LIST OF SYMBOLS

| | |
|---|---|
| $A_V$ | Small-signal AC voltage gain of the MOSFET |
| $C_{db}$ | Drain and bulk capacitance |
| $C_{ds}$ | MOSFET drain to source parasitic capacitance |
| $C_{gb}$ | MOSFET gate and bulk capacitance |
| $C_{gd}$ | MOSFET gate to drain parasitic capacitance |
| $C_{gs}$ | MOSFET gate to source parasitic capacitance |
| $C_{iss}$ | MOSFET input capacitance |
| $C_{oss}$ | MOSFET output capacitance |
| $C_{out}$ | Output Capacitor |
| $C_{OV}$ | Overlap capacitance |
| $C_{ox}$ | The oxide layer capacitance of the MOSFET |
| $C_{p(i)}$ | Capacitor in parallel with the MOSFET |
| $C_{rss}$ | MOSFET reverse transfer Capacitance |
| $C_{sb}$ | MOSFET source and bulk capacitance |
| $C_{total}$ | MOSFET total parasitic Capacitance |
| $D$ | Duty Cycle |
| $D'$ | Inverse duty cycle |
| $\Delta V_{th}$ | Changed in threshold voltage |
| $\eta$ | Efficiency |
| $f$ | Frequency |
| $i$ | Number of capacitors |

| | |
|---|---|
| $I_d$ | MOSFET drain current |
| $I_{d(\max)}$ | MOSFET maximum drain current |
| $I_{drive}$ | Driver current |
| $I_{in}$ | Input current |
| $I_{out}$ | Output current |
| $k'$ | Process trans conductance |
| $L$ | Inductor |
| $L_{channel}$ | Length of MOSFET Channel |
| $L_p$ | Length of P-type MOSFET |
| $L_n$ | Length of N-type MOSFET |
| $\mu_n$ | The charge carrier effective mobility |
| $n$ | Number of MOSFETs. |
| $N_a$ | The doping density |
| $P_{in}$ | Input Power |
| $P_{out}$ | Output Power |
| $q$ | The electron charge |
| $Q_{gs(on)}$ | Gate Charge of MOSFET |
| $Q_{total}$ | Total Charge of MOSFET |
| $r_{ds}$ | MOSFET Drain to Source resistance |
| $R_{DS(on)}$ | MOSFET drain to source resistance during turn ON |
| $R_G$ | Signal line resistance |
| $r_g$ | Gate electrode parasitic resistance |
| $r_j$ | The source and drain junction depth |

| | |
|---|---|
| $\tau$ | Propagation delay (time constant) |
| $t_{d(on)}$ | The MOSFET turn on delay time. |
| $t_{d(off)}$ | Turn off delay time of MOSFET |
| $t_f$ | Fall interval of MOSFET current from 90% to 10% of max current |
| $t_r$ | Rise interval of MOSFET current from 10% to 90% of max current |
| $t_{ox}$ | MOSFET gate oxide thickness |
| $V_d$ | MOSFET drain voltage |
| $V_{dd}$ | Supply voltage |
| $V_{diode}$ | Voltage of diode attached to the source and gate of the MOSFET |
| $V_{ds(on)}$ | Drain to Source Voltage of MOSFET during turn ON |
| $V_E$ | Error Signal representation in voltage |
| $V_g$ | MOSFET gate voltage |
| $V_{in}$ | Input Voltage |
| $V_{op}$ | Output voltage from operational amplifier |
| $V_{out}$ | Output Voltage |
| $V_{PWM}$ | PWM representation in voltage |
| $V_{pulse}$ | Pulse representation in voltage |
| $V_{ref}$ | Reference Voltage |
| $V_s$ | MOSFET source voltage |
| $V_{SAW}$ | Saw Wave representation in voltage |

| | |
|---|---|
| $V_{sleep}$ | Sleep Signal representation in voltage |
| $V_{th}$ | Threshold voltage of MOSFET |
| $V_{tho}$ | The ideal device threshold voltage |
| $W$ | Width of MOSFET Channel |
| $W_n$ | Width of N-type MOSFET |
| $W_p$ | Width of P-type MOSFET |

**REKA BENTUK 0.13-µm CMOS PENUKAR "BUCK" DC/DC KASKOD 3-PERINGKAT BAGI PERANTI BEROPERASIKAN BATERI**

## ABSTRAK

Selaras dengan perkembangan teknologi, voltan bekalan bagi litar atas cip menjadi semakin kecil. Sebagai contoh ialah bekalan voltan yang terhad kepada 1 V bagi kebanyakan rekabentuk litar 90-nm. Walau bagaimanapun, satu sel bateri ion litium yang digunakan dalam peranti elektronik hari ini mempunyai voltan nominal 3.7V dan mencapai 4.2V pada cas penuh. Oleh itu, penukar turun "buck" DC/DC yang berupaya untuk membekalkan voltan dan arus yang stabil kepada litar adalah diperlukan. Penyelidikan ini adalah berkaitan satu reka bentuk cip 0.13-µm CMOS tanpa transistor kuasa tinggi penukar turun "buck" berupaya untuk menukar turun voltan 3.4 V - 4.2 V kepada 1 V. Cabaran dalam melaksanakan reka bentuk ini adalah penggunaan transistor biasa yang tidak mempunyai ketahanan terhadap voltan dan arus yang tinggi dan sebaliknya mempunyai rintangan yang agak tinggi berbanding dengan transistor kuasa tinggi yang digunakan dalam litar penukar turun komersial. Reka bentuk penukar turun "buck" dalam penyelidikan ini adalah berdasarkan Mod Pengaliran Berterusan (CCM) bagi mendapatkan hingar yang lebih rendah dan kecekapan yang lebih baik pada litar yang memerlukan arus tinggi. Di samping itu, transistor dalam bahagian kuasa litar penukar tersebut adalah dalam konfigurasi tindan/kaskod bagi membolehkan penggunaan voltan bekalan yang lebih tinggi daripada voltan runtuhan transistor. Simulasi adalah menggunakan Cadence SpectreRF. Keputusan menunjukkan bahawa penukar "buck" yang direka bentuk menggunakan transistor bukan kuasa tinggi dapat berfungsi secara efektif seperti mana penukar yang menggunakan transistor berkuasa tinggi dengan riak voltan