

**IMPROVED TOPOLOGIES OF SERIES RESONANT AND LLC
RESONANT DC-DC CONVERTERS FOR MEDIUM OUTPUT VOLTAGE
APPLICATIONS**

by

NOR AZURA BINTI SAMSUDIN

Thesis submitted in fulfillment of the requirements

for the degree of

Doctor of Philosophy

January 2017

ACKNOWLEDGEMENTS

From the depth of my heart, praise Allah the Almighty who is the most praise worthy. Nothing may take place without His leave. I express my heartiest indebtedness to my family for their tender care and affection.

I would like to take this opportunity to express my greatest gratitude and appreciation to my supervisor, Dr. Shahid Iqbal for advices, guidance, patience, encouragement, cooperation and continuous support throughout the course of my research. Besides, I am also thankful for the interesting discussions and valuable suggestions that he has given me to improve the quality of my research work.

Special thanks to Hairul Nizam Abdul Rahman and Ahmad Shauki Noor, the technicians in the Power Laboratory for their help during my experimental works. Thanks also to Mohd Zuber Md. Isa and Elias Zainudin, the technician of the PCB Laboratory for helping me a lot in the PCB fabrication for the development of laboratory prototypes of the proposed converters.

I would also like to take this opportunity to deliver my thanks to individual persons, organizations, and to all my friends which contribute directly or indirectly in giving their cooperation, encouragement and moral support to make the completion of this research possible.

Also thank you to my beloved father and mother, Mr. Samsudin Md. Isa and Mrs. Rosnah Ismail in their never ending support, great understanding and encouragement throughout the years has contributed to success of my studies. May The Almighty One Showers His blessing upon all of us and make this small effort useful and beneficial for others for future reference.

Finally, I would like to thank the Universiti for providing all necessary facilities and equipment to make this research possible. In addition, this research was funded by Research University Grant (RUI) 1001/PELECT/814207 from Universiti Sains Malaysia.

TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	ii
TABLE OF CONTENTS	iv
LIST OF TABLES	xi
LIST OF FIGURES	xiv
LIST OF SYMBOLS	xxix
LIST OF ABBREVIATIONS	xxxii
ABSTRAK	xxxiv
ABSTRACT	xxxvi
CHAPTER ONE : INTRODUCTION	
1.1 General Background	1
1.2 Problem Statement	7
1.3 Objectives	8
1.4 Scope of Research	9
1.5 Contributions of the Research	10
1.6 Thesis Outline	11
CHAPTER TWO : LITERATURE REVIEW	
2.1 Introduction	13
2.2 Resonant DC-DC Converter	13
2.2.1 Inverter Circuits	14
2.2.2 Resonant Tank Circuits	15
2.2.3 Step-up Transformer	16

2.2.4	Rectifier Circuits	17
2.2.5	Filter Circuits	18
2.3	Voltage Multiplier based Resonant DC-DC converters	19
2.3.1	Half Wave Voltage Multiplier Circuit	20
2.3.2	Symmetrical Voltage Multiplier Circuit	20
2.3.3	Hybrid Symmetrical Voltage Multiplier Circuit	21
2.3.4	Comparison of the Voltage Multiplier	22
2.4	Series Resonant DC-DC Converters (SRC)	23
2.4.1	Structure of Series Resonant DC-DC Converter	23
2.4.2	Steady-State Operation of the Series Resonant DC-DC Converter	24
	2.4.2.1 Operation Below Half of the Resonant Frequency ($f_s \leq f_r/2$)	25
	2.4.2.2 Operation Above Resonance ($f_s \geq f_r$)	25
2.4.3	Gain Characteristics of the Series Resonant DC-DC Converter	26
2.4.4	Conventional Series Resonant Medium Voltage DC-DC Converters	27
2.5	Parallel Resonant DC-DC Converter (PRC)	30
2.5.1	Circuit Structure of the Parallel Resonant DC-DC Converter	31
2.5.2	Steady-State Operation of the Parallel Resonant DC-DC Converter	32
	2.5.2.1 Operation Below Half of the Resonant Frequency ($f_s \leq f_r/2$)	32

	2.5.2.2 Operation Above Resonance ($f_s \geq f_r$)	33
2.5.3	Gain Characteristics of the Parallel Resonant DC-DC Converter	33
2.5.4	Conventional Parallel Resonant Medium Voltage DC-DC Converters	34
2.6	Series-Parallel Resonant DC-DC Converters (SPRC)	37
2.6.1	Structure of Series-Parallel Resonant DC-DC Converter	37
2.6.2	Steady-State Operation of the Series-Parallel Resonant DC-DC Converter	38
	2.6.2.1 Operation Below Half of the Resonant Frequency ($f_s \leq f_r/2$)	38
	2.6.2.2 Operation Above Resonance ($f_s \geq f_r$)	39
2.6.3	Gain Characteristics of the Series-Parallel Resonant DC-DC Converter	40
2.6.4	Conventional Series-Parallel Resonant Medium Voltage DC-DC Converters	41
2.7	LLC Resonant DC-DC Converters	43
2.7.1	Circuit Structure of the LLC Resonant DC-DC Converter	43
2.7.2	Steady-State Operation of the LLC Resonant DC-DC Converter	44
	2.7.2.1 Below Resonance Mode ($f_s < f_r$)	44
	2.7.2.2 Above Resonance Mode ($f_s > f_r$)	45
2.7.3	Gain Characteristics of the LLC Resonant DC-DC Converter	46

2.7.4	Conventional LLC Resonant Medium Voltage DC-DC Converters	47
2.8	Comparison of the Resonant DC-DC Converters	49
2.9	Summary	51
CHAPTER THREE : METHODOLOGY		
3.1	Introduction	53
3.2	Double Series Resonant DC-DC Converter with Uniform Voltage Stress on Transformers	55
3.2.1	Circuit Description and Principle of Operation	56
3.2.2	Steady-State Operation	57
3.2.3	Steady-state Analysis	63
3.3	Double Series Resonant DC-DC Converters with Single Power Transformer	77
3.3.1	Circuit Description and Principle of Operation	77
3.3.2	Analysis of Steady-State Operation	78
	3.3.2.1 Bridge Rectifier Circuit	79
	3.3.2.2 Half Wave Voltage Multiplier (HWVM) Circuit	85
3.4	Full-bridge LLC Resonant Inverter Fed Voltage Multiplier based Medium Voltage DC-DC Converter	91
3.4.1	Circuit Description and Principle of Operation	91
3.4.2	Steady-State Operation	92
3.4.3	Steady-state Analysis	99
3.4.4	Gain Characteristics of the Proposed Converter	111

3.5	Interleaved LLC Resonant Inverter Fed Voltage Multiplier based Medium Voltage DC-DC Converters	117
3.5.1	Circuit Description and Principle of Operation	117
3.5.2	Analysis of Steady-State Operation	119
3.5.3	Gain Characteristics of the Proposed Converter	130
3.6	Comparison Among Proposed Converter Topologies	132
3.7	Summary	134

CHAPTER FOUR : DESIGN AND IMPLEMENTATION

4.1	Introduction	136
4.2	Design and Implementation of Inverter Circuits	136
4.3	Design and Implementation of Control Signal Generation Circuits	140
4.4	Design and Implementation of Step-Up Transformers	144
4.5	Design and Implementation of the Resonant Tank Circuits	156
4.5.1	Series Resonant DC-DC Converters	156
4.5.2	LLC Resonant DC-DC Converters	158
4.6	Design and Implementation of Bridge Rectifier and Voltage Multiplier Circuits	162
4.7	Design and Implementation of Load Resistors	165
4.8	Design of PCB	167
4.9	Specifications and Photographs of Implemented Prototypes	172
4.9.1	Double Series Resonant DC-DC Converter with Uniform Voltage Stress on Transformers	172
4.9.2	Double Series Resonant DC-DC Converter with Single Power Transformer	174

4.9.2.1	Bridge Rectifier Circuit	174
4.9.2.2	Half Wave Voltage Multiplier (HWVM) Circuit	176
4.9.3	Full-bridge LLC Resonant Inverter Fed Voltage Multiplier based Medium Voltage DC-DC Converter	178
4.9.4	Interleaved LLC Resonant Inverter Fed Voltage Multiplier based Medium Voltage DC-DC Converter	180
4.10	Summary	181
CHAPTER FIVE : RESULTS AND DISCUSSION		
5.1	Introduction	182
5.2	Double Series Resonant DC-DC Converter with Uniform Voltage Stress on Transformers	182
5.2.1	Simulation Results	182
5.2.2	Experimental Results	187
5.3	Double Series Resonant DC-DC Converter with Single Power Transformer	195
5.3.1	Bridge Rectifier Circuit	195
5.3.1.1	Simulation Result	195
5.3.1.2	Experimental Results	199
5.3.2	Half Wave Voltage Multiplier (HWVM) Circuit	209
5.3.2.1	Simulation Results	209
5.3.2.2	Experimental Results	214
5.4	Full-bridge LLC Resonant Inverter Fed Voltage Multiplier based Medium Voltage DC-DC Converter	225
5.4.1	Simulation Results	225

5.4.2	Experimental Results	229
5.5	Interleaved LLC Resonant Inverter Fed Voltage Multiplier based Medium Voltage DC-DC Converter	237
5.5.1	Simulation Results	237
5.5.2	Experimental Results	241
5.6	Comparison Among Proposed Converter Topologies	251
5.7	Summary	255
 CHAPTER SIX : CONCLUSION AND FUTURE WORK		
6.1	Conclusion	258
6.2	Future Work	261
 REFERENCES		262
 APPENDIX-A - TABLE OF THE EE CORE DATA		
 APPENDIX-B - DATASHEET OF THE E70/33/32 TRANSFORMER CORE		
 APPENDIX-C - TABLE OF AMERICAN WIRE GAUGE (AWG)		
 LIST OF PUBLICATIONS		

LIST OF TABLES

		Page
Table 2.1	Comparison of the parameters performance for voltage multiplier circuits.	22
Table 2.2	The advantages and drawbacks of the conventional series resonant dc-dc converters.	30
Table 2.3	The advantages and drawbacks of the conventional parallel resonant dc-dc converters.	36
Table 2.4	The advantages and drawbacks of the conventional series-parallel resonant dc-dc converters.	42
Table 2.5	The advantages and drawbacks of the conventional LLC resonant dc-dc converters.	49
Table 2.6	Comparison of the advantages and drawbacks of the resonant dc-dc converters.	50
Table 2.7	Comparison of the characteristics of the resonant dc-dc converters.	51
Table 3.1	Comparison of the characteristics among proposed converter topologies.	133
Table 4.1	The transformer turn's ratio and number of turn of the primary and secondary windings of the proposed converters.	148
Table 4.3	The design specifications and components parameters of the simulation model and experimental prototype of the double series resonant dc-dc converter with uniform voltage stress on transformers.	173
Table 4.4	The list of the components used in the prototype of the double series resonant dc-dc with uniform voltage stress on transformers.	173

Table 4.5	The design specifications and components parameters of the simulation model and experimental prototype of the double series resonant dc-dc converter with single power transformer and bridge rectifier circuit.	175
Table 4.6	The list of the components used in the prototype of the double series resonant dc-dc with single power transformer and bridge rectifier circuit.	175
Table 4.7	The design specifications and components parameters of the simulation model and experimental prototype of the double series resonant dc-dc converter with single power transformer and HWVM circuit.	177
Table 4.8	The list of the components used in the prototype of the double series resonant dc-dc with single power transformer and HWVM circuit.	177
Table 4.9	The design specifications and components parameters of the simulation model and experimental prototype of the full-bridge LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter.	179
Table 4.10	The list of the components used in the prototype of the full-bridge LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter.	179
Table 4.11	The design specifications and components parameters of the simulation model and experimental prototype of the interleaved LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter.	181
Table 5.1	The efficiency of the proposed double series resonant dc-dc converter with uniform voltage stress on transformers.	194
Table 5.2	The efficiency of the proposed double series resonant dc-dc converter with single power transformer and bridge rectifier.	208
Table 5.3	The efficiency of the proposed double series resonant dc-dc converter with single power transformer and HWVM circuit.	224

Table 5.4	The efficiency of the proposed full-bridge LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter: (a) for different input voltage and (b) for different output load powers.	235
Table 5.5	The efficiency of the proposed interleaved LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter: (a) for different input voltage and (b) for different output load powers.	249
Table 5.6	The comparison among simulation and experimental results of the output voltage for proposed converters.	252
Table 5.7	The comparison of the experimental results of the output voltage, voltage ripple and percent of the voltage ripple for proposed converters.	253
Table 5.8	Comparison of the proposed converters based on experimental results.	254

LIST OF FIGURES

		Page
Figure 1.1	The auto-transformer with rectifier circuit of the ac-dc converter [11].	2
Figure 1.2	The ac voltage controller based dc power supply [13].	2
Figure 1.3	The PWM dc-dc converter topologies: (a) push-pull dc-dc converter, (b) half-bridge dc-dc converter, and (c) full-bridge dc-dc converter [14-16].	4
Figure 1.4	Elementary resonant switches: (a) ZVS and (b) ZCS operation [24].	5
Figure 1.5	The basic block diagram of the resonant dc-dc converters.	6
Figure 1.6	The schematic of double series resonant dc-dc converter [27].	8
Figure 2.1	The structure of the resonant dc-dc converters [31-33].	14
Figure 2.2	The inverter circuits: (a) half-bridge inverter and (b) full-bridge inverter [35].	15
Figure 2.3	The resonant tank circuits (a) series resonant tank, (b) parallel resonant tank, (c) series-parallel resonant tank, and LLC resonant tank [39-42].	16
Figure 2.4	The model of the step-up transformer [45].	16
Figure 2.5	The equivalent circuit for step-up transformer [45].	17
Figure 2.6	Types of various rectifier circuits: (a) full-bridge rectifier and (b) bridge voltage doubler rectifier [35, 47].	18
Figure 2.7	Output filters for resonant dc-dc converters [50].	18

Figure 2.8	Diode voltage and current waveform for capacitive filter [50].	18
Figure 2.9	The single-stage voltage multiplier circuit [53, 54].	19
Figure 2.10	Output voltage waveform of the single-stage voltage multiplier [53, 54].	20
Figure 2.11	The half wave voltage multiplier circuit [55].	20
Figure 2.12	Symmetrical voltage multiplier circuit [56, 57].	21
Figure 2.13	Hybrid symmetrical voltage multiplier circuit [58].	22
Figure 2.14	Series resonant dc-dc converter: (a) schematic circuit and (b) equivalent circuit [61, 62].	24
Figure 2.15	The current and voltage waveform at the resonant tank for series resonant dc-dc converter at the below resonance mode operation [66].	25
Figure 2.16	The current and voltage waveform at the resonant tank for series resonant dc-dc converter at the above resonance mode operation [66].	26
Figure 2.17	The gain characteristic of the series resonant dc-dc converter.	27
Figure 2.18	ZCS-SR inverter-fed voltage multiplier based medium voltage dc-dc converter with open-loop control [75].	28
Figure 2.19	Multi-output ZCS-SR inverter fed voltage multiplier based medium voltage dc-dc converter [78].	28
Figure 2.20	Fast response double series resonant medium voltage dc-dc converter [79].	29
Figure 2.21	Parallel resonant dc-dc converter: (a) schematic circuit and (b) equivalent circuit [81, 84].	31

Figure 2.22	The current and voltage waveform at the resonant tank for parallel resonant dc-dc converter at the below resonance mode operation [81].	32
Figure 2.23	The current and voltage waveform at the resonant tank for parallel resonant dc-dc converter at the above resonance mode operation [84].	33
Figure 2.24	The gain characteristic of the parallel resonant dc-dc converter.	34
Figure 2.25	The main schematic circuit for power supply system with resonant converter [13].	34
Figure 2.26	Auxiliary resonant commutated soft-switching inverter with bidirectional active switches and voltage clamping diodes [90].	35
Figure 2.27	A medium voltage ac/dc resonant converter based on PRC with single capacitor as an output filter and C_s is not resonant capacitor [91].	36
Figure 2.28	Series-parallel resonant dc-dc converter: (a) schematic circuit and (b) equivalent circuit [92, 95].	38
Figure 2.29	The current and voltage waveform at the resonant tank for series-parallel resonant dc-dc converter at the below resonance mode operation [95, 97].	39
Figure 2.30	The current and voltage waveform at the resonant tank of the series-parallel resonant dc-dc converter at the above resonance mode operation [98].	39
Figure 2.31	The gain characteristics of the series-parallel resonant dc-dc converter.	40
Figure 2.32	Design and implementation of a 40-kV, 20-kJs capacitor charger for pulsed-power application [101].	41

Figure 2.33	Series parallel resonant converter model for a solid state 115-kV long pulse modulator [102].	42
Figure 2.34	LLC resonant dc-dc converter: (a) schematic circuit and equivalent circuit [105, 106].	44
Figure 2.35	The current waveform at the resonant tank for LLC resonant dc-dc converter at the below resonance mode operation [107].	45
Figure 2.36	The current waveform at the resonant tank of the LLC resonant dc-dc converter at the above resonance mode operation [108].	45
Figure 2.37	The gain characteristics of the LLC resonant dc-dc converter.	46
Figure 2.38	Medium voltage generator with LLC resonant circuit [28].	48
Figure 2.39	Medium voltage high frequency resonant dc-dc converter [29].	48
Figure 3.1	The proposed double series resonant dc-dc converters with uniform voltage stress on transformers: (a) with SVM circuit and (b) with HSVM circuit.	57
Figure 3.2	The key steady-state waveform of the proposed series resonant dc-dc converters over one switching cycle.	58
Figure 3.3	The equivalent circuit of the double series resonant dc-dc converters with uniform voltage stress on transformers for each operation modes: (a) Mode 1 [$t_0 \leq t \leq t_1$], (b) Mode 2 [$t_1 \leq t \leq t_2$], (c) Mode 3 [$t_2 \leq t \leq t_3$], (d) Mode 4 [$t_3 \leq t \leq t_4$], (e) Mode 5 [$t_4 \leq t \leq t_5$] and (f) Mode 6 [$t_5 \leq t \leq t_6$].	62
Figure 3.4	The proposed double series resonant dc-dc converters with single power transformer: (a) bridge rectifier circuit and (b) HWVM circuit.	78

Figure 3.5	The equivalent circuit of the double series resonant dc-dc converter with single power transformer and bridge rectifier for each mode operation: (a) Mode 1 [$t_0 \leq t \leq t_1$], (b) Mode 2 [$t_1 \leq t \leq t_2$], (c) Mode 3 [$t_2 \leq t \leq t_3$], (d) Mode 4 [$t_3 \leq t \leq t_4$], (e) Mode 5 [$t_4 \leq t \leq t_5$] and (f) Mode 6 [$t_5 \leq t \leq t_6$].	84
Figure 3.6	The equivalent circuit of the double series resonant dc-dc converter with single power transformer and HWVM for each mode operation: (a) Mode 1 [$t_0 \leq t \leq t_1$], (b) Mode 2 [$t_1 \leq t \leq t_2$], (c) Mode 3 [$t_2 \leq t \leq t_3$], (d) Mode 4 [$t_3 \leq t \leq t_4$], (e) Mode 5 [$t_4 \leq t \leq t_5$] and (f) Mode 6 [$t_5 \leq t \leq t_6$].	90
Figure 3.7	The proposed full-bridge LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter.	92
Figure 3.8	The key steady-state waveform of the full-bridge LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter for one switching cycle.	93
Figure 3.9	The equivalent circuits of the full-bridge LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter for each operating modes: (a) Mode 1 [$t_0 \leq t \leq t_1$], (b) Mode 2 [$t_1 \leq t \leq t_2$], (c) Mode 3 [$t_2 \leq t \leq t_3$], (d) Mode 4 [$t_3 \leq t \leq t_4$], (e) Mode 5 [$t_4 \leq t \leq t_5$], and (f) Mode 6 [$t_5 \leq t \leq t_6$], (g) Mode 7 [$t_6 \leq t \leq t_7$] and (h) Mode 8 [$t_7 \leq t \leq t_8$].	98
Figure 3.10	The equivalent circuit of the proposed full-bridge LLC resonant inverter fed voltage multiplier with the ac load resistance.	111
Figure 3.11	The simplified equivalent circuit of the proposed converter.	112
Figure 3.12	The dc gain characteristics of the proposed converter versus different inductance ratio (a) inductance ratio, $L_n = 1$, and (b) inductance ratio, $L_n = 5$.	116
Figure 3.13	The proposed interleaved LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converters: (a) with SVM circuit, and (b) with HSVM circuit.	118

Figure 3.14	The key steady-state waveform of the interleaved LLC resonant inverter fed based medium voltage dc-dc converters over one switching cycle.	120
Figure 3.15	The equivalent circuit of the interleaved LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converters for each operation modes: (a) Mode 1 [$t_0 \leq t \leq t_1$], (b) Mode 2 [$t_1 \leq t \leq t_2$], (c) Mode 3 [$t_2 \leq t \leq t_3$], (d) Mode 4 [$t_3 \leq t \leq t_4$], (e) Mode 5 [$t_4 \leq t \leq t_5$], and (f) Mode 6 [$t_5 \leq t \leq t_6$], (g) Mode 7 [$t_6 \leq t \leq t_7$] and (h) Mode 8 [$t_7 \leq t \leq t_8$].	129
Figure 3.16	The equivalent circuit of the interleaved LLC resonant inverter fed voltage multiplier with the ac load resistance.	130
Figure 3.17	The ac load equivalent circuit at the resonant tank circuit-1 of the proposed converters.	130
Figure 3.18	The gain characteristics of the interleaved LLC resonant inverter fed voltage multiplier at the inductance ratio, $L_n = 4$.	131
Figure 4.1	Schematic diagram of the half-bridge circuit with the gate drive and bootstrap circuit.	139
Figure 4.2	Schematic diagram of full-bridge circuit with the gate drive and bootstrap circuit.	139
Figure 4.3	Photograph of half-bridge inverter with the gate drive and bootstrap circuits.	140
Figure 4.4	Photograph of full-bridge inverter with the gate drive and bootstrap circuits.	140
Figure 4.5	Block diagram of controller with external pin connections.	141
Figure 4.6	The time sequence of the soft start condition of the UCC25600 controller.	142
Figure 4.7	The schematic diagram to setting of the maximum and minimum switching frequency for UCC25600 controller.	143

Figure 4.8	Photograph of the implemented control circuit using UCC25600 controller.	144
Figure 4.9	Windings structure of the step-up transformer for series resonant dc-dc converters.	150
Figure 4.10	Photographs of prototype step-up transformers for series resonant dc-dc converters.	150
Figure 4.11	Winding structure of the step-up transformer for LLC resonant dc-dc converters.	151
Figure 4.12	Photographs of prototype step-up transformers for LLC resonant dc-dc converters.	152
Figure 4.13	The illustration of the procedure for measurement of leakage and magnetizing inductance: (a) shorting the secondary windings and (b) open the secondary windings.	153
Figure 4.14	The effect of the size of magnetomotive force excursions on the magnitude of the hysteresis loss [124].	156
Figure 4.15	Typical gain characteristics of the LLC resonant dc-dc converter.	159
Figure 4.16	The attainable peak gain, $G_{(ap)}$ with different normalized inductance, L_n .	159
Figure 4.17	Photograph of proposed converter with single resonant tank.	161
Figure 4.18	Photograph of proposed converter with double resonant tanks.	162
Figure 4.19	Schematic diagram of the HWVM circuit for the proposed converters.	162
Figure 4.20	Photograph of half wave voltage multiplier circuit on PCB.	163

Figure 4.21	Schematic diagram of the HSVM circuit for the proposed converters.	164
Figure 4.22	Photograph of HSVM circuit.	165
Figure 4.23	Schematic diagram of load resistor for series resonant dc-dc converters.	166
Figure 4.24	Schematic diagram of load resistor for LLC resonant dc-dc converters.	166
Figure 4.25	Implementation of load resistor for the proposed converters.	167
Figure 4.26	The schematic of inverter circuit with the controller and gate drive circuits for proposed converters: (a) full-bridge inverter configuration and (b) half-bridge inverter configuration.	168
Figure 4.27	Schematic of the voltage multiplier circuits of the proposed converters: (a) HWVM configuration and (b) HSVM configuration.	169
Figure 4.28	Layout of the inverter circuit with the controller and gate drive circuits on PCB for proposed converters: (a) full-bridge inverter configuration and (b) half-bridge inverter configuration.	170
Figure 4.29	Layout of the voltage multiplier circuits on the PCB for the proposed converters: (a) HWVM configuration and (b) HSVM configuration.	171
Figure 4.30	The photograph of the experimental prototype of the double series resonant dc-dc converter with uniform voltage stress on transformers.	174
Figure 4.31	The photograph of the experimental prototype of the double series resonant dc-dc converter with single power transformer and bridge rectifier circuit.	176

Figure 4.32	The photograph of the experimental prototype of double series resonant dc-dc converter with single power transformer and HWVM circuit.	178
Figure 4.33	The photograph of the experimental prototype of the full-bridge LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter.	180
Figure 4.34	The photograph of the experimental prototype for interleaved LLC resonant inverter fed voltage multiplier based medium voltage dc-dc converter.	181
Figure 5.1	Simulation waveforms of the gate signals of the power switches and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 25$ kHz and (b) at switching frequency, $f_s = 35$ kHz.	183
Figure 5.2	Simulation waveforms of the gate signal of the power switch, S_2 , output voltage, V_o and the resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 25$ kHz and (b) at switching frequency, $f_s = 35$ kHz.	185
Figure 5.3	Simulation waveforms of the resonant capacitor voltages, V_{Cr1} and V_{Cr2} and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 25$ kHz and (b) at switching frequency, $f_s = 35$ kHz.	186
Figure 5.4	Simulation waveform of the maximum and minimum output voltage of the proposed double series resonant dc-dc converter with uniform voltage stress on transformers.	187
Figure 5.5	Experimental waveforms of the gate signals of the power switches and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 25$ kHz and (b) at switching frequency, $f_s = 35$ kHz.	188
Figure 5.6	Experimental waveforms of the gate signal of the power switch, S_2 , output voltage, V_o and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 25$ kHz and (b) at switching frequency, $f_s = 35$ kHz.	189

Figure 5.7	Experimental waveforms of the resonant capacitor voltages, V_{Cr1} and V_{Cr2} and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 25$ kHz and (b) at switching frequency, $f_s = 35$ kHz.	190
Figure 5.8	Experimental waveforms of the output voltage and gate-signal voltage for switching frequency, $f_s = 25$ kHz.	192
Figure 5.9	Experimental waveforms of the voltage ripple and gate-signal voltage for switching frequency, $f_s = 25$ kHz.	192
Figure 5.10	Experimental waveforms of the output voltage and gate-signal voltage for switching frequency, $f_s = 35$ kHz.	193
Figure 5.11	Experimental waveforms of the voltage ripple and gate-signal voltage for switching frequency, $f_s = 35$ kHz.	193
Figure 5.12	Measured efficiencies of the proposed converter for output load powers.	194
Figure 5.13	Simulation waveforms of gate signal, V_{GE1} and V_{GE2} and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 31$ kHz and (b) at switching frequency, $f_s = 47$ kHz.	196
Figure 5.14	Simulation waveforms of gate signal voltage, V_{GE1} , output voltage, V_o and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 31$ kHz and (b) at switching frequency, $f_s = 47$ kHz.	197
Figure 5.15	Simulation waveforms of resonant capacitors voltages, V_{Cr1} and V_{Cr2} and resonant currents, i_{Lr1} and i_{Lr2} : (a) lighter load and (b) heavy load.	198
Figure 5.16	Simulation waveform of the maximum and minimum output voltage for proposed double series resonant dc-dc converter with single power transformer and bridge rectifier.	199
Figure 5.17	Experimental waveforms of gate signal, V_{GE1} and V_{GE2} of the power switches and resonant currents, i_{Lr1} and i_{Lr2} at $f_s = 47.5$ kHz.	200

Figure 5.18	Experimental waveforms of gate signal voltage, V_{GE1} , output voltage, V_o and resonant currents, i_{Lr1} and i_{Lr2} : (a) at switching frequency, $f_s = 31$ kHz and (b) at switching frequency, $f_s = 47$ kHz.	201
Figure 5.20	Experimental waveforms of the gate signal voltages, V_{GE1} and V_{GE2} , and voltages across resonant capacitors, V_{Cr1} and V_{Cr2} : (a) for lighter load, and (b) for heavy load.	203
Figure 5.19	Experimental waveforms of the resonant capacitors voltages, V_{Cr1} and V_{Cr2} and resonant currents, i_{Lr1} and i_{Lr2} : (a) for lighter load and (b) for heavy load.	204
Figure 5.21	Experimental waveforms of the output voltage and gate-signal voltage for switching frequency, $f_s = 31$ kHz.	206
Figure 5.22	Experimental waveforms of the voltage ripple and gate-signal voltage for switching frequency, $f_s = 31$ kHz.	206
Figure 5.23	Experimental waveforms of the output voltage and gate-signal voltage for switching frequency, $f_s = 47$ kHz.	207
Figure 5.24	Experimental waveforms of the voltage ripple and gate-signal voltage for switching frequency, $f_s = 47$ kHz.	207
Figure 5.25	Measured efficiencies of proposed converter for different output load powers.	208
Figure 5.26	Simulation waveforms of gate signal, V_{GE1} and V_{GE2} and resonant currents, i_{Lr1} and i_{Lr2} : (a) for output load resistance, $R_L = 120$ k Ω , and (b) for output load resistance, $R_L = 20$ k Ω .	210
Figure 5.27	Simulation waveforms of gate signal, V_{GE1} , output voltage, V_o and resonant currents, i_{Lr1} and i_{Lr2} : (a) for output load resistance, $R_L = 120$ k Ω , and (b) for output load resistance, $R_L = 20$ k Ω .	211