TIME DOMAIN REFLECTION METHOD TO DETECT COPPER WIRE MICRO CRACK WELD DEFECT

by

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TABLES OF CONTENTS

		Page
ACKNOWLEDGEMENT		ii
TABLE OF CONTENTS		iv
LIST OF TABLES		viii
LIST OF FIGURES		ix
LIST OF ABBREVIATIONS		xv
LIST OF SYMBOLS		xvii
ABSTRAK		xix
ABSTRACT		xxi
CHAPTER ONE: INTRODUCTION		
1.0	Introduction	1
1.1	Background	1
1.2	Problem Statement	4
1.3	Objective	7
1.4	Research Methodology	8
	1.4.1 Non-Destructive Test Techniques	8
	1.4.2 Destructive Test Techniques	9
	1.4.3 Software Simulation	10
1.5	Introduction to TDR	10
	1.5.1 Determine Micro Crack Weld Defect Location	14
	1.5.2 TDR Reflection Coefficient (rho)	18
	1.5.3 Dielectric Constant (ε)	19
1.6	Dissertation Outline	22
CHAPTER TWO: LITERATURE REVIEW		
2.0	Literature Review	25
2.1	Interconnect Wire Bonding Technology in Microelectronic	26
2.2	Bond Pull Strength Test	32

2.3 Focused Ion Beam Analysis 34

2.4 TDR Test Technique on Semiconductor Devices 35

2.4.1 Impedance and Delay Measurements in Packages 37

2.4.2 Investigating Microelectronic Interconnect Condition 39

2.4.3 Detecting Solder Joint Crack in PCB 52

2.4.4 Detecting Power Mosfet Missing or Broken Wires on Source Pin 53

2.5 ATE Continuity Test Techniques 56

2.6 Electromagnetic Resonance Test 58

2.7 Force Detected Vibration Analysis 60

2.8 Laser Ultrasonic Inspection 62

2.9 3-Dimensional X-radiographic Computed Tomography 64

2.10 Scanning Acoustic Microscopy (SAM) 67

2.11 Semiconductor Integrated Circuit Interconnection and Packaging Development 69

CHAPTER THREE: RESEARCH METHODOLOGY

3.0 Research Methodology 72

3.1 Device Under Test 74

3.2 ATE Test Measurement 75

3.2.1 Test Summary 79

3.3 TDR Measurement 80

3.3.1 Sample Preparation 82

3.3.2 TDR Module Bandwidth (Frequency) Selection 85

3.3.3 Probing System Selection 86

3.3.4 TDR Voltage and Impedance Response on Various Crack Weld Size 87

3.3.5 Two-dimensional and three-dimensional X-radiographic with Computed Tomography Inspection 88

3.3.6 SEM Inspection 89

3.4 TDR Simulation 92

3.4.1 TDR Characteristic Impedance and Reflected Voltage Amplitude Relationship 93

3.4.2 Crack Length (um) and Crack Area (um^2) Software Simulation 95

3.4.3 Prediction of reflected voltage amplitude and load impedance change 96

CHAPTER FOUR: RESULTS AND DISCUSSIONS

4.0 Results and Discussions 99

4.1 ATE Test Result 100

4.1.1 Typical Datasheet Test Parameter versus ATE Test Result Comparison 106

4.1.2 Critical Test Parameter Distribution between Dual Die Mosfet 108

4.1.3 Mosfet Die 1 and Die 2 Probability Plot Comparison 109

4.2 Scanning Electron Microscopy Inspection analysis Result 113

4.3 TDR Result 120

4.3.1 20GHz TDR Measurement Result 121

4.3.2 50GHz TDR Measurement Result 126

4.3.3 50 GHz TDR Voltage Response on Various Crack Weld Size 133

4.3.4 50 GHz TDR Load Impedance Change on Various Crack Weld Size 139

4.3.5 Test Limit Setting for Automated TDR Test Measurement Setup 144

4.3.6 TDR Measurement Statistical Information 147

4.3.7 TDR Test Result Discussion 157

(i) TDR Measurement Over-rejection 158

4.4 2D and 3D Computed Tomography X-radiographic Result 161

4.4.1 2-Dimensional X-radiographic Result 162

4.4.2 3-Dimensional X-radiographic Computed Tomography (CT) Result 163

4.4.3 Virtual Cross Section from 3D X-ray Computed Tomography Image 167

(i) Z-plane Scanning of Virtual Cross Section Result 168

(ii) X-plane Scanning of Virtual Cross Section Result 170

(iii) Y-plane Scanning of Virtual Cross Section Result 172

4.5 TDR Simulation to Estimate DUT Wire Bond Crack Area and Crack Length 175

(i) Wire Bond Crack Area Simulation 176

(ii) Wire Bond Crack Length Simulation 181

(iii) Crack Length Verification on Simulation Versus Experimental Result 183

(iv) Relative Permittivity (ε) 185

(v) Relative Permittivity (ε) Calculation on Defective versus Good Part 188

4.6 Time Domain Reflectometry Simulation to Estimate Reflected Voltage and Impedance Amplitude 190

4.7 Determine Micro Crack Location 198

4.8 TDR Bandwidth and Possible Detectable Crack Length 199

4.9 Time Domain Reflectometry Test Time Comparison 202

4.10 Summary of Simulation Result 204

CHAPTER FIVE: CONCLUSIONS

5.0 Conclusions 205

5.1 Future Research Recommendations 208

REFERENCES 210

LIST OF PUBLICATIONS

LIST OF TABLES

		Page
Table 2.1	Destructive and Non-destructive Wire Bond Test Techniques Comparison	25
Table 2.2	TDR Measurement by Previous Research	35
Table 3.1	Test Parameters on ATE Measurement	78
Table 3.2	Relationship of voltage and impedance with value of rho in the range of -1 to 1	97
Table 4.1	Overall Test Result Summary	103
Table 4.2	Typical Parameter Electrical Characteristics Rated in Product Datasheet	107
Table 4.3	Test Result Statistical Data	108
Table 4.4	TDR Voltage Response on Various Micro crack Weld Size	133
Table 4.5	TDR Impedance on Various Micro crack Weld Size	139
Table 4.6	TDR Test Measurement Summary and Statistical Information	148
Table 4.7	TDR Test Measurement Results on Reflected Voltage Amplitude	179
Table 4.8	TDR Test Measurement Results on Reflected Voltage Amplitude	183
Table 4.9	Simulation versus Experimental Test Result	195
Table 4.10	TDR VS Other Wire Bond Test Techniques Test Time Comparison	203

LIST OF FIGURES

		Page
Figure 1.1	(i) High resistance	5
Figure 1.1	(ii) Low resistance	5
Figure 1.2	Basic TDR Circuit	11
Figure 1.3	Functional Block Diagrams of the TDR	13
Figure 1.4	TDR Measured Voltage Response Relationship	14
Figure 1.5	Power MOSFET Internal Layout	21
Figure 1.6	Overall Thesis Layout	22
Figure 2.1	Wire Bond Structure in Microelectronic Device	26
Figure 2.2	SEM Image of Crack Weld	28
Figure 2.3	Factors That Causing Micro Crack Weld Defect	29
Figure 2.4	Principle of Pull Test	32
Figure 2.5	Failure Modes on Bond Pull Strength Test	33
Figure 2.6	Trend of TDR Measurement from Literature to Current Work	36
Figure 2.7	Open Ended Configuration	38
Figure 2.8	Reflection Measurement in the Package	38
Figure 2.9	Signal Transmission Line with a Top Metal Plate to Act as a Return Path	40
Figure 2.10	Fixed Length Signal Transmission Lines with a Top Metal Plate Length from 5 mm to 25 mm	40
Figure 2.11	TDR Waveforms with the Varied Length Top Metal Plate	41
Figure 2.12	TDR Waveforms of DUT with Discontinuity at Different Location	42
Figure 2.13	SQFP208 Package Top View and X-ray Image	43
Figure 2.14	TDR Equipment Measurement Setup in Lab Environment	43

Figure 2.15	TDR Waveforms to Localize the Short Circuit between IR_IN and IR_OUT pin	44
Figure 2.16	Short Circuits between 2 Pins on Leadframe	45
Figure 2.17	Cross-section Image of the Short Circuit Defect on Leadframe	
Figure 2.18	(a) Cross Sections of EBGA Package Layout	46
Figure 2.18	(b) X-ray Top View Image	46
Figure 2.19	TDR Measurement Setup	47
Figure 2.20	TDR Waveform of Open Failure at Solder Ball and Substrate Compared to Known Good Device	48
Figure 2.21	TDR Waveforms of Short Failure between Two Solder Balls, Bridged Wire and I/O Pad of Chip	48
Figure 2.22	TDR Waveforms of the I/O Open Failure DUT	50
Figure 2.23	Cross Sections of Open Failure Causing by Scratched Copper Trace	50
Figure 2.24	TDR Waveforms of Short Failure Near to C4 Bump	51
Figure 2.25	Short Failure that Causing by Solder Extrusion Between Failing Bump and Vss Bump	51
Figure 2.26	TDR Test Setup and Reflection Signal if RF Impedance Change Along the Transmission Line	52
Figure 2.27	TDR Voltage Reflection that Causing by the Crack on Solder Joint	53
Figure 2.28	DUT Probing Setup, Source Lead with Gate Lead as a Ground Signal	54
Figure 2.29	Triple Aluminium Wire Bonded Source Pin with One Wire and Two Wire Being Cut to Simulate Missing Wires	54
Figure 2.30	(a) TDR Measurement Response for All Three Type of DUTs	55
Figure 2.30	(b) TDR Response Close Up to the Affected Zone at Wire Bond Interconnects	56
Figure 2.31	Principle of the Electromagnetic Resonance Test Setup	60
Figure 2.32	Overall Laser Ultrasonic Testing Methodology	63

Figure 2.33	Basic 3D X-ray Computed Tomography Setup Schematic	65
Figure 2.34	Virtual Cross Section on Bond Wire Crack Defect by using 3D X-ray	66
Figure 2.35	General Scanning Acoustic Microscopy Measurement Methodology	69
Figure 2.36	Semiconductor Packaging Development over the Years	70
Figure 2.37	Packaging Trend for Past, Current and Future	71
Figure 3.1	TDR Measurement and Simulation Research Methodology	73
Figure 3.2	Device Under Test Process	74
Figure 3.3	Test stimulus and DUT response verification	75
Figure 3.4	Test Head and DUT interconnections	76
Figure 3.5	Time Domain Reflectometry Measurement	80
Figure 3.6	TDR Test Setup	81
Figure 3.7	Package Outline and Internal Circuit Diagram for MLP	83
Figure 3.8	Device Under Test Internal Layout	84
Figure 3.9	Identify Crack Weld Size According to Voltage Amplitude	88
Figure 3.10	SEM Sample Image on Micro Crack on Weld Bond Defect	90
Figure 3.11	Time Domain Reflectometry Simulation Flow	92
Figure 3.12	Relationship between Voltage (V) and Impedance (ohm)	98
Figure 4.1	Overall ATE Test Result that Shown in Tesec Map Handler	102
Figure 4.2	User Interface on Test Software Info, Test Job Info and Quantitative Test Result	103
Figure 4.3	Test Software Binning User Interface to Sort Out Good Parts, Assembly Rejects and Test Parametric Rejects	104
Figure 4.4	Location of Sample 1, 2 and 3 on Each Panel	105
Figure 4.5	Physical DUT in Lead Frame Strip with Four Panels in Ring Form	106
Figure 4.6	Pre Gate Threshold Voltage Probability Plot between Die 1 and Die 2	110

Figure 4.7	Normal Gate Threshold Voltage Probability Plot between Die 1 and Die 2	111
Figure 4.8	Post Gate Threshold Voltage Probability Plot between Die 1 and Die 2	112
Figure 4.9	Breakdown Voltage Probability Plot between Die 1 and Die 2	113
Figure 4.10	Laser Decapsulation Technique to Remove Molding Compound for SEM Inspection	114
Figure 4.11	SEM Image on the Micro Crack Wedge Bond 90% Crack Sample	115
Figure 4.12	SEM Image on the Micro Crack Wedge Bond 50 % Crack Sample	115
Figure 4,13	SEM Image on the Micro Crack Wedge Bond 10% Crack Sample	116
Figure 4.14	SEM Image on the Good Wedge Bond Sample	118
Figure 4.15	SEM Image on the Open Wedge Bond Sample	118
Figure 4.16	Optical Microscope Image (600x Magnification) on Micro Crack Weld Sample	119
Figure 4.17	Tektronix 20GHz TDR Voltage Full Waveform for the Micro Crack Weld Samples Compared to the Good Sample	123
Figure 4.18	Tektronix 20GHz TDR Voltage Zoom In Waveform for the Micro Crack Weld	125
Figure 4.19	Overall Tektronix 50GHz TDR Voltage Waveform for the Three Micro Crack Weld Samples Compared to the Good Sample and Bare Sample	128
Figure 4.20	Tektronix 50GHz TDR Voltage Curve for the Micro Crack Weld Sample 1 Compared to the Good Sample and Bare Sample	130
Figure 4.21	TDR Impedance Curve for the Micro Crack Weld Sample compared to the Good Sample and Bare Sample	132
Figure 4.22	TDR Voltage Waveform for 50 % Crack Wedge Bond	136
Figure 4.23	TDR Voltage Waveform for 90 % Crack Wedge Bond	137
Figure 4.24	TDR Voltage Waveform for 10 % Crack Wedge Bond	138
Figure 4.25	TDR Impedance Curve for 50 % Crack Wedge Bond	141

Figure 4.26	TDR Impedance Curve for 90 % Crack Wedge Bond	142
Figure 4.27	TDR Impedance Curve for 10 % Crack Wedge Bond	143
Figure 4.28	Load Impedance Upper and Lower Specification Limit Set for Automated TDR Testing	146
Figure 4.29	(a) Test Map on Panel 1	150
Figure 4.29	(b) Test Map on Panel 2	150
Figure 4.29	(c) Test Map on Panel 3	151
Figure 4.29	(d) Test Map on Panel 4	151
Figure 4.30	Overall TDR Waveform with Test Specification Limit Set	152
Figure 4.31	(a) Boxplot Definition	154
Figure 4.31	(b) Boxplot Comparison from Panel 1 to Panel 4	155
Figure 4.32	Scatter Plot with Specification Limit Set	156
Figure 4.33	TDR Measurement Variance and Over-rejection	159
Figure 4.34	2D X-ray Image on Micro Crack Weld Sample	162
Figure 4.35	3D X-ray CT Image on Micro Crack Weld Sample	164
Figure 4.36	Hi-resolution 3D X-ray CT Image on 50 % Micro Crack Weld Sample 1	166
Figure 4.37	Hi-resolution 3D X-ray CT Image on 90 % Micro Crack Weld Sample 2	166
Figure 4.38	Hi-resolution 3D X-ray CT Images on 10% Micro Crack Weld Sample 3	167
Figure 4.39	Z-Plane Computed Tomography Scanning on 50 % Micro Crack Sample 1	169
Figure 4.40	Z-Plane Overall View of the 50 % Micro Crack Weld Sample 1	169
Figure 4.41	Hi-resolution 50 % Micro Crack Weld Sample 1 X-ray Image in Z-Plane	170
Figure 4.42	X-Plane Computed Tomography Scanning on 50 % Micro Crack Weld Sample 1	171
Figure 4.43	X-Plane Overall View of the 50 % Micro Crack Weld Sample 1	171

Figure 4.44	Hi-resolution 50 % Micro Crack Weld Sample 1 X-ray Image in X-Plane	172
Figure 4.45	Y-Plane Computed Tomography Scanning on 50 % Micro Crack Weld Sample 1	173
Figure 4.46	Y-Plane Overall View of the 50 % Micro Crack Weld Sample 1	173
Figure 4.47	Hi-resolution 50 % Micro Crack Weld Sample 1 X-ray Image in Y-Plane	174
Figure 4.48	Crack Area and Crack Length Definition	176
Figure 4.49	Area of Copper Wire Bond Simulation by Reflected Voltage	178
Figure 4.50	Area of Copper Wire Bond Simulation by Impedance	180
Figure 4.51	Crack Length of Copper Wire Bond Estimation	182
Figure 4.52	Possible Simulated versus Experimental Crack Length	184
Figure 4.53	Dielectric Constant Effect Corresponding to Speed of Time Interval	187
Figure 4.54	Effective Dielectric Constant Calculation for Known Good Device	189
Figure 4.55	Relationship between Reflected Voltage Amplitude and Reflection Coefficient (rho)	192
Figure 4.56	Relationship between Reflection Coefficient and Impedance at the Reflected Path	194
Figure 4.57	(a) Load Impedance on 10 % Crack Weld Device	196
Figure 4.57	(b) Load Impedance on 50 % Crack Weld Device	197
Figure 4.57	(c) Load Impedance on 90 % Crack Weld Device	197
Figure 4.58	TDR Waveform to Determine Micro Crack Weld Location	198
Figure 4.59	Relationship between Possible Detectable Wire Crack Length (μm) and TDR Bandwidth (GHz)	201

LIST OF ABBREVIATIONS

AC	Alternative current
Al	Aluminium
AMD	Advanced micro devices
ATE	Automated test equipment
Au	Gold
BGA	Ball grid array
Bv	Breakdown voltage
CSP	Chip scale package
CT	Computed tomography
Cu	Copper
DIP	Dual in-line package
DUT	Device under test
EBGA	Enhanced Ball Grid Array
EOS	Electrical overstress
ESD	Electrostatic discharge
FIB	Focused ion beam
Ga	Gallium
IC	Integrated circuit
Idss	Zero gate voltage drain current
Igss	Gate-body leakage current
IR	Infrared
I-V	Current-voltage curve
Max	Maximum
Mean	Average
MicroFET	Micro field effect transistor
Min	Minimum
MLP	Micro leadframe package

MOSFET	Metal–oxide–semiconductor field-effect transistor
NiPdAu	Nickel/Palladium/Gold
PCB	Printed circuit board
PLLCC	Plastic Leadless Chip Carrier
QFN	Quad flat no-leads package
R&D	Research and development
RDSon	Static drain-source on resistance
RF	Radio frequency
SAM	Scanning acoustic microscopy
SEM	Scanning electron microscope
SOIC	Small Outline Integrated Circuit package
SOJ	Small outline J-leaded package
SOP	Small outline package
Spec	Specification
Stddex	Standard deviation
TDR	Time domain reflectometry
TSOP	Thin small outline package
TSSOP	Thin small outline package
UPH	Unit per hour
Vgsth	Gate threshold voltage
WLCSP	Wafer level chip scale package
WLP	Wafer level package

LIST OF SYMBOLS

Z_0	Constant impedance/Alternate current resistance
I	Current
β	Degree
ε	Dielectric constant
l	Distance in the conduction path
F	Force
f	Frequency/bandwidth
G	Gauss
GHz	Gigahertz
Hz	Hertz
Z_i	Impedance generated by incident pulse
Z_r	Impedance induced by reflection
$V_{incident}$	Incident voltage wave
keV	Kilo-electronvolt
Z_L	Load impedance
V_{measured}	Measured voltage wave
MHz	Megahertz
m/s	Meter per second
µA	Micro ampere
µm	Micron
mA	Milli ampere
mΩ	Milli ohm
ms	Milli-second
mm	Millimeter
mm/sec	Millimeter per second
mV	Millivolt
mV/div	Millivolt per division

min	Minutes
nA	Nano ampere
nsec	Nano-second
Ω	Ohm
%	Percentage
ε_0	Permittivity of free space
ε	Permittivity of the material
psec	Pico-second
psec/div	Pico-second per division
$V_{\text{reflected}}$	Reflected voltage wave
ε_r	Relative permittivity
μ_r	Relative permeability
ρ	Resistivity
sec	Second
c	Speed of light
rho	TDR Reflection Coefficient
T	Time
mil	Unit of length
v	Velocity of propagation
V	Volt
A	μm^2

KAEDAH PEMANTULAN DOMAIN MASA UNTUK MENGESANKAN KECACATAN RETAKAN MIKRO PADA IKATAN DAWAI TEMBAGA

ABSTRAK

Kecacatan struktur ikatan dawai telah memberikan kesan yang penting terhadap kualiti sesebuah peranti mikroelektronik. Kaedah tradisi yang menggunakan ujian elektrik tidak dapat mengesan retakan ikatan dawai tembaga yang berpanjangan dari 1 hingga 20 μm. Kejadian ini dikenali sebagai retakan mikro yang wujud pada peranti MOSFET kuasa Pembungkusan Tanpa-dawai Bertuangan (MLP) dengan ikatan dawai tembaga berdiameter 38 μm dan panjang 800 μm. Dalam penyelidikan ini, sejumlah 1368 peranti MOSFET telah menjalankan ujian elektrik dengan instrumen Credence ASL1000. Kajian kaedah alternatif Pemantulan Domain Masa (TDR) yang mengesani kecacatan retakan dari segi ciri-ciri fizikal dan simulasi dijalankan untuk tujuan menangani masalah ini. Parameter-parameter kajian merangkumi input TDR (frekuensi 20 dan 50 GHz dan domain masa antara 10 hingga 23 psec) dan keluaran TDR (voltan TDR dari 0 hingga 250 mV dan impedans) pada retakan ikatan dawai (panjang retakan dawai dari hingga 20 μm dan kawasan retakan dawai). 50 GHz TDR berjaya mengesan 10, 50 and 90 % dimensi retakan dengan panjang fizikal 1, 4 and 10 μm masing-masing. Kaedah 2D & 3D Tomographi X-ray Terkomputer (CT) dan Mikroskop Imbasan Elektron (SEM) digunakan untuk membandingkan keputusan ujian TDR. Simulasi panjang retakan dawai dan kawasan retakan membolehkan dimensi retakan dianggarkan tanpa menggunakan ujian instrumentasi TDR. Selain daripada itu, simulasi voltan dan impedans TDR menyediakan maklumat yang penting terhadap keadaan ikatan dawai pada peranti mikroelektronik. Kaedah pemantulan domain masa bernovel ini

membolehkan retakan mikro pada ikatan dawai tembaga dalam peranti MOSFET kuasa diuji dengan dimensi fizikal 1 μm dan simulasi dimensi 10 μm berbanding dengan kaedah-kaedah lain. TDR telah mengatasi had ujian tradisi dan mencapai kaedah novel melalui resolusi pengesanan retakan ikatan dawai.

TIME DOMAIN REFLECTION METHOD TO DETECT COPPER WIRE MICRO CRACK WELD DEFECT

ABSTRACT

Structural integrity of wire bonding interconnection is having a significant impact on the quality of microelectronic devices. Conventional electrical test methodology is unable to detect 1 to 20 μm of cracks that exists in wire bond stitch weld. This micro crack has becomes prominent in Power MOSFET Molded Leadless Package (MLP) with copper wire of 38 μm in diameter and 800 μm long. In this research, total 1368 units of Power MOSFETs was tested using a Credence ASL1000 tester. The aim of this research is to investigate an alternative methodology by establishing a comprehensive physical and simulation characterization technique namely Time Domain Reflectometry (TDR) to address this issue. Parameters that have been investigated included TDR input (frequency of 20 and 50 GHz and time domain between 10 to 23 psec) and output (reflection voltage from 0 to 250 mV and characteristic impedance) responses on the wire crack geometries (length from 1 to 20 μm and crack area). 50 GHz TDR successfully detected 10, 50 and 90 % of crack size with physical length of 1, 4 and 10 μm respectively. In order to complement with the TDR results, other non-destructive 2D & 3D X-ray Computed Tomography (CT) and destructive Scanning Electron Microscopy (SEM) characterization techniques have been used. Simulation of crack weld length and crack area has also been performed, in order to estimate the physical crack dimension without using the actual TDR instrument. Besides, a prediction of TDR response on both reflection voltage and impedance change have also been verified. Novelty of this work is on the non-destructive electrical test methodology that able to detect micro crack defect at

wedge bond in a Power MOSFET gate wire. This effective technique offers up to physical dimension of 1 μm and simulated dimension of 10 μm comparing with other techniques. TDR has overcome the conventional test limitation and achieved a novel approach through the defined detection resolution for micro crack weld.

CHAPTER ONE
INTRODUCTION

1.0 Introduction

This chapter introduces the wire bond micro crack weld defect in semiconductor devices and the problem that manufacturers facing to screen out this defect by using multiple type of test methodologies effectively. The objective of the study that is focused on non-destructive test technique will be discussed in details. No non-destructive electrical measurement method is developed for bond wires small cracks detection (Krüger et al,. 2014). In this research, Time Domain Reflectometry (TDR) test measurement technique is the main test methodology used for detection of micro crack. Existing well-known non-destructive and destructive test techniques are used for benchmarking and comparing TDR measurement test results. Research methodology which involving experimental measurement and simulation will be included as well.

1.1 Background

The integrated circuit (IC) is the electronic circuits that attached to the semiconductor substrate, usually silicon substrate. IC packaging process or semiconductor assembly is the back-end electronic manufacturing process of semiconductor device fabrication where the IC is encapsulated into the supporting dielectric body case that prevents physical damage and causing a functionality or application failure on the microelectronic circuit lifespan. Microelectronic devices are electrically connected to the packaging exterior through the conductive pad or lead (Livshits et al., 1996). Power MOSFET in Molded Leadless Package (MLP) is

selected as Device Under Test (DUT) on this research. Micro crack weld located on gate wire on this Power MOSFET is the interconnect under investigation.

Wire bond technology is the interconnections that connect between IC or semiconductor package to its packaging during semiconductor assembly process (Appelt et al., 2010). In semiconductor industry, wire bonding is the primary method of making interconnections between an IC and a printed circuit board (PCB) during semiconductor device manufacturing process. This interconnect is bonded by ball bonding with a loop wire to the wedge bond at the conductive pad. The wire bond interconnect technology has been the most flexible and common in the semiconductor packaging industry since the last two decade. It usually used the aluminium (Al), copper (Cu) and gold (Au) material as the bond wire (Ano, 2003) with various types of wire diameters and wire length in between connection from IC to the packaging leadframe. Traditionally, Au is the main selection for interconnect material with the aluminium metallized bond pads by a thermosonic process (Srikanth et al., 2004). However, Cu wire bonded on NiPdAu metallization is selected for this research. An efforts to replace the Au wire with Cu wire in the microelectronics packaging technology in recent years due to soaring price of Au (Chen et al., 2011).

Wire bonding is one of the very important method in packing interconnect technology. It will continue to prosper in microelectronic packaging industry. The demand for lighter in weight, smaller in dimension and good reliability products is a challenge in wire bond quality control. The reliability of the wire bond will