HARDWARE DESIGN OF RANDOM NUMBER GENERATOR AND RANDOM WALK-ON-BOUNDARY ALGORITHM TO COMPUTE UNIT CUBE CAPACITANCE IN FPGA

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by

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LIST OF SYMBOLS

$v(y_n)$	The inverse of the distance between static point x and traveling point y
N	Number of samples
μ	Mean
σ	Standard deviation
∑	Summation
r	Pearson correlation coefficient
f	Frequency

LIST OF ABBREVIATIONS

3D	Three-dimensional
ASIC	Application Specific Integrated Circuit
AWGN	Accuracy White Gaussian Noise Generator
BEM	Boundary Elements Method
CA	Cellular Automaton
CASR	Cellular Automata Shift Register
CLB	Configurable Logic Block
CPLD	Complex Programmable Logic Devices
CPU	Central Processing Unit
DDR	Double Data Rate
DDR3	Double Data Rate Type Three
DFG	Data Flow Graph
DSP	Digital Signal Processing
FIFO	First in First Out
FEM	Finite Element Method
FPGA	Field Programmable Gate Array
FRW	Floating Random Walk
FSM	Finite State Machine
GCA	Grand Challenge Application
GUI	Graphical User Interface
HDL	Hardware Description Language
GPU	Graphic Processing Unit
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
ln	Natural logarithm
I/O	Input/Output
IP	Intellectual Property
ISE	Integrated Software Environment
LCA	Logic Cell Array
LFSR	Linear Feedback Shift Register

LUT	Look-Up Table
MC	Monte Carlo
MEMS	Microelectromechanical Systems
NEMS	Nanoelectromechanical Systems
MPI	Message Passing Interface
MT	Mersenne Twister
NRE	Non-Recurring Engineering
NGD	Native Generic Database
ORCA	Optimized Reconfigurable Cell Array
PAR	Place and Route
PC	Personal Computer
pASIC	programmable Application Specific Integrated Circuit
PROM	Programmable Read Only Memory
PLD	Programmable Logic Device
RNG	Random Number Generator
ROM	Read Only Memory
SDR	Single Data Rate
SRAM	Static Random Access Memory
SDRAM	Synchronous Dynamic Random Access Memory
SPRNG	Scalable Parallel Random Number Generators
SRAM	Static Random Access Memory
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VIA	Virtual Interface Architecture
VLSI	Very Large Scale Integration
UCF	User Constraint File
USB	Universal Serial Bus
WOB	Walk on Boundary
WOP	Walk On Planes
XST	Xilinx Synthesis Technology

REKA BENTUK PERKAKASAN PENJANA NOMBOR RAWAK DAN ALGORITMA RANDOM WALK-ON-BOUNDARY UNTUK PENGIRAAN KAPASITAN KIUB UNIT DALAM MEDAN BOLEH-PROGRAM TATASUSUN GET

ABSTRAK

Kaedah Monte Carlo (MC) digunakan secara meluas dalam masalah matematik yang terlalu rumit untuk diselesaikan secara analitikal. Kaedah ini melibatkan proses persampelan nombor rawak dan kebarangkalian untuk menganggarkan keputusan. Disebabkan kaedah MC bergantung kepada bilangan besar nombor rawak yang berkualiti untuk menghasilkan keputusan yang berjitu tinggi, maka pembinaan penjana nombor rawak (RNG) yang baik adalah sangat penting. Secara umumnya, penjana nombor rawak dan kaedah MC dilaksanakan berasaskan perisian dan disimulasikan dengan menggunakan superkomputer dan kelompok komputer peribadi. Walau bagaimanapun, pelaksanaan perkakasan ini menggunakan perbelanjaan yang lebih tinggi dan ruang yang besar. Dengan peningkatan kepadatan dan kelajuan Medan Boleh-Program Tatasusun Get (FPGA) yang terkini, pelaksanaan secara terus kepada perkakasan ini dapat direalisasikan. Projek ini bertujuan untuk melaksanakan kaedah MC cara *Random "Walk on the Boundary"* (WOB) dan penjana nombor rawak untuk mengira kapasitan kiub unit pada Xilinx Spartan-6 LX 150T FPGA yang digabungkan dalam papan Avnet S6LX150T. Empat model gabungan penjana nombor rawak dinilai untuk membina RNG dan model yang menghasilkan hasil pengiraan yang paling tepat telah dipilih untuk pelaksanaan. Keputusan penilaian menunjukkan bahawa RNG yang dibina daripada gabungan penjana nombor rawak 37-bit *Linear Feedback Shift Register* (LFSR) dan 43-bit *Cellular Automata Shift Register* (CASR) menghasilkan keputusan pengiraan yang paling tepat. Pelaksanaan pengiraan kaedah MC dan RNG untuk mengira kapasitan kiub unit ke atas Xilinx Spartan-6 LX 150T FPGA berjaya

dilaksanakan. Ini menunjukkan FPGA boleh digunakan sebagai satu lagi alternatif perkakasan untuk kajian seperti ini.

HARDWARE DESIGN OF RANDOM NUMBER GENERATOR AND RANDOM WALK-ON-BOUNDARY ALGORITHM TO COMPUTE UNIT CUBE CAPACITANCE IN FPGA

ABSTRACT

Monte Carlo (MC) method is widely applied in mathematical problems that are extremely complicated to be resolved analytically. The method involves sampling process of the random numbers and probability to estimate the result. Since it depends on an enormous number of good quality random numbers to produce a high accuracy result, developing a good random number generator (RNG) is vital. Generally, the RNGs and the MC methods are implemented in software-based and simulated using supercomputer and cluster Personal Computer (PC). Nevertheless, this implementation consumes large expenses and inefficient space. With the latest improvement of the density and speed of Field Programmable Gate Arrays (FPGA), a direct implementation onto this hardware is feasible. This work aims to implement the RNG and MC method of Random Walk on the Boundary (WOB) to compute the unit cube capacitance on the target device Xilinx Spartan-6 LX 150T FPGA which were incorporated in Avnet S6LX150T development board. Four uniform RNGs model were evaluated to build the RNG, and the model that produced the most accurate computation result was chosen for the implementation. From the evaluation, the result has demonstrated that the RNG built from uniform RNG of 43-bit Linear Feedback Shift Register (LFSR) and 37-bit Cellular Automata Shift Register (CASR) uniform RNG combination produced the most accurate computation result. The implementation of the MC computation and RNG to compute the unit cube capacitance has been successfully carried out on the Xilinx Spartan-6 LX 150T FPGA. It therefore demonstrates the feasibility of the FPGA as another hardware alternative for this kind of work.

CHAPTER ONE

INTRODUCTION

1.1 Overview

Capacitor is one of the vital inventions produced from the discovery of electrostatic field. It is a passive electronic component which its main function is to electrostatically store energy in an electric field to the highest extent at a given potential (Sadiku, 2010) . The capacitors can be charged-up in minutes or even seconds and able to instantly deliver the electrical energy. They have long lifetime with charge and discharge up to 100,000 to 1,000,000 cycles, withstand weather change, shocks and vibration in various applications (Kim, Kim, Hyun, Kim, & Yang, 2015)

The electrochemical capacitors also referred as ultracapacitors able to power the hybrid vehicle and commuter bus. The ultracapacitors are cost effective with availability to provide capacity with factor of 20 times than capacitor in a similar structure (Atmaja & Amin, 2015). With this breakthrough, it had presented supersede performance over the battery technology. With the increase of the electrical items run on battery-personal electronics, grid energy storage, and medical devices, there is high possibility of capacitor in replacing battery as an electricity storage in the future (Schultz & Querques, 2014).

In high performance integrated circuit (IC) and IC packaging, Wang, Li, P.-S.Kooi, & Leong (2001) stated that the rapid increase in operating frequencies and scales of the circuit systems and computation of capacitance for arbitrarily shaped three-dimensional (3D) structures is necessary in verifying final circuit performance and signal integrity. Similar statement was made by Shu, Sarin, & Weiping (2005) about the 3D capacitance extraction for the timing and signal integrity analysis in Very Large Scale Integration (VLSI) circuits, multi-chip modules, printed circuit boards and packages. The application of capacitance computation in arbitrary shape is not limited to ultracapacitor development and IC design, it is also crucial in the application of the microelectromechanical Systems (MEMS) and nanoelectromechanical Systems (NEMS) development (Kambali & Pandey, 2016). Literally, the efficient computation of the capacitance in high accuracy has become essential.

Nevertheless, the analytic solution to compute the capacitance is restricted to idealize 3D geometries like spherical, infinite parallel plate and infinite cylinder instead of real world applications of finite sized arbitrary objects. For geometry with complicated configuration, numerical solutions based on the discretization of differential and/or integral operators in a computational domain (domain methods) and/or over its boundary (boundary methods) are required (Peres, Neves, Almeida, & Machado, 2013).

Among the 3D arbitrary objects, unit cube particularly categorized as "one of the major unsolved problems of electrostatic theory due to absence of the analytic solution" (Read, 2004; Reitan & Higgins, 1951). Since the first computation method published by Reitan and Higgins in 1951, there are various computation methods have been introduced to numerically estimate the unit cube capacitance in high accuracy. These includes Monte Carlo (MC) algorithms such as Brownian dynamics algorithm, Walk on sphere, Green's function first passage, Walk on planes (WOP) and Random walk on boundary (WOB). The deterministic algorithms associated to this computation are surface-charge or boundary-element method (BEM), the Finite different method and Finite-element method (FEM). According to Hwang, Mascagni, & Won (2008), other than the surface charge method with extrapolation to an infinite number of subdivision, Monte Carlo (MC) algorithms are found to be more efficient than deterministic algorithms.

Although the MC algorithms are preferred and effective for evaluating integrals over high-dimensional domains such as very large and sparse systems of equations, practical issues exist with the computer time and software to be employed (James, 2003). To enhance the efficiency of the application, most of the MC algorithms are implemented with supercomputer or cluster Personal Computer (PC). Apparently, the usage of supercomputer or cluster PC is seen as a limitation to the public people in terms of cost and space. It could be witnessed with available current commercial solutions are mostly based on deterministic methods. For instance, Electro 2D/RS field simulator from Integrated Engineering Software that was developed in 1985 is based on BEM and Finite Element Method FEM (Integrated, 2014). In addition, Robin Hood Solver v2.0 is electrostatic modeling software by Cartes Calculi limited was built from Robin Hood BEM (J. A. Formaggio et al., 2012).

Apart from supercomputer and cluster PC, another compatible and evolving computing hardware are the embedded systems. The embedded systems are computer chips, normally microprocessor or microcontroller that are integrated as a component of some larger or independent system (Reddy, 2002). They have the characteristics of ability to self-start and sustain and command a particular real time device or task. As an added advantage, they are low cost devices (Ball, 2002). There are several hardware platforms that can be applied in developing embedded systems. One of them is Field Programmable Gate Array (FPGA). It has been shown a great interest by the researchers due to its flexibility in implementation, reconfigurable and customized for specific application. This study aims to apply the FPGA as an alternative hardware platform to compute the unit cube capacitance. The MC method with the Random Number Generator (RNG) to supply parallel streams of 10^6 random numbers are developed and implemented on the FPGA.

1.2 Problem Statement

The MC method of random WOB algorithm with the RNG are currently implemented in software executed in supercomputer or cluster of PCs using message passing interface (MPI) and Scalable Parallel Random Number Generator (SPRNG) (Hwang et al., 2008). The SPRNG like most of RNG that developed in software based. It is a common used library to produce parallel streams random numbers for MC simulation. Indeed, with the improvement of FPGA density in recent days, it is getting popular to implement RNG directly in the hardware (D.-U. Lee, Villasenor, Luk, & H.W.Leong, 2006).

FPGAs are suitable platforms for hardware version RNG to produce huge random numbers because of parallel computing capability. Nevertheless, Brownian motion which forms the theoretical base of the random WOB algorithm is simulated using Normal (Gaussian) distribution and the calculation is based on the maximum decimal values in the range of [0, 1] (Klebaner, 2005). According to D.-U. Lee, Villasenor, Luk, & H.W.Leong (2006), majority of digital methods for generating normal distributed random variables are based on transformations of uniform random variables and the popular methods are Inversion method, Ziggurat method, the Wallace method and the Box Muller method. Wheareas uniform random variables are commonly produced from Linear Feedback Shift Register (LFSR) and Cellular Automata Shift Register (CASR) or the combination of both. It is a challenge to select the most suitable RNG model for the Random WOB algorithm in the computation of the unit cube capacitance to high accuracy in FPGA implementation as there has been so far no publication of RNG hardware design in comparison for unit cube Capacitance.

Supercomputer is expensive while a cluster of PCs requires larger space for system set up and higher amount of the electrical energy consumption which add up to a more expensive front cost. FPGAs are suitable platforms because it is not only the parallel computing, it is also faster in speed and low energy consumption (Pong P. Chu, 2008). On the other hand, random WOB algorithm has the specialty of straightforward computation that does not require any charge density computation at the beginning of the process. Instead of the supercomputer or cluster of PCs, the study focuses on implementing the MC algorithm of random WOB and RNG on FPGA to compute the unit cube capacitance.

1.3 Research Objectives

There are a few studies carried out for the improvement in the equipment chosen and the speed to compute the unit cube capacitance. The following objectives are set to overcome the issues:

a) To study and select the most suitable hardware RNG model for the Random WOB algorithm in the computation of the unit cube capacitance.

b) To propose an FPGA-based design of the unit cube capacitance computation engine based on the Random WOB algorithm.

1.4 Scopes of Works

There are two parts of the research work. Four uniform RNG models were investigated for the feasibility to construct the RNG module and the Random WOB algorithm is integrated with the MC algorithm in model-based design for validation and implementation. The tools used, assumption made and limitation are listed below:

a) Verilog Hardware Description Language (HDL) is used in the hardware design of the RNG module. The seeds or the values for the RNG modules are randomly picked and is not part of this study.

b) The Project Navigator in Xilinx Design Suite 14.7 is applied in the design, logic synthesis, simulation and technology mapping to FPGA. Design of the complete system of the unit cube capacitance computation engine is performed using Xilinx Sysgen that enables the application of Simulink Xilinx blocks.
c) The JMP Software is used for statistical analysis on the random number produced by RNG module.
d) The Avnet S6LX150T development board incorporated with Xilinx Spartan-6 LX 150T FPGA -3 speed grade device in FG676 package is the platform applied for the implementation. Dell model Latitude E6410 laptop is used as host PC to communicate with the development board through Xilinx platform cable universal serial bus II but the communication speed is beyond the scope of this study.
e) The elapse time is based on the total clock cycle of the algorithm complete the computation through the simulation in Xilinx ISim.

1.5 Contribution

The contributions of the study are to produce the accurate computation result of MC algorithm for unit cube capacitance computation and to implement the system on FPGA. In this project, four uniform RNG models were evaluated which are hybrid of 43-bit Line Feedback Shift Register (LFSR) and 37-bit Cellular Automata Shift Register (CASR), dual 43-bit LFSR, single 37-bit CASR and dual 37-bit CASR. Hybrid of 43-bit LFSR and 37-bit CASR uniform RNGs were chosen with combination of Box Muller transform to build the parallel random number RNG.

1.6 Thesis Structure

The thesis is organized into six chapters. Chapter one presents the background of the study, problem statement, the objectives and the research scope followed by the contribution of the research. The chapter is ended with the thesis structure.

Chapter two reviews and discusses the previous methods applied to compute the unit cube capacitance. The Random WOB method and the hardware architecture are interpreted extensively as learning foundation for FPGA implementation. The overview of FPGA and its advantages are explored. It is followed by the relevant literature of the study.

Chapter three presents the overall project flow, the Xilinx FPGA configuration tools, the design process flow and the method to verify the program functionality. The overview of the hardware and brief description is covered here. Besides, the statistical software and the analysis methods to validate the random numbers are also discussed.

Chapter four outlines the proposed hardware design workflow and the individual stage design. The functional and performance verification methods are revealed. The hardware set up and verification are also highlighted here.

In Chapter five, the interpretation of the analysis obtained from the simulation and implementation are summarized. They are the statistical analysis result on the random numbers, functionality and performance verification of the program and the hardware implementation. The result is discussed and compared with previous work.

Chapter six concludes the finding and implication of the work. With the consideration on the limitation that has been experienced in doing this work, there are recommendations provided for future research approach.