DESIGN AND CHARACTERIZATION OF SILICON NANOWIRE TRANSISTOR AND LOGIC NANOWIRE INVERTER CIRCUITS

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DESIGN AND CHARACTERIZATION OF SILICON NANOWIRE TRANSISTOR AND LOGIC NANOWIRE INVERTER CIRCUITS

by

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LIST OF SYMBOLS

C	Capacitance
D	Diameter of nanowire
D_n	Diameter of N-channel SiNWT
D_p	Diameter of P-channel SiNWT
I	current
I_{ds}	Drain to source current
I_{ds1}	drain to source current of driver transistor in logic inverter
I_{ds2}	drain to source current of load transistor in logic inverter
Ii	current at the intersection point
I_{OFF}	OFF Current
I_{ON}	ON current
Ir	load resistance current
K	shifting constant
Kr	shifting constant for R-load inverter circuit
L	length of channel
L_n	length of N-channel SiNWT
L_p	length of P-channel SiNWT
m	slope of line
R	load resistor
T_{ox}	Oxide thickness
V	voltage
V_{dd}	drain DC voltage source
V_{gs}	gate to source voltage
Vi	voltage at the intersection point

V_{in}	input voltage
V_{out}	output voltage
V_{IH}	high input voltages
V_{IL}	low input voltages
V_{OHU}	high output voltages
V_{OLU}	low output voltages
V_x	DC voltage source

LIST OF ABBREVIATIONS

CMOS	Complementary metal oxide semiconductor
CNFET	carbon nanotube field-effect transistor
DG-FET	double-gate field-effect transistor
DIBL	Drain induced barrier lowering
FinFET	fin-shaped field effect transistor
GAA	Gate all around
IC	integrated circuits
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal-Oxide-field-effect transistor
NMOS	N-channel metal oxide semiconductor
NM_H	high-state noise margins
NM_L	low-state noise margins
NW	nanowire
SiNWT	Silicon nanowire transistor
SOI	Silicon on insulator
SS	Subthreshold slope
SWCNT	single-walled carbon nanotube
VLS	Vapor–Liquid–Solid
VLSI	very large scale integration

REKABENTUK DAN PENCIRIAN TRANSISTOR NANOWIRE SILIKON DAN LITAR PENYONGSANG LOGIK NANOWIRE

ABSTRAK

Kekurangan yang paling ketara bagi MOSFET planer adalah kebocoran arus di antara sumber dan salir pada keadaan-tutup (I_{OFF}), yang merupakan masalah kritikal bagi meningkatkan kebolehpercayaan litar. Bagi mengatasi masalah ini beberapa jenis transistor 3D sedang diselidiki termasuk transistor nanowire silicon (SiNWT). Bagi mengoptimumkan dimensi-dimensi, suhu ambien serta orientasi salur dalam rekabentuk SiNWT, simulasi diperlukan bagi pencirian kelakuan SiNWT serta membantu dalam rekabentuk. Satu dekad yang lepas, beberapa penyelidikan telah dijalankan, walau bagaimana pun tertumpu kepada fabrikasi SiNWT sahaja. Oleh itu, dalam kajian ini, dimensi, suhu ambien dan orientasi saluran dimodelkan dan diambil kira untuk menganalisis peningkatan prestasi SiNWT Selanjutnya, untuk mengoptimumkan dimensi, dan voltan-voltan logik bagi rekabentuk litar penyongsang logik, simulasi diperlukan untuk mencirikan had jeda hingar penyongsang logik NW dan membantu membuat keputusan-keputusan rekabentuk. Telah ada beberapa penyelidikan yang hanya tertumpu pada fabrikasi penyongsang logic NW, tanpa menimbangkan pengoptimuman tahap logik dan dimensi mengikut jeda hingar sebagai faktor had yang merupakan satu faktor kritikal dalam penentuan prestasi litar logik, dan kajian ini bertujuan untuk menjadi kajian pertama menunjukkan dimensi pengoptimuman penyongsang logik nanowire. Kajian ini mengandungi dua bahagian utama, bahagian pertama adalah mengenai pencirian transistor silikon dawai-nano dan keduanya mengkaji ciri-ciri penyongsang dawai-nano (NW). Dalam bahagian pertama, objektif kajian ini adalah untuk menentukan kesan dimensi (panjang dan garispusat dawai-nano, serta ketebalan oksida), orientasi

saluran dawai-nano, dan suhu pada ciri-ciri SiNWT. Objektif bahagian kedua kajian ini adalah untuk mengkaji ciri-ciri litar penyongsang-NW (beban rintangan, CMOS, dan NMOS) dengan merekabentuk program MATLAB untuk mengira output dan ciri-ciri arus penyongsang-NW. Kajian ini adalah kerja-kerja penyelidikan pertamanya untuk menunjukkan pengoptimuman dimensi penyongsang-NW. Margin hingar dan voltan lengkokan ciri-ciri pemindahan digunakan sebagai menghadkan faktor dalam pengoptimuman ini. Alat simulasi OMEN dan MuGFET digunakan untuk menghasilkan ciri-ciri keluaran SiNWTs saluran-N dan P. Model MATLAB yang direkabentuk dalam kajian ini menggunakan ciri-ciri keluaran transistor NW sebagai input kepada program MATLAB untuk mengira ciri-ciri statik setiap penyongsang. Keputusan menunjukkan bahawa pengurangan skala yang sesuai merujuk kepada pengurangan dalam semua dimensi dengan faktor skala 0.5 kerana peningkatan besar dalam I_{ON}/I_{OFF} (sehingga $2.5* 10^{10}$) dan mengurangkan dalam SS berhampiran kepada nilai yang sesuai (60 mV/dec.). Cara peminimuman ini cenderung untuk meningkatkan ciri-ciri transistor. Juga, penemuan menunjukkan kesan negatif suhu tinggi semasa operasi penggunaan SiNWTs dalam litar elektronik, kerana nisbah I_{ON}/I_{OFF} akan lebih rendah, DIBL akan lebih tinggi (21 mV/V), dan SS akan juga lebih tinggi (119 mV/dec.) pada suhu yang lebih tinggi (150 ^{o}C). Keputusan menunjukkan ciri-ciri yang bebagi bekenaan kebaikan dan keburukan setiap penyongsang litar; NW-CMOS dan NW-NMOS adalah didapati litar penyongsang yang terbaik berdasarkan tahap logik dan margin hingar. Keputusan kajian penyongsang NW-CMOS menunjukkan pengoptimuman bergantung kepada kedua-dua nisbah dimensi dan tahap voltan digital V_{dd}. Pengoptimuman diameter mendedahkan bahawa apabila V_{dd} meningkat sehingga 3V, nilai di optimumkan D_p/D_n berkurangan ke 2.2. Keputusan pengoptimuman panjang Channel

menunjukkan bahawa apabila V_{dd} meningkat sehingga 3V, nilai di optimumkan penurunan L_n dan L_p/L_n bertambah sehingga 0.351. Nisbah dimensi pengoptimuman menunjukkan bahawa apabila V_{dd} sehingga 3V, nilai optimum k_p/k_n menurun kepada 2.4, dan transistor silikon dawai-nano dengan dimensi yang sesuai (D_p dan L_n yang lebih tinggi dan L_p dan D_n yang lebih rendah) boleh difabrikasikan.

DESIGN AND CHARACTERIZATION OF SILICON NANOWIRE TRANSISTOR AND LOGIC NANOWIRE INVERTER CIRCUITS

ABSTRACT

The most important limitation in planer MOSFETs is current leakage between the source and the drain at the off-state (I_{OFF}), which presents a critical problem in securing circuit reliability. To mitigate this problem, there are new types of transistors with a 3D structure, including silicon nanowire transistors (SiNWT). In order to optimize dimensions, ambient temperature and orientation of channel in SiNWT design, simulation is needed to characterize the behaviour of the SiNWT and help making design decisions. Over the last decade, there have been many researches focused on SiNWTs fabrication fields. However, these researches are all based on fabrication fields. Therefore, in this research, dimensions, ambient temperature and orientation of channel are modelled and taken into account to analyze performance improvement of SiNWT. Furthermore, in order to optimize dimensions, and logic-level voltages of nanowire logic inverters circuits design, simulation is needed to characterize the limits of noise margins of the NW logic inverter and help making design decisions. There have been some proposed researches focused on NW logic inverters fabrication without focusing on optimization of logic levels and dimensions depending on noise margins as a limitation factor which represents a critical factor in the working of logic circuits performance, and this study is intended to be the first research to demonstrate dimensional optimization of nanowire logic inverter. This research contains two main parts, first part on the characterization of silicon nanowire transistor and the second on studying the characteristics of nanowire (NW) inverters. In the first part, the objectives of this study are to determine the effects of dimensions (length and diameter of nanowire, as well as oxide thickness),

orientations of nanowire channels, and temperature on SiNWT characteristics. The second part objectives of this study is to study the characteristics of NW-inverter (resistance load, CMOS, and NMOS) circuits by designing a MATLAB program to calculate output and current characteristics of NW-inverters. This study is the first research work to demonstrate dimensional optimization of NW-inverters. Noise margins and inflection voltage of transfer characteristics are used as limiting factors in this optimization. The OMEN and MuGFET simulation tools were used to produce the output characteristics of N and P-channel SiNWTs. MATLAB model designed in the present study utilized these output characteristics of NW transistors as input to the MATLAB program to calculate the static characteristics of each inverter. The results show that the appropriate scaling minimization refers to the scaling down of all the dimensions with scaling factor 0.5 because of the considerable increase in I_{ON}/I_{OFF} (up to $2.5 * 10^{10}$) and decrease in subthreshold slope (SS) (near to ideal value 60 mV/dec.). This type of minimization tends to improve transistor characteristics. Also, the findings reveal the negative effect of higher working temperature on the use of SiNWTs in electronic circuits, because of the lower I_{ON}/I_{OFF} ratio, higher drain induced barrier lowering DIBL (21 mV/V), and higher SS (119 mV/dec.) at higher temperature (150 ^{o}C). The results show different characteristics for the advantages and disadvantages of each circuit inverter; the NW-CMOS and the NW-NMOS circuits are found to the best circuit inverters based on logic level and noise margins. Results for NW-CMOS inverter indicate that optimization depends on both dimensions ratio and digital voltage level V_{dd}. Diameter optimization reveals that when V_{dd} increases up to 3V, the optimized value of D_p/D_n decreases down to 2.2. Channel length optimization results show that when V_{dd} increases up to 3V, the optimized value of L_n decreases and L_p/L_n increases up to

0.351. Dimension ratio optimization reveals that when V_{dd} increases up to 3V, the optimized value of K_p/K_n decreases down to 2.4, and silicon nanowire transistor with suitable dimensions (higher D_p and L_n with lower L_p and D_n) can be fabricated.

CHAPTER 1

INTRODUCTION

1.1 Nanowires in Electronics

Electronic engineering has played an important role in the cognitive development of human beings in various fields of sciences and, most importantly, in the manufacturing evolution of integrated circuits (ICs). The latter occurred as a result of the revolution in the minimization of transistors, the basic unit of the IC chips, which have emerged in the size of tens of nanometers. The number of transistors in ICs quadrupled every three years with the size of the transistor shrinking to half [1].

Nanowires can be prepared for electronic device applications by either “top-down” approaches using advanced nano-lithographic tools [2-4] or by the synthesis of semiconductor nanowires using “bottom-up” approaches, such as the Vapor–Liquid–Solid (VLS) growth technique [5-7].

A nanowire in electronics engineering is a circular or rectangular cross-sectional nanostructure that has a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. Numerous different types of nanowires exist, including metallic, semiconducting, and insulating, for electronic device applications. All of these types are important. In nanoelectronic research, a semiconducting nanowire is used in active devices, an insulating nanowire is used in nano-capacitors, and a metallic nanowire is used to link nano-components into extremely small circuits.

Nanowires are still under research and experimental fields in laboratories. A number of early studies have shown how nanowires can be used to build the next generation of computing devices [8].

In order to create active electronic devices, an important step is to dope a semiconductor nanowire to create p-type and n-type semiconductors [9]. This process has already been performed on individual nanowires. The second step is to create a p-n junction nanowire-diode, which is the simplest among electronic devices. This process was conducted by either physically crossing a p-type wire over an n-type wire [10] or doping a single wire with different dopants along the length of the wire [11] or radially [12].

By connecting nano-diodes p-n junctions together, building logic gates are possible. Researchers have been able to create logic circuits, such as AND, OR, and NOT gates, from semiconductor nanowire crossings [8, 10]. Hence, semiconductor nanowire crossings will be important to the future of digital computing circuits.

1.2 Problem statements

The high performance of ICs under very large scale integration (VLSI) depends on the capability of the MOSFET and is a core part of VLSI technology. Obtaining high-performance devices depends on the miniaturization of the MOSFET using known scaling methods. The scaling of MOSFET is based on the reduction of dimensions both laterally and vertically. Recent technologies use a planar MOSFET to fabricate IC chips, while the minimization of MOSFETs achieves its scaling limits. When the size of a planar MOSFET scales to nanometer ranges, several limitations emerge, such as threshold voltage (V_T) roll-off and drain-induced-barrier-lowering (DIBL) [1, 13, 14]. The most important limitation is current leakage

between the source and the drain at the off-state (I_{OFF}), which presents a critical problem in securing circuit reliability. To mitigate this problem, new types of transistors with a 3D structure, including silicon nanowire transistors (SiNWT), are being investigated as candidates for future electronic devices. SiNWT can suppress I_{OFF} and can achieve further short-channel operation because its structure is constructed from a thin, wire-shaped silicon channel and because the current between source and drain is such a transistor is effectively controlled by the surrounding gate.

In order to optimize dimensions, ambient temperature and orientation of channel in SiNWT design, simulation is needed to characterize the behavior of the SiNWT and help making design decisions. Over the last decade, there have been many researches focused on SiNWTs fabrication [15-18] with different parameters such as semiconducting materials, insulating materials and various fabrication technologies [3-7] developed to predict the SiNWT performance. However, these researches are all based on fabrication fields. Therefore, in this research dimensions, ambient temperature and orientation of channel are modeled and taken into account to analyze performance improvement of SiNWT.

In the current research, the device characteristics of SiNWTs are examined based on various parameters, such as nanowire type, channel orientation, channel diameter, channel length, concentrations, and ambient temperature effects. Focus has been directed toward the dependence of device performance on the I-V characteristics.

Furthermore, in order to optimize dimensions, and logic-level voltages of nanowire logic inverters circuits design, simulation is needed to characterize the limits of noise margins of the NW logic inverter and help making design decisions. There have been some proposed researches focused on NW logic inverters fabrication [19, 20]

without focusing on optimization of logic levels and dimensions depending on noise margins as a limitation factor which represents a critical factor in the working of logic circuits performance, and this study is intended to be the first research to demonstrate dimensional optimization of nanowire logic inverter.

1.3 Objectives of the Current Research

The present study aims to examine SiNWT characteristics with different parameters depending on simulation tools for SiNWT. The objectives and scope of the current research are as follows:

1. To determine the effects of channel dimensions, channel orientations and ambient temperature on SiNWT characteristics.

2. To study the characteristics of NW-inverter (resistance load, CMOS, and NMOS) basic circuits as an application of SiNWT.

3. To develop a MATLAB program to calculate output and current characteristics of NW-inverters depending on calculated SiNWT output characteristics.

1.4 Research scope and limitations

The scope of the present work is focused on designing and characterization of silicon nanowire transistor and nanowire logic inverters circuits. This research contains two main parts, first part focused on designing and characterization of silicon nanowire transistor and the second on studying and designing nanowire (NW) inverters. In the first part, the research of this study is focused to determine the effects of dimensions (length and diameter of nanowire, as well as oxide thickness), orientations of

nanowire channels, and temperature on SiNWT characteristics. The second part of this study is focused to study the characteristics of NW-inverter (resistance load, CMOS, and NMOS) circuits by designing a MATLAB program to calculate output and current characteristics of NW-inverters. To achieve the aforementioned objectives, the following limitations were conducted:

1. Suitable simulation tool (OMEN or MuGFET) was selected based on SiNWT dimensions.

2. Simulation of SiNWT characteristics using selected parameters.

3. Simulation of the transfer characteristics of NW-Inverter circuits depending on the I-V characteristics of SiNWT.

4. Analysis of the results of SiNWT and NW-inverters simulations.

Based on these steps, a flowchart diagram of the research methodology was drawn and is shown in Figure 1.1. Figure 1.1 illustrate the main steps of research methodology as a flowchart which contains two main parts, the first part is about simulation of SiNWT and the second about simulation of logic nanowire inverters. The simulation of SiNWT depends on simulation tools while the simulation of logic nanowire inverter depends on designed MATLAB program.

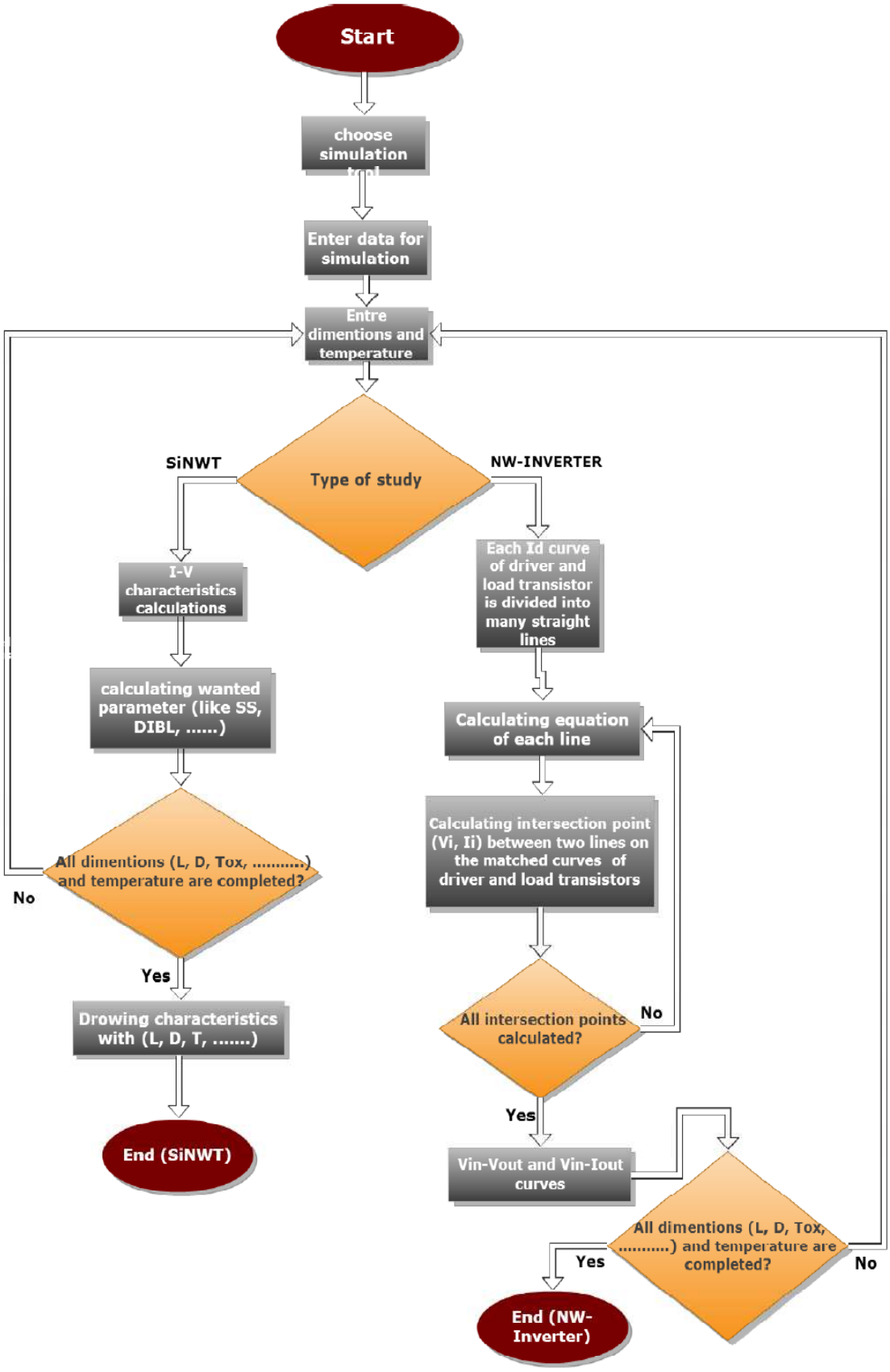


Figure 1.1 Methodology flowchart

1.5 Contribution of the Present Study

Various novel device structures are being extensively explored because the conventional silicon MOSFET has scaling limits. Among these devices is the SiNWT, which has attracted considerable attention from both the semiconductor industry and the academia [1].

Silicon nanowires are remarkably considered by the electronics industry because of the demand for relatively small electronic devices, such as transistors, diodes, resistors, and capacitors. The operation of these future devices and a wide array of additional applications [8] will depend on the properties of the fabricated nanowires, whereas the outcome of the present study is important in the investigation and understanding of the dependence of SiNWT characteristics on these properties. A new generation of ultra-small transistors and more powerful computer chips using tiny structures called semiconducting nanowires will be more applicable in the future after further research and discoveries [21]. The fabrication of NW-FETs is still a developing technology that requires further innovations before challenging the state-of-the-art MOSFETs.

Simulation is necessary to understand the mechanism of the device and to evaluate the performance limits of SiNWTs. Simulation tools can support the experimental work to accelerate the development of NW FETs [22], to reduce costs, and to identify strengths and weaknesses, as well as demonstrate the scalability of these materials down to the nm range [23-25].

1.6 Thesis organization

In this thesis, the device characterization of SiNWT and its application as a NW-inverter were addressed. The purpose of the characterization of SiNWT is to define the strengths and weaknesses in transistor characteristics because the SiNWT structure is the best transistor instead of a normal MOSFET structure with nano-version. The importance of the characterization of SiNWTs will improve our understanding of this future device.

The literature review on SiNWTs and NW-inverters is presented in Chapter 2. The literature review is concentrated on scaling down of the MOSFET and its limitations, as well as the need to overcome such limitations by inventing new structures, such as the SiNWT.

In Chapter 3, the methodology of the research with theoretical background is addressed. In this chapter, the instruments, procedures, and theoretical basis of the research were presented.

Chapter 4 focuses on the results and discussion. The results of the SiNWT characterization are concentrated on the effects of dimensions and temperature on the key parameters of transistors. Meanwhile, the results of the NW-inverter characterization are concentrated on the noise margin change with the dimensions of transistors.

Chapter 5 summarizes the results of this study and provides suggestions for future research directions.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, the literature review related to the research is presented. The aim of this chapter is to provide theories, information and previous work about certain related topics.

2.2 Nano-transistors

Complementary metal–oxide–semiconductor (CMOS) technology has led to the steady minimization of transistors with each new generation, thereby yielding continuous improvements in transistor performance. However, the International Technology Roadmap for Semiconductors (ITRS) had indicated that the scaling of gate transistor lengths to sub-22 nm levels could yield several serious problems, such as high sub-threshold leakages, short-channel effects, device-to device variations, and so on [26]. Several studies have attempted to overcome these problems by designing new transistor structures, such as the double-gate field-effect transistor (DG-FET), fin-shaped field effect transistor (FinFET), carbon nanotube transistor (CNT), and silicon nanowire field-effect transistor (SiNWT).

Planar DG-FETs are shown in Figure 2.1. This structure contains two gates, top and bottom, that control the channel. The DG-FET provides better control of the short-channel effects, lowers leakage, and provides better yield in aggressively scaled traditional CMOS technology [27].

To overcome the difficulty of aligning the two gates, a special type of DG-FET, known as the FinFET, is used. FinFETs are relatively easy to manufacture and feature no alignment problems that plague many other DG-FET structures. Furthermore, the use of a lightly doped channel in FinFETs allows them to become resistant to random dopant variations [26].

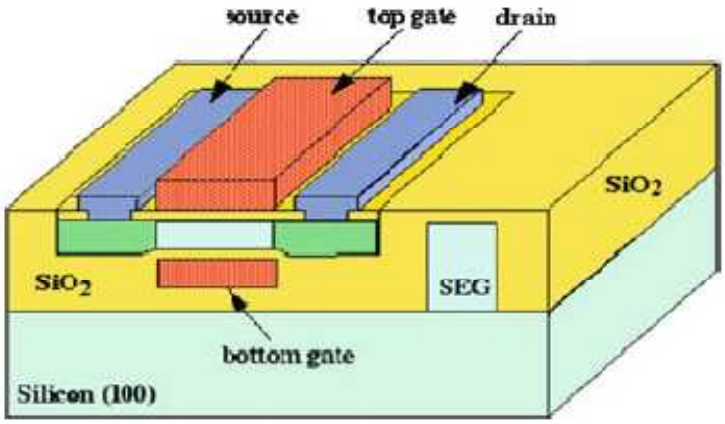


Figure 2.1 DG-FET structure [26].

Figure 2.2 shows the FinFET structure. A FinFET is a FET in which the channel is made to stand up and turn on its edge. As shown in Figure 2.3, the two gates of a FinFET can be made independently controllable by etching away its top part.

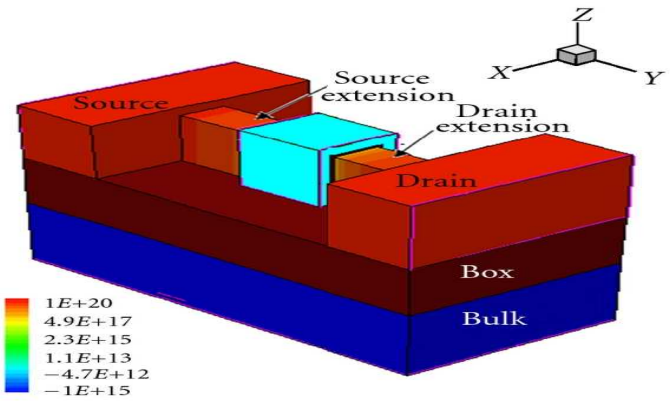


Figure 2.2 Fin-FET structure [28].

The two most promising replacements for silicon in future transistor channels are CNTs [29] and graphene. Carbon nanomaterials in their semiconducting forms exhibit room-temperature mobilities of over tenfold higher than that of silicon. This feature provides transistors with significant improvements in power and performance and allows higher integration at the same power density. In addition, carbon-based materials can be scaled to feature sizes smaller than those provided by silicon-based materials while maintaining favorable electrical properties. As shown in Figure 2.4, CNTs can be divided into two groups: single-walled carbon nanotubes (SWCNTs) and multi-walled carbon nanotubes. Semiconducting SWCNTs have characteristics that are ideal for use in FETs. Previous studies have indicated that single CNFET devices can be 13 and 6 times faster than pMOS and nMOS transistors, respectively, at similar gate lengths [26].

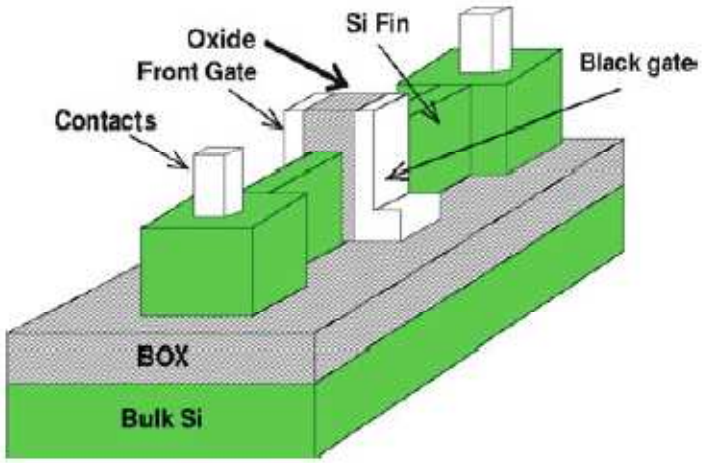


Figure 2.3 Fin-FET with double gate [26].

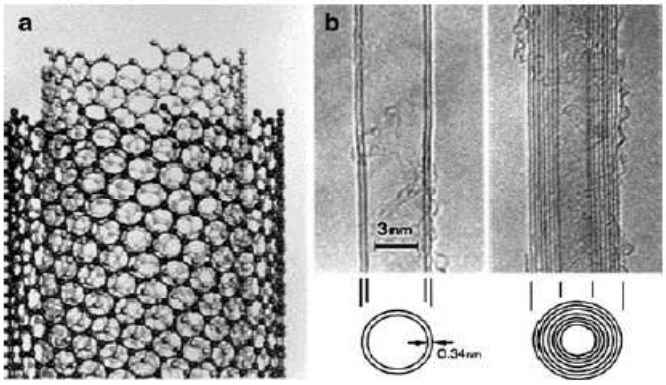


Figure 2.4 Multiwalled CNT [29].

In 1998, IBM [30] and the Delft University of Technology [31] first created operational room-temperature CNFETs. The structures of the transistor of the CNFETs are shown in Figure 2.5. These structures have similar architectures: a single nanotube acts as the channel region and puts on metal source/drain electrodes. Both designs use SiO_2 as a dielectric on top of a silicon back-gate. Au or Pt contacts are used as source/drain electrodes because their functions are close to the CNT function for improving transistor speed [26].

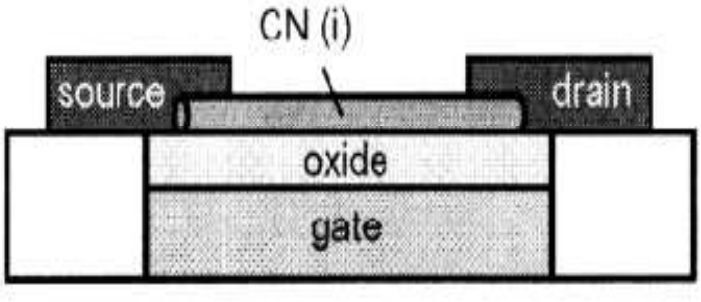


Figure 2.5 The structures of the transistor of the CNFETs [32]

A nanowire is a nanostructure with a diameter constrained to tens of nanometers or less and an unconstrained length. Many types of nanowires exist, including metallic (Ni or Au), semiconducting (silicon), and insulating (SiO_2) nanowires.

SiNWTs represent a promising alternative to conventional CMOS devices at the end of the ITRS because of the improved electrostatic control of the channel via the gate voltage and the consequent suppression of short-channel effects. The first step to creating active electronic elements is chemical doping of a semiconductor nanowire. This step has already been performed on individual nanowires to create p-type and n-type semiconductors.

SiNWTs can strongly reduce the impact of off-leakage currents because their thin wire-shaped silicon channels (nanowire channels) are effectively controlled by the surrounding gate. Toshiba developed a 16 nm SiNWT using multi-nanowire channels. The ON-current is improved by optimizing gate fabrication and reducing the thickness of the gate sidewall. A schematic of the device is shown in Figure 2.6 [33].

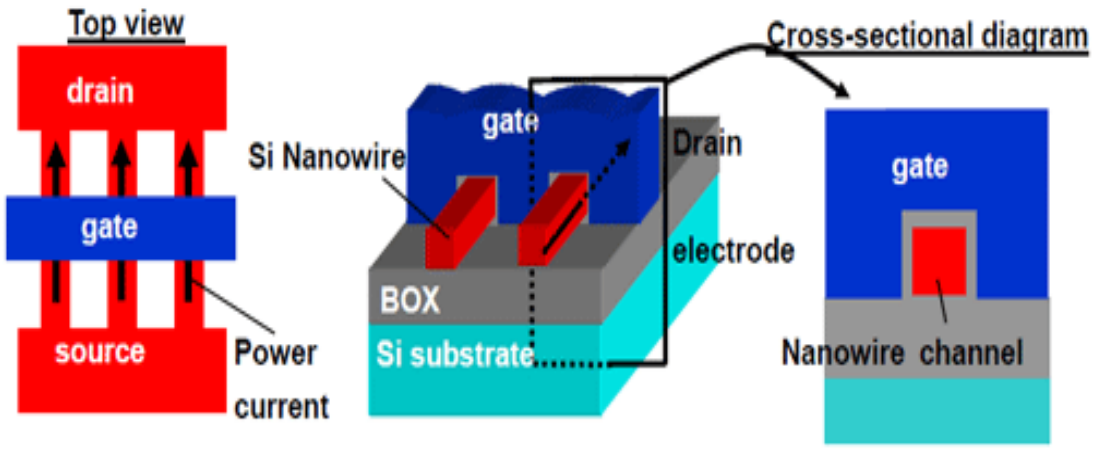


Figure 2.6 SiNWT using multi-nanowire channels [33]

Recent studies have developed a junction-less nanowire transistor [34]. Figure 2.7 shows the design of an N-channel SiNWT. The buried oxide, which is considered the underlying insulator layer, is not shown. The doping concentration in the channel is identical to that in the source and drain. In a normal tri-gate SiNWT, the source and drain regions are heavily doped n-type materials and the channel region under the gate is a lightly doped p-type material. In the junction-less gated resistor, the silicon nanowire is a uniformly doped n-type material and the gate material is a p-type polysilicon [26].

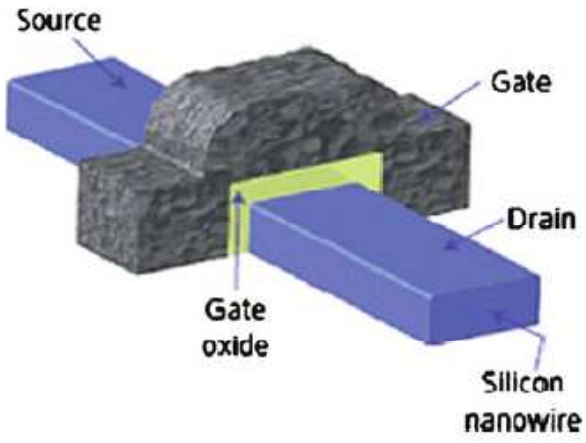


Figure 2.7 The design of an N-channel SiNWT [34]

2.3 Scaling down of MOSFET and its limitations

Moore's law [35] states that every three years, the quadrupling of the number of devices in a chip is similar with the doubling of transistor performance. The great progress has been achieved through scaling down the MOSFETs from larger transistor dimensions to smaller transistor dimensions, leading to increased speed and density.

Scaling down the conventional MOSFET beyond the 50 nm length of channel requires innovations to circumvent barriers because of the fundamental physics that constrains the conventional MOSFET. The limitations of scaling down MOSFETs [36-41] are as follows:

1) Increasing of gate leakage current because of the quantum-mechanical tunnelling of carriers through the thin gate oxide.

2) Increasing I_{OFF} because of the quantum-mechanical tunnelling of carriers from the drain to the body, and from the source to the drain of the MOSFET.

3) Lower I_{ON}/I_{OFF} ratio because of the lower control of the density and location of dopant atoms in the MOSFET channel and source/drain region to provide a high on-off current ratio.

4) Lowering of subthreshold slope.

These limitations led to the predictions of the end of technological progress for the semiconductor industry [35].

The figure of merit for MOSFETs in digital circuits for unloaded circuits is *CV/I*, where *C, V,* and *I* are the gate capacitance, voltage swing, and current drive of the transistor, respectively. The current drive of the MOSFET is important for loaded circuits. Scaling the MOSFET channel length improves circuit speed [36-41]. The off-current specification for CMOS has been rising rapidly to keep the speed performance high. However, this trend in planer MOSFETs cannot continue because the on-current increases only linearly as off-current increases exponentially. Thus, the means to reduce the standby power increase must be found [36-41].

Meanwhile, the decreasing physical thickness of the dielectric gate tends to exponentially grow in the direct tunnelling current through the dielectric gate [42]. The increase of gate tunnelling current has significantly impacts the standby power of the IC and limits the reduction of the physical thickness of the dielectric gate. According to [43], the tunnelling currents arising from (SiO_2), which are thinner than 0.8 nm, cannot be tolerated even in high-performance systems. Solutions have been explored through the introduction of new dielectrics with high dielectric-constant to reduce the gate tunnelling current and gate capacitance degradation caused by polysilicon depletion. The benefits of using high dielectric constant insulators instead of SiO_2 for the same electrical thickness are limited because of the presence of two-

dimensional electric fringing fields from the drain through the physically thicker gate dielectric[36].

The drain fringing field lowers the potential barrier in the source-to-channel region and the V_T in a way similar to the well-known drain-induced barrier lowering (DIBL), in which the drain field modulates the source to the channel potential barrier via coupling through the Si substrate. Therefore, the use of higher *k* insulators must be combined with an agreeable reduction of the electrical thickness [36].

2.4 Silicon nanowire transistors (SiNWT)

The performance of MOSFETs has degraded over the last years because of their uneasy scaling. One of their important figures of merit is the subthreshold swing (SS), which is defined as the change in gate voltage (V_g) required for a change of an order of magnitude of current from the off to on state [44]. The SS of a MOSFET is controlled by the thermionic emission-carrier diffusion over a thermal barrier, and has a minimum value of 60 mV/decade at room temperature [44]. Thus, further scaling down of MOSFET is very difficult without a significant increase in the I_{OFF}. For the future ICs, ultra low-power and energy-efficient transistors with acceptable SS are needed [39].

SiNWT is a nano-modified version of the planer MOSFET, SiNWT structure is illustrated in Figure 2.8 a [45]. Researchers concentrated in inventing new structures of the MOSFET after overcoming the limitations of planer MOSFETs. Semiconductor nanowires serve as one of the most powerful platforms available today in nanoelectronics, given that it is now possible to design device structures. Silicon nanowires (SiNWs) are attracting significant attention from the electronics industry because of the drive for smaller electronic devices, such as transistors,

diodes, resistors, and capacitors. The operation of these new nano-electronic devices and a wide array of its applications will depend on the properties of the nanowire dimensions. A new generation of ultra small transistors and more powerful computer chips using tiny structures called semiconducting nanowires will be more applicable in the future after more discoveries by researchers.

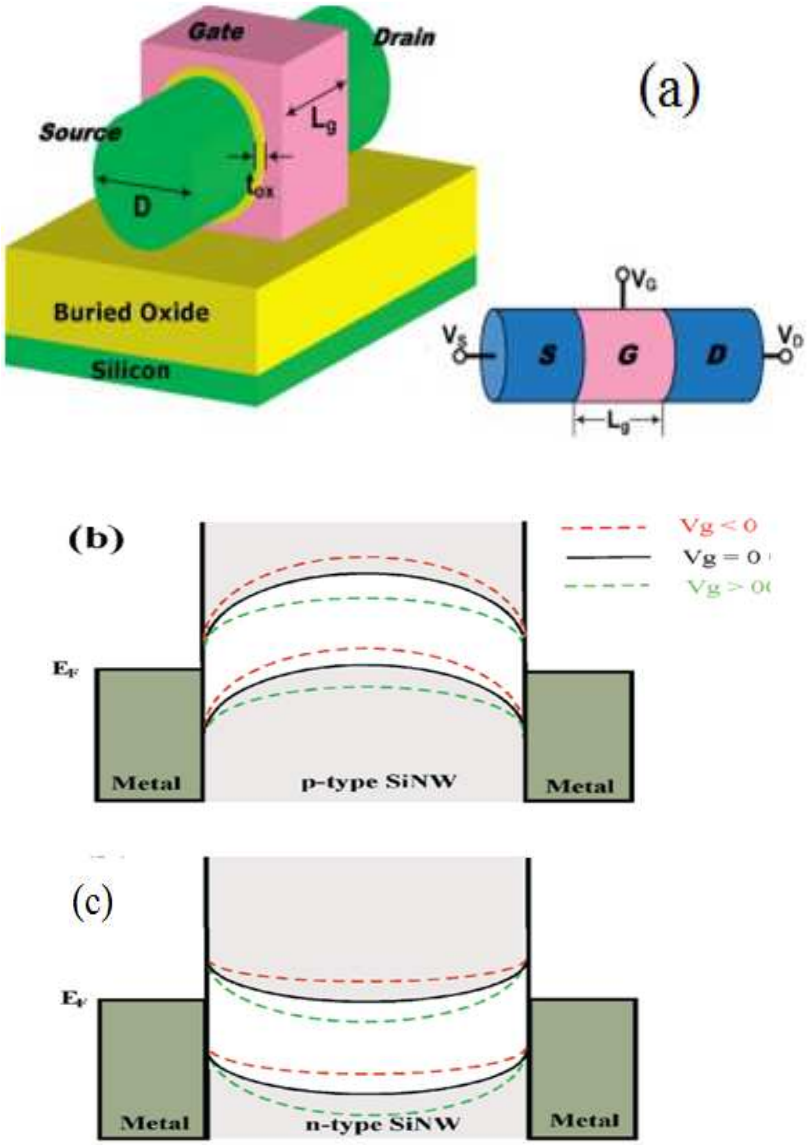


Figure 2.8 (a) SiNWT structure [45]. Energy band diagrams for (b) p-type SiNW (c) n-type SiNW devices. [46]

Cui et al. [46] was the first group that studied the possibility to build FET transistors using a single-crystal n-type and a p-type SiNWs. The successful doping of SiNWs to create n-type and p-type materials opened up exciting opportunities in nanoscience and nanotechnology. The structural studies in [46] are the first SiNWTs (shown in Figure 2.8 b and c), and it is possible to apply them in nanoelectronics. The researchers also suggested that using a combined p-type and n-type SiNWs in crossed arrays to create p-n junctions may also be considered for devices and sensors.

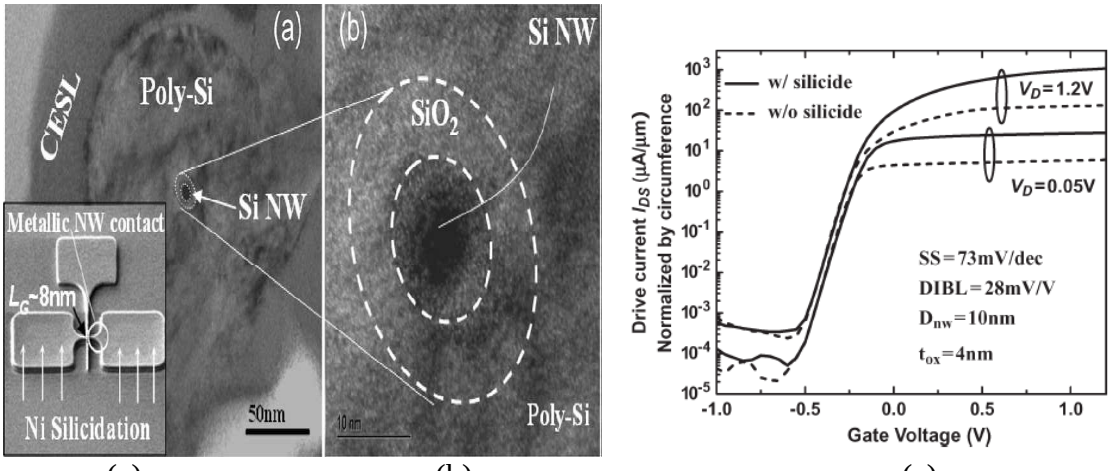
Tan et al. [47] fabricated a high-performance gate-all-around (GAA) vertical structure of SiNWT high I_{ON}/I_{OFF} ratio, near-ideal SS (~60 mV/decade), and low DIBL (~10 mV/V) characteristics. The improvements in the performance are due to the superior gate control of the GAA structure and the Schottky barrier thinning in a scaled nanosized metal-semiconductor junction [47].

Ghandi et al. [44] studied a new structure of SiNWTs using a CMOS-compatible vertical gate-all-around structure, from which excellent characteristics were obtained. For the first time, the lowest subthreshold swing (SS), with 30 mV/decade at room temperature and low drain voltage, was demonstrated. A very convincing SS of 50 mV/decade for almost three decades of drain current was also reported. Moreover, this device exhibits excellent characteristics without ambipolar behavior and with high I_{ON}/I_{OFF} ratio (~ 10^5), as well as a low drain-induced barrier lowering of ~70 mV/V.

Cui et al. [48] made a direct comparison of the key parameters. The SiNWT results have been scaled using the Si on the insulator FET with a gate length of 50 nm and gate oxide thickness of 1.5 nm. Significantly, the scale (I_{ON}) for the SiNWT is larger

than the MOSFET. The average subthreshold slope (SS) approaches its theoretical limit (60) and the average transconductance is 10 times larger. These improvements may lead to substantial benefits for high-speed and high-gain devices. The SiNWT also have larger leakage currents; however, this issue may be overcome by implementing the source and drain contacts as in planer MOSFETs. The comparison of these results and other key parameters with planar silicon devices shows substantial advantages for the SiNWs as building blocks.

Jiang et al. [49] demonstrated the successful integration of GAA SiNWT with low resistance metallic source/drain contacts. The ultrascaled SiNWT with NWs that have diameter of 10 nm, 4 nm SiO_2, and gate lengths down to 8 nm have been achieved in this research (Figure 2.9), exhibiting good performance among the NW FETs reported on that date. Compared with other reference devices, the metallic contact SiNWT showed 58% enhancement in I_{ON} from 103 μA/μm to 705 μA/μm, at a fixed I_{OFF} of 10 nA/μm. The SS is 73 mV/dec and DIBL is 28 mV/V. The significant drive current enhancement was achieved in this research



-(a)- -(b)- -(c)-

Figure 2.9 (a) GAA SiNWT structure. (b) NW diameter is 10 nm with 4-nm SiO_2. (c) Transfer characteristics for SiNW devices with and without metallic NW contacts. [49]

Yang et al. [50] fabricated SiNWTs as a vertical structure, with good electrical characteristics that used low cost bulk wafers. This structure with simple gate definition process steps may make this device a suitable candidate for the next generation technology nodes. They present a vertical GAA SiNWT on Si wafer with fully CMOS compatible technology. In this research, vertical nanowires with a diameter of ~20 nm were achieved from the lithography and dry-etch defined Si-pillars with subsequent oxidation. The N-channel SiNWTs fabricated with a gate length of ~150 nm showed excellent transistor characteristics with a large drive current (1.0×10^3 μA/μm), high on/off current ratio (~10^7), good SS (~80 mV/dec), and low DIBL (~10 mV/V) (Figure 2.10) [50].

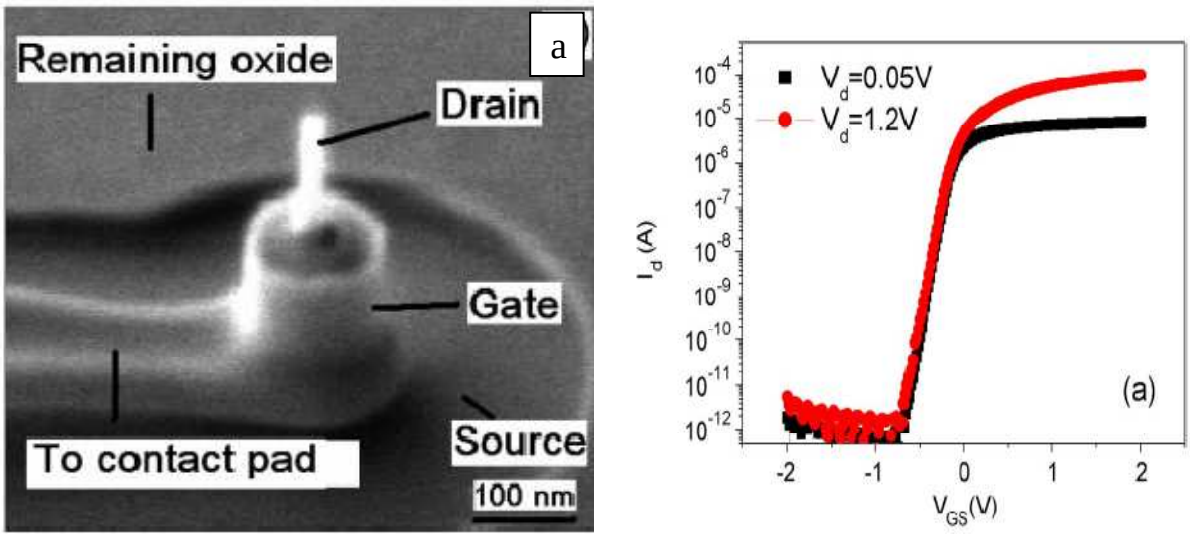


Figure 2.10 (a) Structure of vertical GAA SiNWT. (b) Id-Vg characteristics of vertical GAA SiNWT [50].

2.5 Nanowire Logic Inverter

According to the importance of nano-scale devices and challenges in developing technologies, there is a strong need for evaluating circuit performance with NW structures architecture, including digital circuits such as the CMOS inverter.

Cui and Liber [19] carried out preliminary experiments to explore CMOS inverter-like structures depending on SiNWTs as load and driver transistors (Figure 2.11). The lightly doped p- and n-type SiNWs used in the inverters showed that large gate effects may be completely depleted (Figure 2.11 B). The output voltage from the device (V_{out}) varied from negative (high) to zero, whereas the input gate voltage (V_{in}) varied from positive to negative; that is, the signal is inverted. The calculation of voltage gain is 0.13 from the slope of transfer characteristics. As they suggested, the low gain exhibited by this initial NW-CMOS inverter may be improved by preparing SiNWs that switch on and off at lower voltages. Nevertheless, this first NW-CMOS inverter still exhibits the low static power dissipation expected of a CMOS inverter structure; that is, this inverter has a static dissipation of 0.5 nW to 5 nW in either high or low states, whereas a single Si nanowire CMOS has a power dissipation which is 10^3 to 10^4 times larger.

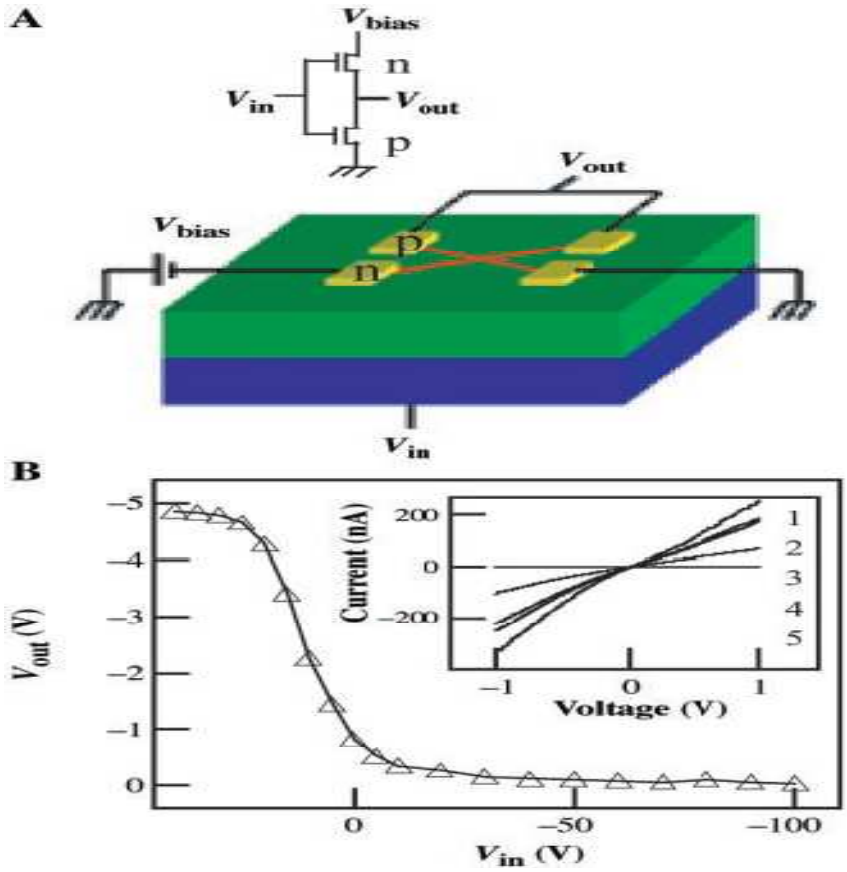


Figure 2.11 CMOS inverter-like structures [19].

Buddharaju et al. [20] presented, for the first time, the GAA SiNWT into the CMOS logic inverter. The on currents for the N-channel and P-channel transistors are matched using different number of channels for each transistor to obtain symmetric pull-up and pull-down characteristics. High voltage gains with sharp on-off transitions are obtained, which are best reported among the nanowire and carbon nanotube inverters. The inverters maintain their good noise margins for a wide range of V_{DD} values. The short circuit current at 0.2 V V_{DD} is ~6 pA, indicating the excellent potential of these devices for low voltage and ultra low power applications. These findings resulted to the best reported nanowire and FinFET inverters.

Maheshwaram et al. [51] studied and simulated the NW-CMOS inverter with a vertical structure using TCAD. In the present study, different vertical NW-CMOS inverter configurations were investigated. The static and dynamic characteristics show excellent performance with an improvement in speed and a significant saving in area and power consumption. The researchers compared the planar and FinFET technologies. The two-wire vertical inverter (TWVI) has a lower delay than the single-wire vertical inverter (SWVI) configuration because of the lower series resistance (shown in Figure 2.12).

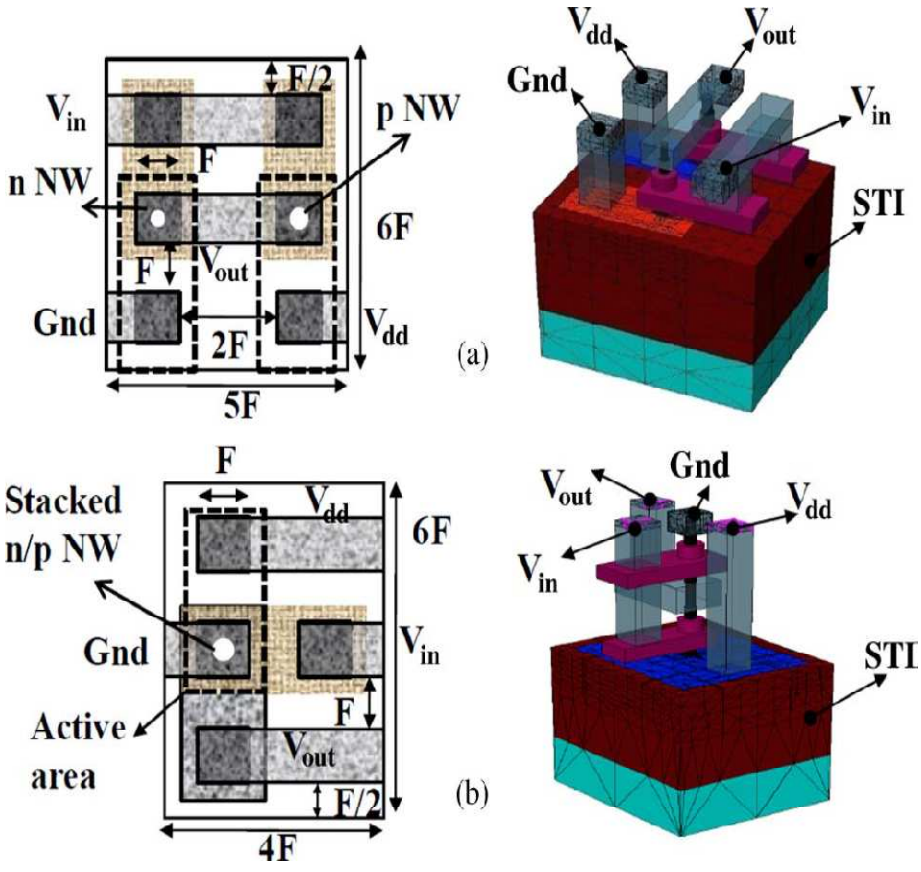


Figure 2.12 Typical layout and structure of (a) the TWVI and (b) the SWVI [51].