INVESTIGATION OF SIMULTANEOUS THERMAL OXIDATION AND NITRIDATION OF SPUTTERED ZIRCONIUM ON SILICON AND SILICON CARBIDE IN NITROUS OXIDE GAS ENVIRONMENT

WONG YEW HOONG

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by

WONG YEW HOONG

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Doctor of Philosophy

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Tandatangan Calon / *Signature of Candidate*

Nama Calon / *Name of Candidate*

WONG YEW HOONG

Tarikh / *Date*

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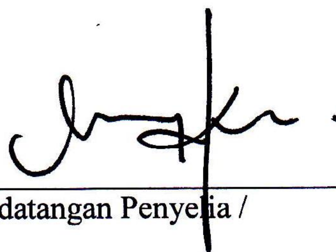

Tandatangan Penyelia / *Signature of Supervisor*

Nama Penyelia & Cop Rasmi / *Name of Supervisor & Official Stamp*

ASSOC. PROF. IR. DR. CHEONG KUAN YEW
Universiti Sains Malaysia
Engineering Campus
School of Materials & Mineral Resources Engineering
14300 Nibong Tebal,
Penang, Malaysia.
E-mail: cheong@eng.usm.my

Tarikh / *Date*

18 MAY 2012

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TABLE OF CONTENTS

		Page
ACKNOWLEDGEMENTS		ii
TABLE OF CONTENTS		iv
LIST OF TABLES		x
LIST OF FIGURES		xi
SELECTED LIST OF ABBREVIATIONS		xx
SELECTED LIST OF SYMBOLS		xxi
LIST OF PUBLICATIONS		xxiii
ABSTRAK		xxv
ABSTRACT		xxvi
CHAPTER 1: INTRODUCTION		
1.1	Theoretical Background	1
1.2	Problem Statement	2
1.3	Research Objectives	8
1.4	Scope of Study	8
1.5	Thesis Outline	9
CHAPTER 2: LITERATURE REVIEW		
2.1	Introduction	10
2.2	SiC as Alternative Substrate for Si	11
2.3	Comparison of Si and Polytypes of SiC	12
2.4	Metal-Oxide-Semiconductor (MOS) Structure and Device Fundamentals	15

2.3.1 MOS Structure 15
2.3.2 Influence of Applied Bias 16
2.5 Gate Oxide on Si 17
2.6 Gate Oxide on SiC 20
2.7 ZrO_2 as Alternative High-κ Gate Dielectric 22
2.6.1 Electrical Properties of ZrO_2: Dielectric Constant (κ) Value and Band Offsets 22
2.6.2 Material and Structural Properties of ZrO_2 25
2.6.2.1 Thermodynamic and Kinetic Stability of ZrO_2 in contact with Si 25
2.6.2.2 Interfacial Quality of ZrO_2/Si 30
2.8 ZrO_2 Thin Films Deposition 33
2.7.1 Thermal Evaporation 34
2.7.2 Electron Beam Evaporation (EBE) 35
2.7.3 Pulsed Laser Deposition (PLD) 36
2.7.4 Cathodic Arc Deposition 39
2.7.5 Atomic Layer Deposition (ALD) 40
2.7.6 Metalorganic Chemical Vapour Deposition (MOCVD) 42
2.7.7 Sputtering 43
2.9 Oxidation Mechanism of Si 46
2.10 Oxidation Mechanism of Zr 48
2.11 Oxidation of Sputtered Zr on Si 50
2.12 Nitridation Process 53
2.13 ZrO_2 Thin Films on SiC Substrate 55
2.14 Role of Nitrogen in Gate Oxides on Si and SiC Substrates 56

CHAPTER 3: MATERIALS AND METHODOLOGY

3.1	Introduction	59
3.2	Materials	63
	3.2.1 Substrate Materials	63
	3.2.2 Materials for Substrate Cleaning and Quartz Tube Cleaning	63
	3.2.3 Materials for Sputtering	64
	3.2.4 Materials for Oxidation/Nitridation Process	64
	3.2.5 Materials for Metallization and Photolithography Process	64
3.3	Experimental Procedures	66
	3.3.1 Substrate Cleaning Process	66
	3.3.2 Sputtering Process	68
	3.3.3 Simultaneous Oxidation/Nitridation Process	69
	3.3.4 Metallization and Photolithography Processes	72
3.4	Characterizations Techniques	75
	3.4.1 XPS Measurements	75
	3.4.2 EFTEM Analysis	76
	3.4.3 XRD Analysis	77
	3.4.4 Raman Analysis	78
	3.4.5 FTIR Analysis	79
	3.4.6 AFM Analysis	79
	3.4.7 High Frequency *C-V* Measurement	80
	3.4.8 *I-V* Measurement	81

CHAPTER 4: RESULTS AND DISCUSSION:
SILICON-BASED SUBSTRATE

4.1 Introduction 82

4.2 Effects of Oxidation/Nitridation Durations on Sputtered Zr Based on Si Substrate 82

4.2.1 Structural and Chemical Properties 83

4.2.1.1 XPS Measurements 83

4.2.1.2 Band Alignment 93

4.2.1.3 EFTEM Analysis 98

4.2.1.4 XRD Analysis 101

4.2.1.5 Raman Spectroscopy 102

4.2.1.6 FTIR Analysis 103

4.2.1.7 Oxidation and Nitridation Mechanisms 105

4.2.2 Electrical Properties 112

4.2.2.1 *C-V* Measurements 112

4.2.2.2 *J-E* Characteristics 120

4.2.3 Summary 127

4.3 Effects of Oxidation/Nitridation Temperatures on Sputtered Zr Based on Si Substrate 128

4.3.1 Electrical Properties 128

4.3.1.1 *C-V* Measurements 128

4.3.1.2 *J-E* Characteristics 133

4.3.2 Summary 135

CHAPTER 5: RESULTS AND DISCUSSION:

SILICON CARBIDE-BASED SUBSTRATE

5.1 Introduction 137

5.2 Effects of Oxidation/Nitridation Temperatures on Sputtered Zr Based on SiC Substrate 137

5.2.1 Structural and Chemical Properties 137

5.2.1.1 XPS Measurements 137

5.2.1.2 Band Alignment 148

5.2.1.3 Oxidation and Nitridation Mechanisms 152

5.2.1.4 EFTEM Analysis 157

5.2.1.5 XRD Analysis 161

5.2.1.6 Raman Spectroscopy 162

5.2.1.7 AFM Analysis 163

5.2.2 Electrical Properties 166

5.2.2.1 *C-V* Measurements 166

5.2.2.2 *J-E* Characteristics 170

5.2.3 Summary 174

5.3 Comparison of Oxidation/Nitridation of Sputtered Zr Based on Si and SiC substrates in 100% N_2O 176

5.3.1 Structural and Chemical Properties 176

5.3.2 Electrical Properties 178

5.3.3 Summary 179

5.4 Oxidation/Nitridation of Sputtered Zr Based on SiC Substrate in Diluted N_2O 180

5.4.1 Structural and Chemical Properties 180

5.4.1.1 XPS Measurements 180

5.4.1.2 Band Alignment 191

5.4.1.3 EFTEM Analysis 194

5.4.1.4 XRD Analysis 197

5.4.1.5 Raman Spectroscopy 202

5.4.1.6 AFM Analysis 203

5.4.2 Electrical Properties 206

5.4.2.1 *C-V* Measurements 206

5.4.2.2 *J-E* Characteristics 212

5.4.3 Summary 217

CHAPTER 6: CONCLUSION AND FUTURE RECOMMENDATIONS

6.1 Conclusion 218

6.1.1 Effects of Oxidation/Nitridation Durations and Temperatures on Sputtered Zr Thin Films on Si Substrate 219

6.1.2 Oxidation/Nitridation Temperatures and Concentrations of N_2O Gas on Sputtered Zr Thin Films on SiC Substrate 220

6.1.3 Comparison of Oxidized/Nitrided Sputtered Zr Thin Films on Si and SiC Substrates 222

6.2 Recommendations For Future Research 222

REFERENCES 224

LIST OF TABLES

		Page
2.1	Comparison of the properties of Si and selected polytypes of SiC at room temperature.	14
2.2	Differences between thermodynamic and kinetic.	25
2.3	Calculated Gibbs energy (ΔG^0) changes in kJ/mol for ZrO_2 in contact with Si at T = 727˚C.	28
2.4	Various thermodynamically stable temperatures for ZrO_2/Si reported.	29
2.5	Summary of ZrO_2 thin film quality fabricated by PLD technique.	38
2.6	Summary of the characteristics of ZrO_2 thin films deposited by cathodic arc deposition technique.	39
3.1	List of chemicals for substrate cleaning and quartz tube cleaning.	63
3.2	List of materials and chemicals for sputtering process.	64
3.3	Gases employed in oxidation process.	65
3.4	Materials for metallization and photolithography process.	65
3.5	Step by step cleaning process.	66
4.1	Possible compounds in the interfacial layers of the investigated samples (oxidation and nitridation was at 700°C in N_2O).	91
4.2	Comparison of the obtained values of $E_{g(ZrO_2)}$, $E_{g(IL)}$, ΔE_v, and ΔE_c in this work with the literatures.	94
5.1	Possible compounds in the substrate, interfacial layer, and bulk of the investigated samples (oxidation and nitridation time was 15 min in N_2O).	147
5.2	Optimized parameters of simultaneous oxidation and nitridation of sputtered Zr on different semiconductor substrates of Si and SiC in 100% N_2O.	176
5.3	Comparison of structural and chemical properties of oxidized/nitrided sputtered Zr based on Si and SiC substrates.	177
5.4	Comparison of electrical properties of oxidized/nitrided sputtered Zr based on Si and SiC substrates.	179
5.5	Possible compounds in the substrate, interfacial layer, and bulk of the investigated samples (oxidation and nitridation was at 700°C and 15 min).	191

LIST OF FIGURES

Page

2.1 The basic component of Si-C-bilayer for the formation of polytypes. 13

2.2 Schematic diagram of MOS structure capacitor. 15

2.3 Energy-band diagrams for ideal MOS capacitors of n-type and p-type under various bias conditions: (a) accumulation, (b) depletion, and (c) inversion. 17

2.4 Comparison of *J-E* characteristics of various metal/high-κ gate oxide/4H-SiC MOS capacitors reported in the literature. 21

2.5 Simple schematic of bandgap and band offsets of ZrO_2 and carrier injection mechanism (red dotted lines) in its band states. CB = Conduction Band, VB = Valence Band. 24

2.6 Ternary phase diagrams for Zr-Si-O compounds at 727˚C. 27

2.7 Interfacial bonding of ZrO_2 with Si(100). (a) Polar unit of $O^{2-}O^{2-}Zr^{4+}O^{2-}$ bonds with two neighbouring Si forms Si-O-Si bridge. (b) Polar unit of $Zr^{4+}O^{2-}$ bonds with Si satisfies the valence requirement. 32

2.8 Simple model for thermal oxidation of silicon: 1. Transportation of oxidizing gas bulk to the outer surface where it reacts or is adsorbed. 2. Transportation of oxygen across the oxide film towards the silicon. 3. Reaction at the silicon surface to form a new layer of SiO_2. 47

2.9 (a) The total oxide-film growth thickness (d_{total}), (b) stoichiometric ZrO_2 films top (d_{ZrO2}), and (c) the relative Zr-enriched bottom ($d_{interface\ oxide}$), as a function of oxidation time at various temperatures (373 K–573 K). 49

2.10 Oxidation curves of Zr/Si structures at (1) 473, (2) 498, (3) 523, (4) 573, (5) 598, (6) 623, (7) 673 K in a reactor mounted in a resistance furnace. 51

3.1 An overview of research methodology. 61

3.2 An overview on characterization techniques used in this work. 62

3.3 Working chamber of RF sputtering system employed in this work. 69

3.4 Set up for oxidation process. 71

3.5 Configuration of thermal evaporator chamber. 72

3.6 Overview process of metallization (front and back contact) and photolithography. 74

4.1 Atomic percentage of Zr, Si, O, and N as a function of etching time for different oxidation/nitridation duration samples: (a) 5 min, (b) 10 min, (c) 15 min, (d) 20 min (oxidation and nitridation was at $700^{o}C$ in N_2O). 84

4.2 Evolution of Zr 3*d* core level XPS spectra as a function of etching time for different oxidation/nitridation duration samples: (a) 5 min, (b) 10 min, (c) 15 min, and (d) 20 min (oxidation and nitridation was at $700^{o}C$ in N_2O). 88

4.3 Evolution of Si 2*p* core level XPS spectra as a function of etching time for different oxidation/nitridation duration samples: (a) 5 min, (b) 10 min, (c) 15 min, and (d) 20 min (oxidation and nitridation was at $700^{o}C$ in N_2O). 89

4.4 Evolution of O 1*s* core level XPS spectra as a function of etching time for different oxidation/nitridation duration samples: (a) 5 min, (b) 10 min, (c) 15 min, and (d) 20 min (oxidation and nitridation was at $700^{o}C$ in N_2O). 90

4.5 Evolution of N 1*s* core level XPS spectra as a function of etching time for different oxidation/nitridation duration samples: (a) 5 min, (b) 10 min, (c) 15 min, and (d) 20 min (oxidation and nitridation was at $700^{o}C$ in N_2O). 92

4.6 (a) XPS valence band spectra of ZrO_2 and IL for all investigated samples. (b) XPS O 1*s* plasmon loss spectra of ZrO_2 and IL for 15-min sample. 95

4.7 The calculated values of $E_{g(ZrO_2)}$, $E_{g(IL)}$, $\Delta E_{c(ZrO_2/Si)}$, $\Delta E_{c(IL/Si)}$, and $\Delta E_{c(ZrO_2/IL)}$ in the band alignment of ZrO_2/IL/Si system. 96

4.8 Band alignment of ZrO_2/IL/Si system. $E_{g(ZrO_2)}$ = bandgap of ZrO_2, $E_{g(IL)}$ = bandgap of IL, $E_{g(Si)}$ = bandgap of Si, $\Delta E_{v(ZrO_2/Si)}$ = valence band offsets of ZrO_2 to Si, $\Delta E_{v(IL/Si)}$ = valence band offsets of IL to Si, $\Delta E_{c(ZrO_2/Si)}$ = conduction band offset of ZrO_2 to Si, $\Delta E_{c(IL/Si)}$ = conduction band offset of IL to Si, $\Delta E_{c(ZrO_2/IL)}$ = conduction band offset of ZrO_2 to IL. 97

4.9 Cross-sectional of EFTEM images of the investigated samples at different oxidation/nitridation durations: (a) 5 min, (b) 10 min, (c) 15 min, and (d) 20 min. Magnified images of Si substrate of each of the investigated sample is shown on the right side respectively (oxidation and nitridation was at $700^{o}C$ in N_2O). 99

4.10 Average thicknesses of ZrO_2 and interfacial layers for the investigated samples. Error bars define the maximum and minimum thicknesses obtained. 100

4.11 XRD patterns of bare n-type Si substrate, as-deposited Zr on Si, and oxidized/nitrided samples at 700^oC for various durations (5 – 20 min). Inset shows c-Si(400) peak with very strong intensity at 69.0^o. 101

4.12 Raman spectra of oxidized/nitrided samples at 700^oC for various oxidation/nitridation durations (5 – 20 min). 103

4.13 FTIR transmittance spectra for bare n-type Si substrate, as-deposited Zr on Si, and oxidized/nitrided samples at 700^oC for various oxidation/nitridation durations (5 – 20 min). 104

4.14 Growth mechanisms of oxidation/nitridation of Zr on Si: (a)-(c) are the initial stages when N_2O is exposed to Zr and after (d) 5 min, (e) 10 min, (f) 15 min, and (g) 20 min (all samples were exposed to 100% N_2O at 700^oC). 111

4.15 *C-V* characteristic of MOS capacitors with ZrO_2 oxidized/nitrided at various durations (5–20 min). The inset shows capacitors in series (oxidation and nitridation was at 700^oC in N_2O). 113

4.16 Effective oxide charge and total interface-trap density in ZrO_2 as a function of oxidation/nitridation durations (5–20 min). The inset shows slow trap density in ZrO_2 as a function of oxidation/nitridation durations (5–20 min) (oxidation and nitridation was at 700^oC in N_2O). 115

4.17 Inter-relationship of normalized interfacial layer thickness against normalized effective oxide charge, slow trap density, total interface-trap density, and dielectric breakdown. 116

4.18 Interface-trap density of the investigated ZrO_2 gate oxide oxidized/nitrided at 700^oC for various oxidation/nitridation durations (5–20 min). 117

4.19 Peak area of Zr-N and Si-N under the deconvoluted peaks from the interfacial depth profile of N 1*s* spectra. The inset shows deconvoluted peaks of Zr-N and Si-N from the interfacial depth profile of N 1*s* spectra. 119

4.20 Effective dielectric constant of the investigated oxides deduced from the *C-V* measurements as a function of oxidation/nitridation durations (5–20 min) (oxidation and nitridation was at 700^oC in N_2O). 120

4.21 *J-E* characteristics of the investigated $Al/ZrO_2/IL/Si$ MOS capacitors. Inset shows the average breakdown fields (E_B and E_{HDB}) for the investigated samples (oxidation and nitridation was at 700°C in N_2O). 122

4.22 Cumulative failure percentage of dielectric breakdown field (E_{BD}) of the investigated samples (oxidation and nitridation was at 700°C in N_2O). 123

4.23 FN tunneling linear regression plot [$\ln(J/E^2) - 1/E$] of investigated samples oxidized/nitrided in various oxidation/nitridation times (oxidation and nitridation was at 700°C in N_2O). 126

4.24 Barrier height values as a function of oxidation/nitridation durations (oxidation and nitridation was at 700°C in N_2O). 126

4.25 *C-V* characteristics of the investigated samples oxidized/nitrided at various temperatures. The inset shows the calculated κ_{eff} values as a function of oxidation/nitridation temperature (oxidation and nitridation time was 15 min in N_2O). 129

4.26 Effective oxide charge and total interface-trap density in the investigated sample as a function of oxidation/nitridation temperature. The inset shows slow trap density in the investigated sample as a function of oxidation/nitridation temperature (oxidation and nitridation time was 15 min in N_2O). 130

4.27 Interface-trap density of investigated sample oxidized/nitrided at various temperatures (oxidation and nitridation time was 15 min in N_2O). 132

4.28 *J-E* characteristics of investigated sample oxidized/nitrided at various temperatures (oxidation and nitridation time was 15 min in N_2O). 134

4.29 F-N tunneling linear regression plot [$\ln(J/E^2) - 1/E$] of investigated sample oxidized/nitrided at various temperatures (oxidation and nitridation time was 15 min in N_2O). 135

4.30 Effective barrier height values as a function of oxidation/nitridation temperature (oxidation and nitridation time was 15 min in N_2O). 136

5.1 Atomic percentage of Zr, Si, O, N, and C as a function of etching time for sample oxidized/nitrided samples at (a) 400°C, (b) 500°C, (c) 700°C, 900°C, and (e) nitrogen depth profile of all investigated samples (oxidation and nitridation time was 15 min in N_2O). 141

5.2 Evolution of Zr 3*d* core level XPS spectra as a function of etching time for different oxidation/nitridation temperature samples: (a) 400°C, (b) 500°C, (c) 700°C, and 900°C (oxidation and nitridation time was 15 min in N_2O). 142

5.3 Evolution of Si 2*p* core level XPS spectra as a function of etching time for different oxidation/nitridation temperature samples: (a) 400°C, (b) 500°C, (c) 700°C, and 900°C (oxidation and nitridation time was 15 min in N_2O). 143

5.4 Evolution of O 1*s* core level XPS spectra as a function of etching time for different oxidation/nitridation temperature samples: (a) 400°C, (b) 500°C, (c) 700°C, and 900°C (oxidation and nitridation time was 15 min in N_2O). 144

5.5 Evolution of N 1*s* core level XPS spectra as a function of etching time for different oxidation/nitridation temperature samples: (a) 400°C, (b) 500°C, (c) 700°C, and 900°C (oxidation and nitridation time was 15 min in N_2O). 146

5.6 A typical narrow scan of C 1*s* core-level spectra of interfacial layer for all investigated samples (oxidation and nitridation time was 15 min in N_2O). 147

5.7 (a) XPS valence band spectra of Zr-oxynitride and IL for all investigated samples. (b) XPS O 1*s* plasmon loss spectra of Zr-oxynitride and IL for 500°C sample. 149

5.8 The calculated values of $E_{g(ZrON)}$, $E_{g(IL)}$, $\Delta E_{c(ZrON/SiC)}$, $\Delta E_{c(IL/SiC)}$, and $\Delta E_{c(ZrON/IL)}$ in the band alignment of Zr-oxynitride/IL/SiC system. 150

5.9 Band alignment of Zr-oxynitride/IL/SiC system. $E_{g(ZrON)}$ = bandgap of Zr-oxynitride, $E_{g(IL)}$ = bandgap of IL, $E_{g(SiC)}$ = bandgap of SiC, $\Delta E_{v(ZrON/SiC)}$ = valence band offsets of Zr-oxynitride to SiC, $\Delta E_{v(IL/SiC)}$ = valence band offsets of IL to SiC, $\Delta E_{c(ZrON/SiC)}$ = conduction band offset of Zr-oxynitride to SiC, $\Delta E_{c(IL/SiC)}$ = conduction band offset of IL to SiC, $\Delta E_{c(ZrON/IL)}$ = conduction band offset of Zr-oxynitride to IL. 151

5.10 Cross-sectional of EFTEM images of the investigated samples at different oxidation/nitridation temperatures: (a) 400°C, (b) 500°C, (c) 700°C, and (d) 900°C. Lower magnification of each of the investigated sample is shown on the right side respectively (oxidation and nitridation time was 15 min in N_2O). 158

5.11 Average thicknesses of Zr-oxynitride, IL, and total (Zr-oxynitride + IL) for the investigated samples. Error bars define the maximum and minimum thicknesses obtained. 159

5.12 Arrhenius plots of Zr-oxynitride, IL, and total (Zr-oxynitride + IL) growth in the N_2O ambient. 160

5.13 Close-up XRD patterns of as deposited Zr on Si and oxidized/nitrided samples at different temperatures within the 2θ range of 25° – 35° to clearly show the characteristic peaks of tetragonal phase. The inset shows 4H-SiC(004) peaks with very strong intensity at 35.5^o and weak one at 43.2^o. 162

5.14 Raman spectra of bare n-type SiC substrate, as-deposited Zr on SiC, and oxidized/nitrided samples at various temperatures (400–900°C). 163

5.15 Two-dimensional AFM surface topography of (a) bare SiC substrate, (b) sputtered Zr on SiC substrate, and oxidized/nitrided samples at (c) 400°C, (d) 500°C, (e) 700°C, and (d) 900°C (oxidation and nitridation time was 15 min in N_2O). 164

5.16 Root-mean-square (RMS) surface roughness of samples oxidized/nitrided at various temperatures (400 – 900°C) (oxidation and nitridation time was 15 min in N_2O). 164

5.17 *C-V* characteristics of MOS capacitors with Zr-oxynitride oxidized/nitrided at various temperatures (400–900°C). The inset shows effective dielectric constant of the investigated samples deduced from the *C-V* measurement as a function of oxidation/nitridation temperatures (400–900°C) (oxidation and nitridation time was 15 min in N_2O). 167

5.18 Effective oxide charge and slow trap density contained in the investigated samples as a function of oxidation/nitridation temperatures (400–900°C) (oxidation and nitridation time was 15 min in N_2O). 168

5.19 Interface-trap density of the investigated samples oxidized/nitrided at various temperatures (400–900°C). The inset shows total interface-trap density of the investigated samples as a function of oxidation/nitridation temperatures (400–900°C) (oxidation and nitridation time was 15 min in N_2O). 170

5.20 *J-E* characteristics of investigated samples oxidized/nitrided at various temperatures (400–900°C) (oxidation and nitridation time was 15 min in N_2O). 171

5.21 Cumulative failure percentage of dielectric breakdown field (E_B) of the samples (oxidation and nitridation time was 15 min in N_2O). 172

5.22 FN tunneling linear regression plot [$\ln(J/E^2) - 1/E$] of investigated Zr-oxynitride film oxidized/nitrided at various temperatures (400 – 900°C) for 15 min. 173

5.23 Barrier height values as a function of oxidation/nitridation temperatures (oxidation and nitridation time was 15 min in N_2O). 174

5.24 Atomic percentage of Zr, Si, O, N, and C as a function of etching time for sample oxidized/nitrided in (a) 100%, (b) 70%, (c) 30%, and (d) 10% N_2O (oxidation and nitridation time was 15 min in N_2O). 184

5.25 Evolution of Zr 3*d* core level XPS spectra as a function of etching time for different N_2O concentration samples: (a) 100%, (b) 70%, (c) 30%, and (d) 10% (oxidation and nitridation time was 15 min in N_2O). 185

5.26 Evolution of Si 2*p* core level XPS spectra as a function of etching time for different N_2O concentration samples: (a) 100%, (b) 70%, (c) 30%, and (d) 10% (oxidation and nitridation time was 15 min in N_2O). 186

5.27 Evolution of O 1*s* core level XPS spectra as a function of etching time for different N_2O concentration samples: (a) 100%, (b) 70%, (c) 30%, and (d) 10% (oxidation and nitridation time was 15 min in N_2O). 188

5.28 Evolution of N 1*s* core level XPS spectra as a function of etching time for different N_2O concentration samples: (a) 100%, (b) 70%, (c) 30%, and (d) 10% (oxidation and nitridation time was 15 min in N_2O). 189

5.29 A typical narrow scan of C 1*s* core-level spectra of interfacial layer for all investigated samples (oxidation and nitridation time was 15 min in N_2O). 190

5.30 (a) XPS valence band spectra of Zr-oxynitride and IL for all investigated samples. (b) XPS O 1*s* plasmon loss spectra of Zr-oxynitride and IL for 10% N_2O sample. 192

5.31 The calculated values of $E_{g(ZrON)}$, $E_{g(IL)}$, $\Delta E_{c(ZrON/SiC)}$, $\Delta E_{c(IL/SiC)}$, and $\Delta E_{c(ZrON/IL)}$ in the band alignment of Zr-oxynitride/IL/SiC system, as a function of N_2O concentration. 193

5.32 Cross-sectional of EFTEM images of the investigated samples in different N_2O concentrations: (a) 100%, (b) 70%, (c) 30%, and (d) 10% (oxidation and nitridation was at 700^oC and 15 min). 195

5.33 A typical cross-sectional of EFTEM images of the 70% N_2O sample at lower magnification. The red circle shows two crystalline planes. 196

5.34 Average thicknesses of Zr-oxynitride, IL, and total (Zr-oxynitride + IL) for the investigated samples. Error bars define the maximum and minimum thicknesses obtained. 196

5.35 Close-up XRD patterns of as deposited Zr on Si and oxidized/nitrided samples at different temperatures within the 2θ range of 25°–35° to clearly show the characteristic peaks of tetragonal phase. 198

5.36 Illustration of t-ZrO_2 crystal structure arrangement with respect to baseline of substrate (t_{max} = maximum inclination height; t_{min} = maximum inclination height). 198

5.37 Williamson-Hall plot of t-ZrO_2 (oxidation and nitridation was at 700°C and 15 min). 200

5.38 Relationship of crystallite size and microstrains as a function of N_2O concentration calculated from Williamson-Hall plot (oxidation and nitridation was at 700°C and 15 min). 200

5.39 Crystallite size as a function of N_2O concentration calculated from Scherrer equation. 201

5.40 Raman spectra of oxidized/nitrided samples in various N_2O concentrations (10–100%). 203

5.41 Two-dimensional AFM surface topography of oxidized/nitrided samples at different N_2O concentrations: (a) 100%, (b) 70%, (c) 30%, and (d) 10% (oxidation and nitridation was at 700°C and 15 min). 205

5.42 Root-mean-square (RMS) surface roughness of samples oxidized/nitrided in various N_2O concentrations (10–100%) (oxidation and nitridation was at 700°C and 15 min). 206

5.43 *C-V* characteristics of MOS capacitors with Zr-oxynitride oxidized/nitrided in various N_2O concentrations (10–100%). The insets show effective dielectric constant of the investigated samples deduced from the *C-V* measurement as a function of N_2O concentrations (10–100%) and capacitors in series (oxidation and nitridation was at 700°C and 15 min). 208

5.44 Effective oxide charge and slow trap density contained in the investigated samples as a function of N_2O concentrations (10–100%) (oxidation and nitridation was at 700°C and 15 min). 209

5.45 Interface-trap density of the investigated samples oxidized/nitrided in different N_2O concentrations (10–100%). The inset shows total interface-trap density of the investigated samples as a function of N_2O concentration (10–100%) (oxidation and nitridation was at 700°C and 15 min). 211

5.46 *J-E* characteristics of investigated samples oxidized/nitrided in various N_2O concentrations (10–100%) (oxidation and nitridation was at 700°C and 15 min). 212

5.47 Cumulative failure percentage of dielectric breakdown field (E_{HDB}) of the investigated samples (oxidation and nitridation was at 700°C and 15 min). 215

5.48 FN tunneling linear regression plot [$\ln(J/E^2) - 1/E$] of investigated Zr-oxynitride film oxidized/nitrided in various N_2O concentrations (10–100%). The inset shows the barrier height values as a function of N_2O concentration (10–100%) (oxidation and nitridation was at 700°C and 15 min). 216

SELECTED LIST OF ABBREVIATIONS

AFM	:	Atomic Force Microscopy
C-V	:	Capacitance-Voltage
EFTEM	:	Energy-Filtered Transmission Electron Microscopy
FN	:	Fowler-Nordheim
FTIR	:	Fourier Transform Infrared
I.T.R.S.	:	International Technology Roadmap for Semiconductor
ICDD	:	International Conference for Diffraction Data
IL	:	Interfacial Layer
I-V	:	Current-Voltage
J-E	:	Leakage Current Density – Electric Field
LCR	:	Inductance-Capacitance-Resistance
MOS	:	Metal-Oxide-Semiconductor
RF	:	Radio Frequency
SPA	:	Semiconductor Parameter Analyzer
t	:	Tetragonal
XPS	:	X-ray Photoelectron Spectroscopy
XRD	:	X-ray Diffraction

SELECTED LIST OF SYMBOLS

$\emptyset_B$	:	Barrier height (eV)
$\emptyset_s$	:	Surface potential (eV)
ε_o	:	Permittivity of free space (F m^{-1})
A	:	Capacitor Area (cm^2)
C	:	Capacitance (pF)
C_{IL}	:	Capacitance of interfacial layer (IL) (pF)
C_{ox}	:	Oxide capacitance (pF)
C_{total}	:	Total capacitance (pF)
C_{ZrO2}	:	Capacitance of ZrO_2 (pF)
C_{ZrON}	:	Capacitance of Zr-oxynitride (pF)
d	:	Interplanar spacing (nm)
D_{it}	:	Interface trap density (eV^{-1} cm^{-2})
D_{total}	:	Total interface trap density (cm^{-2})
E	:	Electric field (MV cm^{-1})
E_C	:	Conduction band edge (eV)
E_V	:	Valence band edge (eV)
I	:	Current (A)
J	:	Leakage current density (A cm^{-2})
m	:	Free electron mass
m_{ox}	:	Effective electron mass in the oxide
q	:	Electronic charge (C)
Q_{eff}	:	Effective oxide charge
T	:	Oxidation temperature (^oC)
t	:	Oxidation time (min)

t_{ox}	:	Oxide thickness (nm)
t_{ZrO_2}	:	Thickness of ZrO_2 (nm)
t_{ZrON}	:	Thickness of Zr-oxynitride (nm)
V_{FB}	:	Flatband voltage (V)
V_g	:	Gate voltage (V)
θ	:	Diffraction angle
κ	:	Dielectric constant
κ_{eff}	:	Effective dielectric constant

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2. Y.H. Wong and K.Y. Cheong, "Physical and Electrical Characterizations of Thermally Oxidized/Nitrided Zr Thin Films on Si at Various Temperatures in N_2O Environment," *International Conference on Enabling Science and Nanotechnology (ESciNano) 2012*, Persada International Convention Centre, Johor Bahru, Malaysia, 5th – 7th January 2012.

KAJIAN PENGOKSIDAAN DAN PENITRIDAAN TERMA SERENTAK TERHADAP ZIRKONIUM YANG DIPERCIKKAN DI ATAS SILIKON DAN SILIKON KARBIDA MENGGUNAKAN GAS NITROUS OKSIDA

ABSTRAK

Filem nipis Zr yang dipercikkan di atas Si dan SiC telah menjalani pengoksidaan and penitridaan serentak dengan menggunakan gas N_2O. Kesan masa (5–20 min) dan suhu (500–1100^oC) pengoksidaan/penitridaan ke atas sistem Zr/Si dan kesan suhu pengoksidaan/penitridaan (400–900^oC) dan kepekatan N_2O (10–100%) ke atas sistem Zr/SiC telah dijalankan. Pencirian struktur, kimia, dan elektrik seterusnya dijalankan. Keputusan spektroskopi fotoelektron sinar-X menunjukkan filem nipis ZrO_2 dan lapisan antaramuka (IL) Zr-silikat oksinitrida (ZrSiON) telah dihasilkan di atas Si, manakala Zr-oksinitrida (ZrON) dan IL ZrSiON dan karbon nitrida telah dihasilkan di atas SiC. Mekanisme pengoksidaan dan penitridaan telah dicadangkan dan dijelaskan dengan mengambilkira semua keputusan diperolehi daripada mikroskop elektron pancaran penapis tenaga, pembelau sinar-X, spektrometer Raman, spektrometer inframerah jelmaan Fourier, dan/atau mikroskop daya atom. Keputusan elektrik menunjukkan pengoksidaan/penitridaan ke atas Zr/Si pada suhu 700^oC selama 15 min dalam 100% N_2O mencatatkan medan pecah tebat (E_B) tertinggi iaitu 13.60 MV/cm pada 10^{-6} A/cm^2. Untuk Zr/SiC, E_B yang tertinggi iaitu 5.05 MV/cm pada ketumpatan arus yang sama diperoleh daripada pengoksidaan/penitridaan Zr pada suhu 500^oC selama 15 min. Penambahbaikan E_B (7.59 MV/cm) ke atas sistem Zr/SiC telah diperoleh menggunakan parameter pengoksidaan/penitridaan yang sama tetapi dengan kepekatan N_2O yang rendah (10%). Ketumpatan perangkap antaramuka oksida-semikondukor, cas oksida, dan perangkap perlahan, serta ketinggian sawar telah dikira dan dihubungkait dengan E_B.

INVESTIGATION OF SIMULTANEOUS THERMAL OXIDATION AND NITRIDATION OF SPUTTERED ZIRCONIUM ON SILICON AND SILICON CARBIDE IN NITROUS OXIDE GAS ENVIRONMENT

ABSTRACT

Thin film Zr on Si and SiC were formed by sputtering. The films then underwent simultaneous oxidation and nitridation in N_2O. The effects of oxidation/nitridation durations (5–20 min) and temperatures (500–1100^oC) on the sputtered Zr/Si system and the effects of oxidation/nitridation temperatures (400–900^oC) and the concentrations of N_2O (10–100%) to the characteristics of the sputtered Zr/SiC system were studied. Structural, chemical, and electrical properties of the samples were examined. X-ray photoelectron spectroscopy results showed that ZrO_2 thin film was formed with an interfacial layer (IL) of Zr-silicate oxynitride (ZrSiON) on Si, while Zr-oxynitride (ZrON) thin film was formed with an IL of ZrSiON and carbon nitride on SiC. Oxidation and nitridation growth mechanisms has been proposed, after considering all results obtained by energy filtered transmission electron microscope, X-ray diffractometer, Raman spectrometer, Fourier transform infrared spectrometer, and/or atomic force microscope. Electrical results showed that oxidized/nitrided Zr/Si at 700^oC for 15 min in 100% N_2O has demonstrated the highest breakdown field (E_B) of 13.60 MV/cm at 10^{-6} A/cm^2. As for Zr/SiC, the highest E_B of 5.05 MV/cm at the same current density was attained by oxidized/nitrided Zr at 500^oC for 15 min. Further enhancement on the E_B was recorded (7.59 MV/cm) for Zr/SiC system oxidized/nitrided at the same parameters but with lower concentration of N_2O (10%). Oxide-semiconductor interface-trap density, effective oxide charge, slow trap density, and barrier height were calculated and correlated with the breakdown field of the investigated samples.

CHAPTER 1

INTRODUCTION

1.1 Background

The current progress in semiconductor industry is mainly focusing in four parallel directions, which include downscaling of circuit elements on an inexpressible scale, reducing its power consumption, increasing operation speed, and tolerance-temperature range (Wilk *et al.*, 2001). Although silicon (Si) possesses several merits, such as: (i) ability to be produced in a very large defect-free single crystal, with very low and well-controlled doping level as required by high voltage application, and (ii) ability to grow native oxide (SiO_2) with superior properties (Chante *et al.*, 1998). Nevertheless, the current technology of Si and design of new device structures have yet complied with the endless demand for higher current and voltage handling capacity (Dimitrijev and Jamet, 2003; Yu *et al.*, 2008). Hence, this advent of technology boom has spurred utilization of wide bandgap (WBG) semiconductors as alternative substrates to replace silicon for high-power, high-temperature, and/or high-radiation applications metal-oxide-semiconductor (MOS)-based switching devices (Luo *et al.*, 2004; Lim *et al.*, 2010).

Amongst WBG semiconductors, silicon carbide (SiC) has developed into one of the leading contenders owing to its commercial availability and ability to grow SiO_2 as well (Dimitrijev *et al.*, 2004; Lim *et al.*, 2010). SiC appears in different polytypes (Casady and Johnson, 1996; Soo *et al.*, 2010). 4H-SiC is one of the polytypes that provides a wide bandgap of 3.26 eV, high breakdown field strength of

~3 MV/cm, high saturation electron drift velocity of ~2×10^7 cm/s, and high thermal conductivity of ~3.7 W/cm^{o}C (Wesch, 1996; Afanas'ev *et al.*, 2004; Lim *et al.*, 2010). Demonstration of these properties makes SiC-based MOS devices potentially suited for operation under harsh conditions (Casady and Johnson, 1996; Wesch, 1996; Afanas'ev *et al.*, 2004; Dimitrijev *et al.*, 2004; Lim *et al.*, 2010; Soo *et al.*, 2010). In order to fabricate these devices, a high quality gate oxide must be deposited or grown between a metal electrode and the semiconductor substrate in order to sustain a high transverse electric field and a low gate leakage current in the MOS-based devices (Cheong *et al.*, 2008).

1.2 Problem Statement

Aggressive miniaturization of Si-based metal-oxide-semiconductor (MOS) devices has attributed more transistors to be packed in a chip (Wilk *et al.*, 2001; Guha and Narayanan, 2009). Consequently, dimension of MOS structure has to be reduced proportionally without affecting its electrical design (Robertson, 2004). Therefore, SiO_2, which has been used for decades as a gate dielectric in MOS devices, has to be scaled down. As the oxide thickness is less than 1.2 nm, the occurrence of relatively huge leakage current through the oxide, due to direct tunneling of carriers, is highly possible (Robertson, 2004; Kurniawan *et al.*, 2011; Kurniawan *et al.*, 2011).

In order to overcome the aforementioned challenge, a high dielectric constant (κ) oxide acting as an alternative dielectric to supersede SiO_2 has been developed. The physical thickness of the high κ oxide must demonstrate similar or better MOS characteristics that are equivalent to the SiO_2 (Robertson, 2004; Quah *et al.*, 2010).

To proportionally scale the dimension of a MOS structure without affecting the electrical designs (Robertson, 2004; Robertson, 2006), it is convenient to define an equivalent oxide thickness (*EOT*) as the thickness of high-κ material that would be required to have the same capacitance as SiO_2, which is given by Equation (1.1) (Wilk *et al.*, 2001; Wallace and Wilk, 2003):

$$EOT = t_{\text{high-}\kappa} = \frac{\kappa_{high-k}}{\kappa_{SiO_2}} t_{SiO_2} \tag{1.1}$$

where, $t_{\text{high-}\kappa}$ and t_{SiO_2} are the thicknesses of high-κ dielectric material and SiO_2 respectively, while $\kappa_{\text{high-}\kappa}$ and κ_{SiO_2} are the dielectric constants of the high-κ dielectric material and SiO_2 respectively. Therefore, the objective is to develop high-κ oxides, which allow scaling to a much thinner *EOT*.

On the other hand, in SiC-based MOS devices, the low-κ value of 3.9 in SiO_2, as compared to SiC with κ value of 10, could cause oxide breakdown and reliability issues. According to Gauss law as given by Equation (1.2) (Lipkin and Palmour, 1999):

$$E_{ox} \bullet \kappa_{ox} = E_{SiC} \bullet \kappa_{SiC} \quad (1.2)$$

where, E_{ox} and E_{SiC} are the electric field strengths in the oxide and SiC, respectively, while κ_{SiC} is the dielectric constant of SiC. The high electric field strength in SiC of ~3 MV/cm, would give a high electric field of ~7.69 MV/cm in SiO_2, in which, it is equivalent to a factor of ~2.56 times higher electric field being imposed on the gate oxide than on the SiC. Consequently, the gate oxide may electrically break down much earlier than the SiC substrate thus depletes the objective of using SiC as the primer substrate for high power, high temperature, and/or high radiation applications.

An approach to circumvent this is to supersede the relatively low-κ SiO_2 with a gate oxide with higher κ value (Choyke *et al.*, 2004). The integration of high-κ dielectrics on Si is to solve the down-scaling issues, while integration of high-κ dielectrics on SiC is to lower the electric field being imposed on the gate oxide.

Of the high-κ materials investigated, Al_2O_3 is found to have large fixed charge and interface trap density and with only a κ value of about 10 (Maria *et al.*, 2001; Wilk *et al.*, 2001; Robertson, 2004; Robertson and Peacock, 2004; Robertson, 2006; Wong and Iwai, 2006). TiO_2 and Ta_2O_5 have too low conduction band offsets with Si conduction band aggravate the film leakage (Robertson, 2002; Robertson, 2004; Robertson and Peacock, 2004; Robertson, 2006; Wong and Iwai, 2006). In addition, thermodynamic instabilities of TiO_2 and Ta_2O_5 on Si are another demerit (Hubbard and Schlom, 1996; Chaneliere *et al.*, 1998; Wong and Iwai, 2006). TiO_2 and Y_2O_3 are found to have low crystallization temperature (< 400 °C) (Cho *et al.*,

1999; Wong and Iwai, 2006), which is below most of the processing temperatures in the present MOS fabrication technology. Additionally, the interface density of Y_2O_3 (> 10^{12} $eV^{-1}cm^{-2}$) (Wong and Iwai, 2006) is too high for MOS device applications. On the other hand, a rough interface layer is found when La_2O_3 in contact with Si (Wong and Iwai, 2006), which gives undesirable electrical interface. Besides, lower breakdown field and higher leakage current are found in La_2O_3/4H-SiC system (Moon *et al.*, 2006). Furthermore, moisture absorption (hygroscopic) in La_2O_3 is also a serious problem (Robertson, 2004; Robertson, 2006; Wong and Iwai, 2006).

Zirconium oxide (ZrO_2) has attracted much attention owing to its fascinating properties, such as high κ value (22–25), large energy bandgap (5.8–7.8 eV), and easily stabilized in the form of cubic or tetragonal polymorphs, which may further enhance its effective κ value (Wilk *et al.*, 2001). In addition, it also possesses good thermodynamic stability when in contact with Si and it has minimal lattice mismatch with Si(100) (Puthenkovilakam *et al.*, 2004; He *et al.*, 2005; Wang *et al.*, 2005; Giorgi *et al.*, 2008; Ma and Zhang, 2008; Zhang *et al.*, 2009).

Generally, the ZrO_2/semiconductor interfaces are often regarded as non-ideal owing to the existence of interface defects, which is arisen from surface-structural defects, oxidation-induced defects, or radiation-induced defects (Mudanai *et al.*, 2002; Cheng *et al.*, 2006; Schroder, 2006). The interface trap has a significant impact on the reliability and lifetime of a MOS device, as it is a major contributor to leakage current besides the characteristics of the oxide itself (Yamanaka *et al.*, 1996; Cheng *et al.*, 2006). Therefore, various deposition techniques have been used to control the thickness and composition of interfacial layer (IL) in between the oxide and

semiconductor. By doing that, an acceptable level of interface-trap density may be obtained.

So far, it is reported that the formation of interface traps can be effectively suppressed by nitridation of a Si surface prior to the deposition of ZrO_2 film or by incorporating nitrogen into ZrO_2 film (Koyama *et al.*, 2001; Chen *et al.*, 2007). Chen *et al.* (2007) demonstrated that a thinner IL (2.5 nm) with a lower interface trap density of a MOS structure with Si surface being nitrided prior to the oxide deposition. An ultrathin IL (2.2 nm) was also revealed by ZrO_2 incorporated with nitrogen to form a non-stoichiometric ZrO_2 (ZrON) film demonstrated. (Koyama *et al.*, 2001). Although the IL was thin, MOS characteristics of the capacitor was not improved significantly owing to a low effective dielectric constant (κ_{eff} = 17) of the oxide. Besides, post-deposition annealing of ZrO_2 film in nitrogen ambient was also studied in order to improve its electrical properties (Lin *et al.*, 2003; Zhu *et al.*, 2006). It was found that incorporation of nitrogen into the film may retard the growth of interfacial layer and improved electrical properties of the film. This improvement may be attributed to two factors. Firstly, the presence of nitrogen is postulated to passivate the oxygen vacancies by forming Zr-N, Si-N, and/or Si-O-N bonds, thus reducing amount of interfacial traps. In addition, these particular bonds are believed to effectively suppress crystallization that may enhance thermal stability of the film. Secondly, dangling bonds of Si surface may be passivated by the nitrogen-rich species generated during nitridation process (de Almeida and Baumvol, 2003).

Based on several studies, ZrO_2 thin films were successfully formed by a combination of Zr metal sputtering and oxidation process in an oxygen ambient (Nagasato *et al.*, 2005; Hsieh *et al.*, 2006; Kim *et al.*, 2006; Kurniawan *et al.*, 2011).

In this work, formation of ZrO_2 and Zr-oxynitride by simultaneous thermal oxidation and nitridation of sputtered Zr thin film was proposed. This simultaneous process can be carried out in N_2O or NO ambient. The nitridation effect in this process is postulated to provide good electrical properties to the MOS device. When the gas is heated high enough, nitrogen, oxygen, and their related compounds are formed. The dominance of the oxidation and nitridation processes may depend on their respective reaction rate. Gas of NO is extremely toxic (Enta *et al.*, 2006). Hence, to perform a simultaneous thermal oxidation and nitridation on metallic Zr, N_2O gas is more appropriate and preferable due to its non-toxic property (Enta *et al.*, 2006). However, up to date, there is no report on the effects of either N_2O or NO gas on a sputtered Zr thin film on Si and SiC substrates. Therefore, this is the main objective of this thesis is to report on the effects of thermal oxidation and nitridation of sputtered Zr/Si and sputtered Zr/SiC systems in N_2O ambient on their structural, chemical, and electrical properties. Based on these results, a possible growth mechanism related to the oxidation and nitridation is proposed.

1.3 Research Objectives

The main objective of this research is to form oxidized/nitrided Zr thin films on Si and SiC substrates by simultaneous thermal oxidation and nitridation of sputtered Zr in N_2O ambient. With this main objective, the following aspects are to be achieved:

1. To investigate the effects of oxidation/nitridation durations and temperatures on the structural, chemical, and electrical properties of the oxidized/nitrided sputtered Zr thin films on Si substrate.
2. To investigate the effects of oxidation/nitridation temperatures and concentrations of N_2O gas on the structural, chemical, and electrical properties of the oxidized/nitrided sputtered Zr thin films on SiC substrate.
3. To compare the structural, chemical, and electrical properties of the oxidized/nitrided sputtered Zr thin films on Si and SiC substrates.
4. To establish a growth mechanism related to oxidation/nitridation to explain the formation of oxidized/nitrided Zr thin films on both Si and SiC substrates.

1.4 Scope of Study

In this study, Zr thin film was sputtered on Si and SiC substrates and then submitted to simultaneous thermal oxidation and nitridation in N_2O ambient to form oxidized/nitrided Zr on Si and SiC substrates. Various parameters were performed, namely (i) effects of oxidation/nitridation durations on sputtered Zr on Si substrate, (ii) effects of oxidation/nitridation temperatures on sputtered Zr on Si substrate, (iii)

effects of oxidation/nitridation temperatures on sputtered Zr on SiC substrate, (iv) comparison of oxidation/nitridation of sputtered Zr on Si and SiC substrates in 100% N_2O, and (v) oxidation/nitridation of sputtered Zr on SiC substrate in diluted N_2O.

Structural and chemical characterizations of oxidized/nitrided Zr thin films were conducted by using X-ray photoelectron spectroscopy (XPS) measurements, energy-filtered transmission electron microscopy (EFTEM) analysis, X-ray diffraction (XRD) analysis, Raman analysis, Fourier transformed infrared (FTIR) spectroscopy, and atomic force microscopy (AFM) analysis. On the other hand, semiconductor parameter analyzer (SPA) and LCR meter were employed in order to characterize the electrical properties of the films.

1.5 Thesis Outline

This thesis is organized and divided into five chapters. Chapter 1 provides an overview of current issues and challenges faced in MOS-based devices, research objectives, and scope of study. Chapter 2 covers the detailed literature review, which corresponds to the background theories adopted in the study. The following chapter 3 presents the systematic methodology of the research. Chapters 4 and 5 focus on the results and discussion from the conducted characterizations. Chapter 6 summarizes this study and its conclusions. Recommendations for future works are also presented in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In line with the demand of microelectronic devices suitable for high power, high temperature, and/or high radiation applications, the research direction of such devices is now focusing on the utilization of SiC substrate. This chapter reviews the superior properties of SiC as an alternative substrate to replace Si. A comparison of materials properties between Si and SiC is summarized. It is followed by an introduction to MOS structure and on device fundamentals. In order to tailor the electrical properties of a MOS device, it is essential to understand the materials properties of a gate oxide as a dielectric layer on a semiconductor substrate. Literatures of gate oxide on Si and SiC are reviewed. The selection criteria for the integration of a gate oxide as dielectric on Si and SiC are described. As ZrO_2 was selected as a material for gate oxide in this study, this chapter reviews the electrical and material properties of ZrO_2. Various deposition techniques to form ZrO_2 thin films on Si are discussed in this chapter. Since one of the techniques focused in this work is thermal oxidation of sputtered Zr, the mechanisms of the formation of the thin film metal into oxide is reviewed in here. Reports on the characteristics of ZrO_2 on SiC substrate are summarized and reviewed. Finally, the role of nitrogen in gate oxide on Si and SiC substrates is described.

2.2 SiC as an Alternative Substrate for Si

Since the late 1990s, in the microelectronic industry, the dominance of Si as a semiconductor substrate for power devices is very common. This is owing to its ability to be produced in a very large defect-free single crystal, with very low and well-controlled doping level as required by high voltage application, ability to grow SiO_2 with superior dielectric properties, and has established technology in electronic processing and packaging (Chante *et al.*, 1998).

Nonetheless, due to the narrow bandgap of Si, high intrinsic carrier concentrations at temperatures as low as 200 – 250°C is observed, leading to high leakage current (Chante *et al.*, 1998). This indicates that the operating temperature of Si is limited to a maximum of 250°C therefore limits Si to be used for device applications requiring high-power, high-temperature, and/or high-radiation conditions. Practical operation of Si-based electronic devices above 250°C will raise problem, as self-heating at high power levels results in high internal junction temperatures and leakages. As a result, substantial effort has been placed on the search of semiconductor material that can function at temperatures above 250°C.

The superior properties in the field of high temperature, high power and/or high radiation applications can be estimated by comparing bandgap and breakdown of the semiconductor (Soo *et al.*, 2010). It has been recognized that wide bandgap semiconductor like SiC are capable of electronic functionality at much higher temperatures (Casady and Johnson, 1996; Neudeck *et al.*, 2002; Soo *et al.*, 2010). Mass productions of single crystal SiC wafers have been commercially available for

nearly two decades. SiC crystals have fewer dislocation defects as compared to other wide bandgap semiconductors (Casady and Johnson, 1996; Dimitrijev *et al.*, 2004; Lim *et al.*, 2010; Soo *et al.*, 2010). Besides, the ability of growing SiO_2 on SiC is another merit of SiC (Casady and Johnson, 1996; Dimitrijev *et al.*, 2004; Lim *et al.*, 2010; Soo *et al.*, 2010). In addition, SiC comprised of light atoms held together by strong forces. With this high strength Si–C bond, it produces useful properties such as chemical inertness and low diffusion coefficients at high temperatures (Wright *et al.*, 2008; Soo *et al.*, 2010). This implies that SiC has high temperature stability.

2.3 Comparison of Materials Properties Between Si and SiC

The unique feature of SiC is its appearance in many different polytypes (Pensl *et al.*, 2005; Soo *et al.*, 2010). There are approximately 250 polytypes have been discovered and identified by Laue patterns (Pensl *et al.*, 2005; Soo *et al.*, 2010). All polytypes of SiC have an identical planar arrangement, which is composed of Si-C-bilayers perpendicular to the c-axis (Pensl *et al.*, 2005), as shown in Figure 2.1. However, the disorder in the stacking periodicity (staking sequence) of identical planes produces polytypes, with the same atomic composition. The most common polytypes those are of greatest interest include 4H-, 6H-, and 3C-SiC.

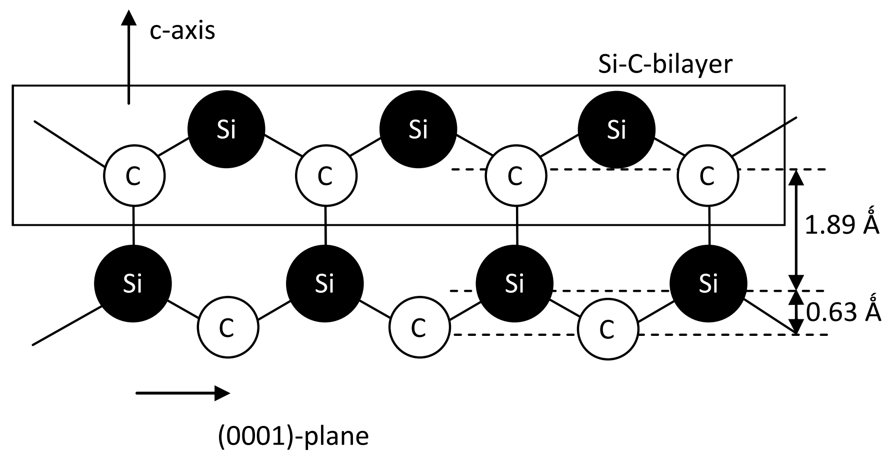

Figure 2.1: The basic component of Si-C-bilayer for the formation of polytypes.

The properties of Si and selected polytypes of SiC at room temperature are compared in Table 2.1 (Yoder, 1996; Luo *et al.*, 2004). Amongst the polytypes, the dielectric constants, thermal conductivities, and saturated electron velocity are not much different. For high temperature and high power applications, 3C-SiC is inferior to 4H- and 6H-SiC due to its lower bandgap, higher intrinsic carrier concentration, and lower breakdown field. But, single-crystal of 3C-SiC bulk substrate has not been achieved, thus it is unavailable commercially. 4H- and 6H-SiC on the other hand are readily available as bulk single-crystal substrates commercially. 4H-SiC has relatively larger bandgap and a lower intrinsic concentration by two orders of magnitude compared to 6H-SiC. The higher carrier mobility of 4H-SiC as compared to 6H-SiC makes it preferable to be used for power electronic devices.

Table 2.1: Comparison of the properties of Si and selected polytypes of SiC at room temperature (Yoder, 1996; Luo *et al.*, 2004).

Properties	Si	4H-SiC	6H-SiC	3C-SiC
Bandgap (eV)	1.12	3.26	3.00	2.20
Dielectric constant	11.80	10.00	9.70	9.60
Intrinsic carrier concentration (cm^{-3})	10^{10}	10^{-7}	10^{-5}	10
Thermal conductivity (W/cmK)	1.50	4.90	4.90	5.00
Breakdown field (MV/cm)	0.30–0.60	3.00	2.50–3.30	2.00
Saturated electron drift velocity (10^7 cm/s)	1.00	1.08–2.00	1.96–2.00	2.50
Hall mobility (cm^2/Vs)				
Hole	1100–1450	800–1000	370–500	750–1000
Electron	420–500	115	90	40
Availability of commercial wafers	Yes	Yes	Yes	No

By comparing the properties between Si and 4H-SiC (Table 2.1), it is found that the bandgap of 4H-SiC is significantly larger than that of Si. Hence, the wide bandgap provides a substantial barrier to thermal excitation and electrical conduction (Yoder, 1996; Soo *et al.*, 2010). The intrinsic concentration of 4H-SiC is 17 orders of magnitude lower than that of Si. Intrinsic concentration of semiconductor increases exponentially as the temperature increases (Neudeck *et al.*, 2002). Si-based devices will suffer from malfunctioning at above 250°C, whereas SiC-based devices can function at 600°C. The thermal conductivity of 4H-SiC is three times higher than that of Si. Consequently, heat dissipation is more efficient, allowing operation at higher junction temperature thus reducing the numbers of cooling hardware (Yoder, 1996; Elasser and Chow, 2002). 4H-SiC shows an order magnitude of improvement in the electrical breakdown field, which allows a ten-fold reduction in drift layer thickness, thus lessening the minority carrier charge storage and greatly increasing the switching frequency of a power device (Elasser and Chow, 2002).

2.4 Metal-Oxide-Semiconductor (MOS) Structure and Device Fundamentals

2.4.1 MOS Structure

MOS structure consists of three layers, with a conductive metal electrode on the top layer, a gate oxide in the middle layer, and a semiconductor substrate at the bottom layer, as shown in Figure 2.2. This structure is one of the most essential and widely used systems in the electronic devices, especially in integrated circuits. Of all MOS devices, the two-terminal MOS capacitor (Figure 2.2) is the simplest one and it is usually fabricated and utilized for electrical characterizations. In particular, the charge, electric field, and band bending inside the MOS capacitor under different static biasing conditions (V_g) can be quantitatively visualized (Pierret, 1990).

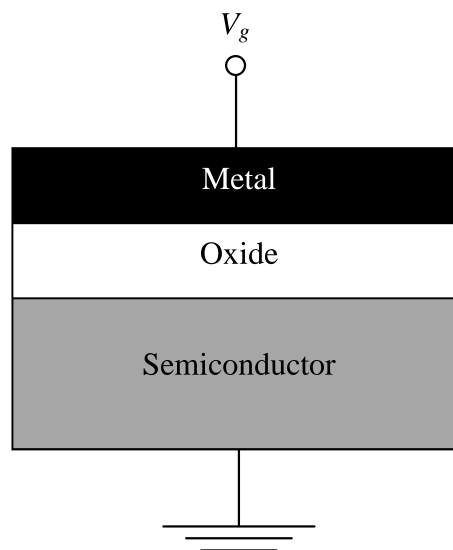

Figure 2.2: Schematic diagram of MOS structure capacitor.

2.4.2 Influence of Applied Bias

Figure 2.3 displays the energy-band diagrams for ideal MOS capacitors of *n*-type and *p*-type under various bias conditions of accumulation, depletion, and inversion. Taking the semiconductor substrate to be an *n*-type first, with an application of a positive bias (V > 0) to the metal plate. It is seen that the valence-band edge (E_v) bends downward [Figure 2.3(a)]. Electron concentration inside the semiconductor increases as it approaches the oxide-semiconductor interface. This particular condition, where the majority carrier concentration is greater near the oxide-semiconductor interface than in the bulk of semiconductor, is known as accumulation. When a small negative voltage (V < 0) is applied, the bands bend upward [Figure 2.3(b)], the concentration of the majority carrier electrons decreases and depletes, in the vicinity of the oxide-semiconductor interface. This is the depletion case. When a larger negative voltage is applied, the bands bend even more upward so that the intrinsic level (E_i) at the surface crosses over the Fermi level (E_F) [Figure 2.3(c)]. At this point, whereby the number of electrons (minority carriers) at the surface is larger than that of the holes, the surface is inverted; hence this is the inversion case. Similar results can be obtained for the *p*-type semiconductor; however, the changing of the polarity of the voltage is necessary (Pierret, 1990; Sze and Ng, 2007).

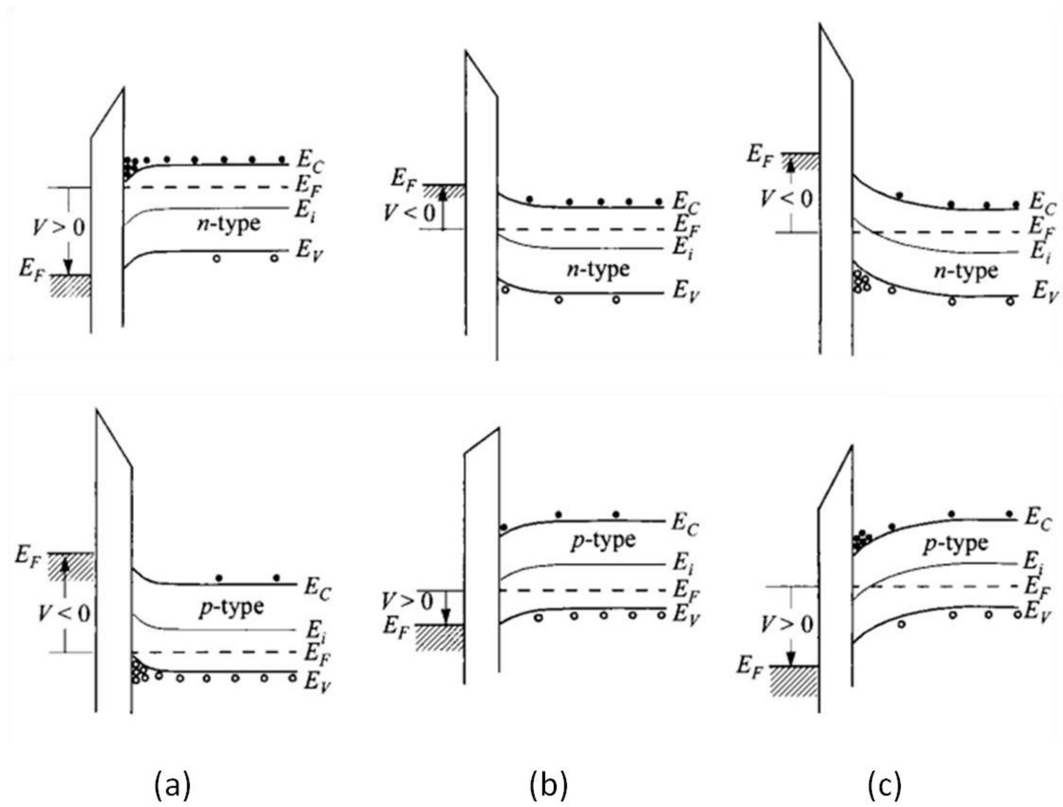

Figure 2.3: Energy-band diagrams for ideal MOS capacitors of n-type and p-type under various bias conditions: (a) accumulation, (b) depletion, and (c) inversion (Sze and Ng, 2007).

2.5 Gate Oxide on Si

Owing to the continuous improvement of integrated circuit (IC) performance for microelectronic industry, there are several technological requirements to fuel the market's enormous growth (Wilk *et al.*, 2001). The requirements include performance (speed), low static (off-state) power, and a wide range of power supply and output voltages (Wilk *et al.*, 2001; Conard *et al.*, 2007; Degraeve *et al.*, 2007; Guha and Narayanan, 2009). This eventually has been accomplished by reducing the dimensions of MOS structure.

The continual miniaturization of MOS devices has led SiO_2, which has been used for decades as gate dielectric, a necessity to be scaled down. Unfortunately, according to International Technology Roadmap for Semiconductors (ITRS) for the most recent updates 2010 (http://www.itrs.net, accessed August 2010) and several reports (Miyazaki, 2002; Chau *et al.*, 2003; Conard *et al.*, 2007; Degraeve *et al.*, 2007; Giorgi *et al.*, 2008; Guha and Narayanan, 2009), a limit of thickness of SiO_2 gate layers is 1.2 nm, if the gate layer is made thinner, problems such as (Robertson, 2004; Robertson, 2006; Wong and Iwai, 2006), (i) gate leakage current due to direct tunnelling of electrons through SiO_2 will be very high, (ii) difficulty in fabricating the film in such small thickness, and (iii) reliability of SiO_2 films against electrical breakdown, will be raised. Equation (2.1) shows:

$$C_{SiO_2} = \frac{\kappa_{SiO_2} \bullet \varepsilon_o \bullet A}{t_{SiO_2}} \tag{2.1}$$

where, C_{SiO_2} is the capacitance of SiO_2, κ_{SiO_2} is the dielectric constant of SiO_2, which is 3.9, ε_o is the permittivity of free space (8.85×10^{-12} F/m), A is the area of capacitor, and t_{SiO_2} is the thickness of SiO_2. From Equation (2.1), it tells that by decreasing the thickness of SiO_2, the gate capacitance will increase. Higher dielectric constant material than SiO_2 is necessary in order to maintain the gate capacitance value. In MOS structure, all dimensions scale proportionally without affecting the electrical designs (Robertson, 2004; Robertson, 2006), thus, it is convenient to define an equivalent oxide thickness (*EOT*) as the thickness of high-κ material that would be required to have the same capacitance as SiO_2.

There are a lot of works on finding an alternative oxide with high κ properties for the gate dielectric as to replace SiO_2 on Si, for instance, Al_2O_3 (Manchanda *et al.*, 1998; Gusev *et al.*, 2001; Groner *et al.*, 2002), ZrO_2 (Copel *et al.*, 2000; Gusev *et al.*, 2001; Jeon *et al.*, 2001; Maria *et al.*, 2001; Gutowski *et al.*, 2002; Zhang *et al.*, 2002; Shin and Liu, 2007), HfO_2 (Gusev *et al.*, 2001; Gutowski *et al.*, 2002; Gusev *et al.*, 2003; Shin and Liu, 2007), La_2O_3 (Maria *et al.*, 2001; Vellianitis *et al.*, 2004), TiO_2 (Campbell *et al.*, 1997; McCurdy *et al.*, 2004), Ta_2O_5 (Dimitrova and Atanassova, 1998; Lu *et al.*, 1999; Spassov *et al.*, 2006), and Y_2O_3 (Kang *et al.*, 1999; Kwo *et al.*, 2003; Paumier and Gaboriaud, 2003). Although these transition metal oxides have higher κ than SiO_2, not all of them can be used as dielectric layer in MOS device. In order to select an appropriate high-κ material to replace SiO_2 on Si, there are six requirements to be satisfied (Robertson, 2004; Robertson, 2006):

1. It must have a significantly higher κ value than SiO_2.
2. It must be thermodynamically stable when it is in contact with the Si channel.
3. It must be kinetically stable and compatible with processing temperature up to 1000˚C.
4. It must act as an insulator by having band offsets with Si of over 1 eV to minimize carrier injection into its bands.
5. It must form a good electrical interface with Si.
6. It must have a low density of electrically active defects at the Si-dielectric interface and in the bulk of material.

2.6 Gate Oxide on SiC

Like Si, SiC can be thermally oxidized to form SiO_2 on SiC (Casady and Johnson, 1996; Dimitrijev *et al.*, 2004; Lim *et al.*, 2010; Soo *et al.*, 2010). To date, thermally nitrided-SiO_2 on SiC is still considered as the best choice for gate oxide on SiC. This is because of its low interface and slow trap densities, high reliability, and low leakage current (Jamet and Dimitrijev, 2001; Jamet *et al.*, 2001; Cheong *et al.*, 2003; Cheong *et al.*, 2007; Rozen *et al.*, 2007; Cheong *et al.*, 2008; Rozen *et al.*, 2009; Cheong *et al.*, 2010). However, as stated by Gauss law in Eq 1.3, the low dielectric constant (κ) value of 3.9 of SiO_2, as compared to SiC with κ value of 10, could cause oxide breakdown and reliability issues. If the low-κ gate oxide electrically breaks down, this would diminishes the purpose of using SiC as the potential substrate for high power, high temperature, and/or high radiation applications. Apart from that, there are numerous problems associated with the SiO_2 thin film on SiC; high SiO_2-SiC interface-trap density and insufficient stability at elevated temperature and high electric field being imposed on the gate oxide (Lipkin and Palmour, 1999; Moon *et al.*, 2010).

In order to overcome the problems, an alternative gate oxide, with higher κ value has been proposed. Several high κ gate oxides on SiC have been investigated, which include MgO (Goodrich *et al.*, 2008), Gd_2O_3 (Fissel *et al.*, 2006), Pr_2O_3 (Lo Nigro *et al.*, 2006), oxidized Ta_2Si (A. Pérez-Tomás *et al.*, 2004), Al_2O_3 (Cheong, 2007; Tanner *et al.*, 2007; Tanner *et al.*, 2007), AlN (Wolborski *et al.*, 2006), La_2O_3 (Moon *et al.*, 2006), ZrO_2 (Karlsson *et al.*, 2007; Kurniawan *et al.*, 2011), HfO_2 (Hullavarad *et al.*, 2007; Wolborski *et al.*, 2007; Wang and Cheong, 2008), CeO_2

(Lim *et al.*, 2010; Chuah *et al.*, 2011; Lim *et al.*, 2011), and Y_2O_3 (Quah *et al.*, 2011). The *J-E* characteristics of various high-κ gate oxides on 4H-SiC are re-plotted, using a linear approximation method in Figure 2.4. Based on this figure, the breakdown field of ZrO_2 on 4H-SiC is considerably low, with higher leakage current compared to other gate oxides. Therefore, in this study, it is postulated that simultaneous thermal oxidation and nitridation technique may enhance the breakdown field and lower the leakage current.

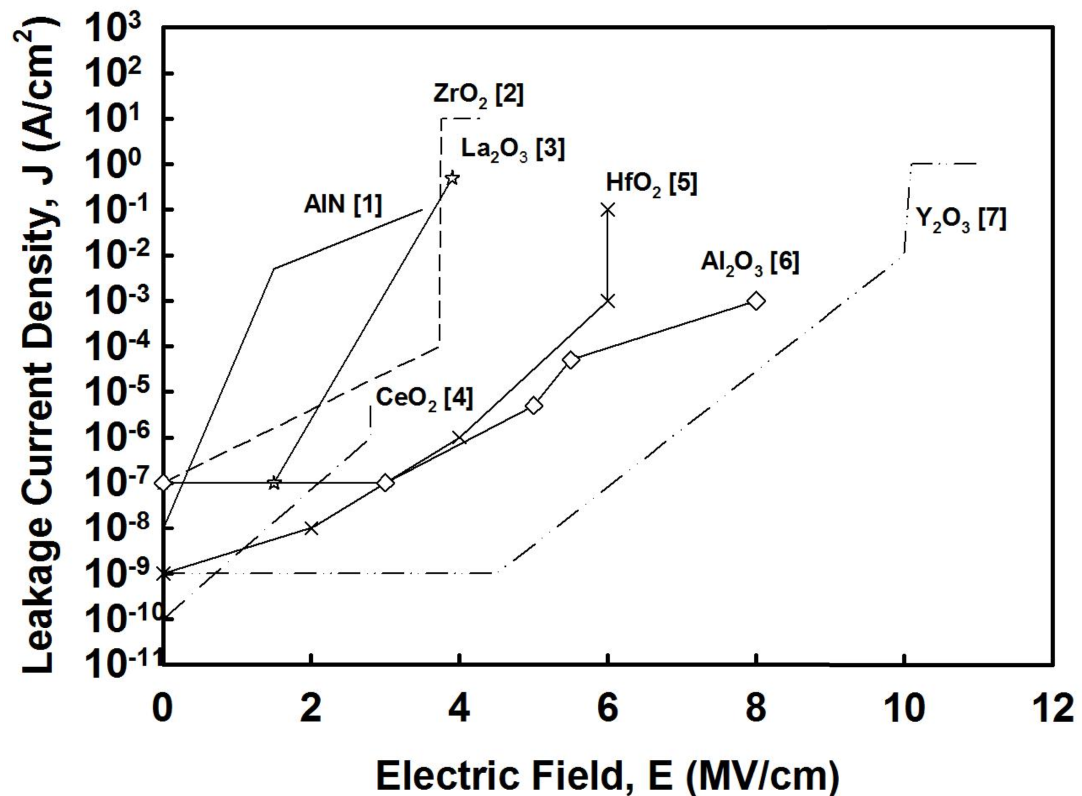

Figure 2.4: Comparison of *J-E* characteristics of various metal/high-κ gate oxide/4H-SiC MOS capacitors reported in the literature.

References: [1] = Wolborski *et al.*, 2006; [2] = Kurniawan *et al.*, 2011; [3] = Moon *et al.*, 2006; [4] = Lim *et al.*, 2011; [5] = Wolborski *et al.*, 2007; [6] = Tanner *et al.*, 2007; [7] = Quah *et al.*, 2011.

In short, down scaling of device dimensions is not the driving force for development of SiC-based power devices. Instead, the motivation for the study of alternative high-κ gate oxides on SiC is to extend the performance capabilities in high power, high temperature, and/or high radiation applications.

2.7 ZrO_2 as an Alternative High-κ Gate Dielectric

2.7.1 Electrical Properties of ZrO_2: Dielectric Constant (κ) Value and Band Offsets

As mentioned, κ value is the first requirement in order to select a material for gate oxide application. As a promising candidate for the mentioned application, it must have a significantly higher κ value than SiO_2, with preferable values of between 10 and 30 (Robertson, 2004; Houssa *et al.*, 2006; Robertson, 2006; Guha and Narayanan, 2009). If the κ value of a material is too high, for example, TiO_2 ($\kappa \sim 80$) (Wilk *et al.*, 2001; Wallace and Wilk, 2003; Robertson, 2004; Robertson, 2006; Wong and Iwai, 2006) will cause fringing field from the drain through the gate dielectric. The fringing field can degrade the source-to-channel potential barrier, thus possesses poor subthreshold performance (Cheng *et al.*, 1999; Mohapatra *et al.*, 2001; Mohapatra *et al.*, 2002; Wong and Iwai, 2006; Ji *et al.*, 2008), which is undesirable. As a potential candidate for gate dielectric application, ZrO_2 has high enough κ value, i.e., 22–25 (Thompson *et al.*, 1992; Wilk *et al.*, 2001; Wallace and Wilk, 2003; Robertson, 2004; Robertson, 2006; Wong and Iwai, 2006).

In addition to high κ value, a promising candidate for high-κ dielectrics must have large band offsets. Band offset between an oxide and Si semiconducting

substrate can be defined as the barrier for holes or electrons to be injected into the oxide (Franciosi and Van de Walle, 1996; Robertson and Peacock, 2004), and it is closely related to band gap of material, whereby material with larger bandgap will correspond to larger band offset. By having large band offsets, the carrier generation and conduction can be minimized (Wilk *et al.*, 2001; Robertson, 2002; Wallace and Wilk, 2003). This criterion is essential as it helps to suppress the leakage current (Wong and Iwai, 2006). From the periodic table of elements, as the atomic number of an element increases, the ionic size (radius) of an element increases but the ionic bonding force (cohesive force) decreases. This results a high dielectric constant but a narrow bandgap (Boer, 2002). Subsequently, material with higher κ value has lower band offset value. According to Clausius-Mossotti equation, the inverse relationship between energy bandgap and dielectric constant can be clearly demonstrated (He *et al.*, 1999), as shown in Equation (2.2).

$$E_g \approx 20 \bullet [3/(\kappa+2)]^2 \tag{2.2}$$

where, E_g is the energy bandgap and κ is the dielectric constant value.

Besides having high κ value, ZrO_2 has reasonably high band offsets as well, i.e., 5.8 – 7.8 eV, with its electron offset or conduction band offset (ΔE_c) values of 1.2 – 1.5 eV (Wilk *et al.*, 2001; Robertson, 2002; Robertson, 2002; Bonera *et al.*, 2003; Wallace and Wilk, 2003; Wu *et al.*, 2003; Robertson, 2004; Robertson and Peacock, 2004; Robertson, 2006), depending upon deposition conditions. Therefore, when ZrO_2 (with $\Delta E_c > 1.0$ eV) is used, carrier generation (electron transport) can be reduced, either from enhanced Schottky emission, thermal emission, or tunnelling.

This will reduce leakage current. Figure 2.5 illustrates a simple schematic diagram to show bandgap and band offsets of ZrO_2 and carrier injection mechanism in its band states when coupled with Si (Robertson, 2004; Robertson, 2006; Wong and Iwai, 2006). If an *n*-type Si is used, a potential barrier [conduction band (CB) offset] of 1.2 – 1.4 eV must be overcame in order to induce conduction by Schottky emission of electrons into the ZrO_2 band. On the other hand, if a *p*-type Si is used, a potential barrier [valence band (VB) offset] of 5.8 – 7.8 eV must be overcame in order to induce conduction by Schottky emission of holes into the ZrO_2 band.

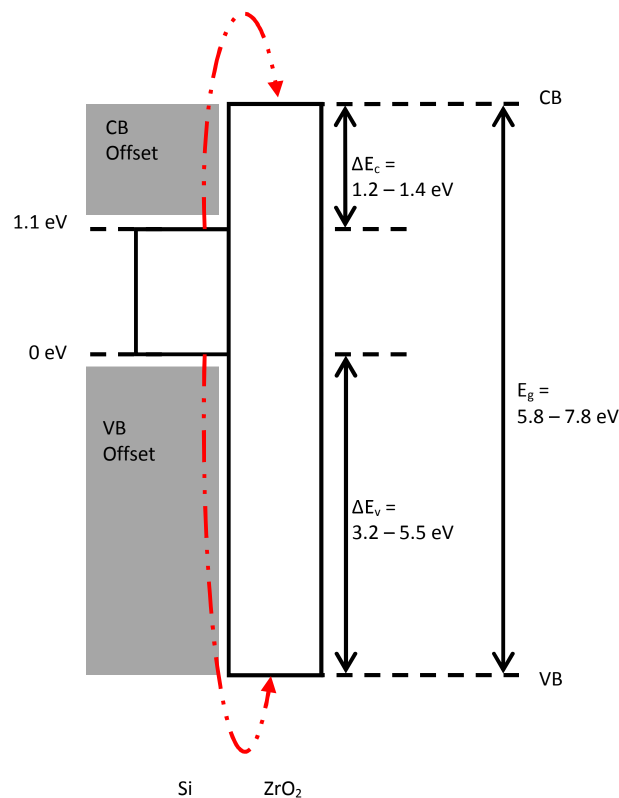

Figure 2.5: Simple schematic of bandgap and band offsets of ZrO_2 and carrier injection mechanism (red dotted lines) in its band states. CB = Conduction Band, VB = Valence Band (Robertson, 2004; Robertson, 2006; Wong and Iwai, 2006).