SIMULATION OF UNDERFILL ENCAPSULATION OF ELECTRIONIC PACKAGING USING THE LATTICE-BOLTZMANN METHOD

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by

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LIST OF SYMBOLS

ϵ	Volume fraction
ρ	Density
σ	Standard deviation
τ	Relaxation factor
Ω	Collision operator
ω	Collision frequency
$\mathbf{e}$	Microscopic velocity
A	Interrogation matrix
B	Interrogation matrix
C	Cross-correlation function
L	Reference length
M	Mass content
c	Basic speed of lattice
f	Single particle distribution equation
i	Coordinate in horizontal axis
j	Coordinate in vertical axis
t	Time
u	Velocity
w	Weight
x	Position

LIST OF ABBREVIATIONS

BGA	Ball Grid Array
BGK	Bhatnagar-Groos-Krook
CFD	Computational Fluid Dynamics
DCC	Direct Cross Correlation
DFT	Discrete Fourier Transform
DPIV	Digital Particle Image Velocimetry
EMC	Epoxy Moulded Compound
FE	Finite Element
FEM	Finite Element Method
FVM	Finite Volume Method
IC	Integrated Circuit
IDE	Integrated Development Environment
LBM	Lattice-Boltzmann Method
LED	Light Emitting Diode
MPI	Message Passing Interface
N-S	Navier-Stokes
PCB	Printed Circuit Board
PIV	Particle Image Velocimetry
SMT	Surface Mount Technology
SPH	Smoothed Particle Hydrodynamics
TSV	Through-Silicon Via
VOF	Volume of Fluid

SIMULASI PENGKAPSULAN ISIAN BAWAH PAKEJ ELEKTRONIK MENGGUNAKAN KAEDAH KEKISI BOLTZMANN

ABSTRAK

Kebanyak kajian berasaskan kaedah isipadu terhingga (FVM) telah dilaksanakan untuk mengoptimumkan dan memperbaiki proses pengkapsulan isian bawah. Namun, terdapat kajian yang terhad telah dilaksanakan dengan kaedah kekisi-Boltzmann (LBM) untuk aplikasi yang berkaitan dengan pengkapsulan isian bawah. Dalam kajian ini, LBM akan digunakan untuk mensimulasikan proses pengkapsulan untuk sendi pateri yang berlainan bentuk, penyusuan sendi pateri dan cara dispens. Sesetengah keputusan simulasi yang diperolehi dengan LBM akan dibandingkan dengan keputusan yang diperolehi daripada eksperimen pengimejan velocimetri partikel (PIV). Keputusan yang diperolehi daripada simulasi LBM dan eksperimen PIV adalah lebih kurang seiras. Dari segi penyusunan sendi pateri, adalah didapati bahawa penyusunan jajaran keliling memberikan masa pengisian yang paling singkat berbanding dengan penyusuan jajaran kosong tengah dan penuh. Bagi kaedah suntikan berbeza, adalah didapati bahawa kaedah penyutikan jenis U memberikan pengurangan masa pengisian sebanyak 67% berbanding dengan penyuntikan jenis I. Namun, ruang kosong yang besar dibentuk dengan kaedah suntikan jenis U. Suntikan jenis L pula menunjukkan pengurangan masa isian sebanyak 45% tanpa formasi ruang kosong makro. Di samping itu, kesan bentuk sendi pateri yang berbeza juga dikaji. Jajaran sendi pateri dengan sendi berbentuk jam pasir berjaya mengurangkan masa pengisian sebanyak 10% sambil menghasilkan ruang kosong yang lebih kecil. Sendi pateri berbentuk silinder tidak menunjukkan sebarang penambahbaikan yang ketara kepada masa pengisian kalau dibandingkan dengan pengisian bawah dengan sendi pateri

konvensional yang berbentuk sfera terpenggal. Isian bawah tekanan dapat mengurangkan masa pengisian sehingga 99% berbanding dengan isian bawah konvensional. Tekanan maksimum dalam domain aliran adalah lebih kurang 2.5 hingga 3 kali lebih tinggi daripada tekanan masuk semasa isian bawah yang disebabkan oleh pembinaan tekanan.

SIMULATION OF UNDERFILL ENCAPSULATION OF ELECTRONIC PACKAGING USING LATTICE-BOLTZMANN METHOD

ABSTRACT

Many finite volume method (FVM) based studies had been conducted by researchers to optimize and improve the underfill encapsulation process. However, there are limited studies conducted using lattice-Boltzmann method (LBM) for underfill encapsulation process. In this study, LBM will be used to simulate the encapsulation process of different solder joint shapes, different solder joint arrangements and injection methods. Some of the simulation results obtained using LBM will then be compared with the results obtained from experiment using particle image velocimetry (PIV) method. High conformity were obtained from both LBM and PIV results. In terms of the solder ball arrangements, perimeter arrangement was found to give the shortest filling time compared to middle empty and full arrangements. As for different injection methods, it was found that U-type injection gives a 67% reduction of filling time compared to I-type injection. However, a huge void is formed with U-type injection. Meanwhile, L-type injection shows a 45% reduction of filling time with no macro void formed. Furthermore, the effect of different solder joint shapes are also studied. Solder joint array with hourglass shape solder joints managed to reduce the underfill filling time by around 10% while yielding a smaller void. Cylindrical shape joints did not show any significant improvement on the filling time compared to that with truncated sphere shape joints. Pressurised underfill was found to reduce filling time by up to 99% compared to conventional underfill. The maximum pressure within the flow domain was found to be approximately 2.5 to 3 times higher than the inlet pressure during pressurised underfill due to pressure build-up.

CHAPTER ONE
INTRODUCTION

1.1 Introduction

The constant demand by consumers for better performing electronic devices in smaller footprints had led constant innovation by engineers to fulfil such demand. Thus, integrated circuit packages of compact size, high reliability and high performance are required to cope with such stringent requirements. Quality and reliability of the package pose as a concern as we continue the drive towards miniaturisation of integrated circuit package. This is where the study of electronic packaging comes into place.

Electronic packaging is an engineering discipline which sought to provide enclosure and protective features which can be built onto electronic products and components. During the service lifetime of an electronic product, they are constantly being exposed to various environmental factors like heat, humidity and vibrations. Exposure to such factors are detrimental, and could potentially lead to failure of such electronic devices. In order to ensure the longevity of an electronic devices, it is essential to protect the electronics from such constant exposure.

Electronic components can be classified into hierarchies based on its level of packaging level as shown in Figure 1.1. The first level packaging provides interconnection between the IC chips with the module. A second level packaging provides an interconnection between the first level electronic package to a PCB. Fulfilling such connection could be completed either with through hole technologies or surface mount technologies. The assembly could be coated with a polymer layer to provide additional protection towards them. Third level packaging can be realized by interconnecting several of those second level packaging onto a motherboard. A fourth level packaging would have the motherboad, together with its interconnected second level packaging, being assembled into its fixture or casing such to become a final product like a computer or a CD player, which could be used by the end user.

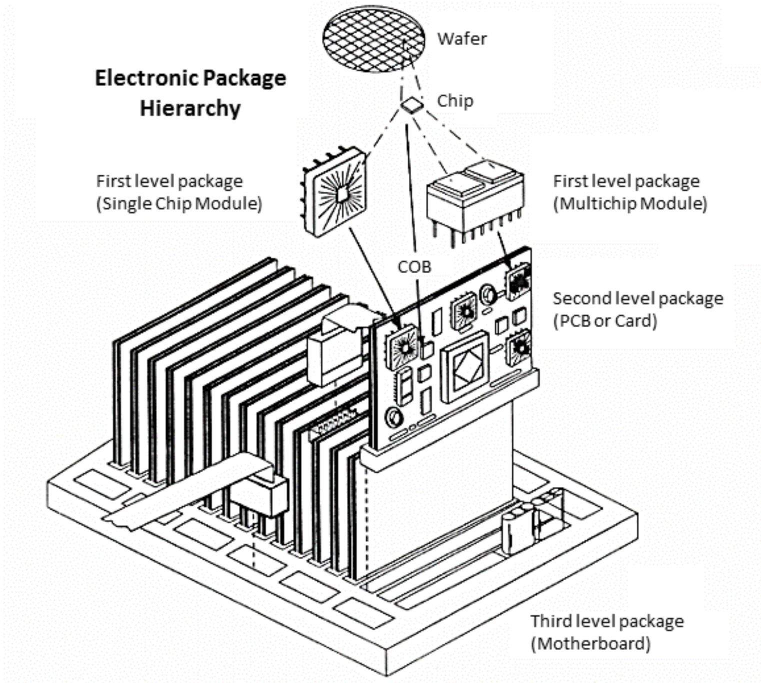

Figure 1.1: Electronic Packaging Hierarchy (Lau, 1994)

In this study, we are going to focus on the second level packaging, specifically, BGA encapsulation using underfill process. In SMT, small, intricate electronic components are mounted onto the surface of PCB without the need of through-hole mounting. BGA, being a type of SMT, utilizes small solder balls to form connection between the electronic components with the PCB. BGA outshines its SMT counterparts like pin grid array as it allows for higher interconnection density, better performance due to shorter leads, and better heat conduction. Figure 1.2 shows the arrangement of solder balls under an Intel Embedded Pentium MMX Processor.