IMPROVING THE PERFORMANCE OF AN EQUIPMENT ENGINEERING GROUP IN A WAFER FOUNDRY

by

PALANIAPPA A/L SUBRAMANIAM

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Table of Contents

Acknowledgement …………………………………………………...ii

Table of Contents……………………………………………………iii

List of Tables…………………………………………………………v

List of Figures………………………………………………………...vi

List of Abbreviation…………………………………………………viii

Abstrak…………………………………………………………………..ix

Abstract………………………………………………………………….x

Executive Summary…………………………………………………..xi

1.0 Introduction……………………………………………………….1

2.0 Industry Background……………………………………………..10

3.0 Company Background……………………………………………15

3.1 Company Overview………………………………………….…15

3.2 Vision…………………………………………………………...17

3.3 Mission………………………………………………………....18

3.4 Organization Structure…………………………………………18

3.5 Description of the Wafer Fabrication Process……………….20

3.6 Description of the department and the persons involved….…23

4.0 Case Issues……………………………………………………...27

5.0 Case Analysis…………………………………………………..…31

5.1 Failure Mode 1…………………………………………………32

5.2 Failure Mode 2………………………………………………....42

5.3 Failure Mode 3…………………………………………………47

5.4 Failure Mode 4………………………………………………....51

5.5 Failure Mode 5…………………………………………………56

5.6 Failure Mode 6……………………………………………61

5.7 Input-Process-Output model summary of root-cause…….64

6.0 Discussion and Recommendation…………………………………....68

6.1 Structure of recommendations…………………………….....68

6.2 Recommendation 1 : Human Capital Development………69

6.3 Recommendation 2: Knowledge Management…… ………..71

6.4 Recommendation 3: Improving Systems…………………....73

6.5 Other Recommendations……………………………………....74

7.0 Conclusion………………………………………………………...76

8.0 References…………………………………………………………78

9.0 Appendix…………………………………………………………..79

List of Tables

		Page
Table 1.1	Ranking of Pure-Play Foundry Companies based on Sales Revenue, 2012	3
Table 1.2	Etch Equipment Group Description	7
Table 5.1	Summary of Low Uptime Occurrences by Failure Mode for Etch Tools	31
Table 5.4.1	Benchmarking of Head Count to Tool Ratio with Fab I	55

List of Figures

		Page
Figure 1.1	The Etch module critical tool Uptime performance trend for Q3	7
Figure 1.2	Overall Equipment Wafer Scrap Trend by Department	8
Figure 2.1	The Semiconductor Value Chain	11
Figure 2.2	2013 Top 20 Semiconductor Sales Leaders	12
Figure 2.3	Ranking of Pure-Play Foundry Companies based on Sales Revenue for 2012	14
Figure 3.1	Silterra Design Service Partners Network	17
Figure 3.4.1	Silterra (M) Sdn. Bhd. Senior Management Organization Chart	19
Figure 3.4.2	Fab Operations Management Teams Organization Chart	19
Figure 3.5.1	A zoom in on ASIC wafer construction.	20
Figure 3.5.2	Wafer Fabrication Process Loop and the Departments involved	21
Figure 3.5.3	Scanning Electron Microscope Picture of a completed ASIC Chip	23
Figure 3.6.1	Etch Department Organization Chart	29
Figure 4.1	The Etch Department Organization Chart in second quarter of 2014.	29
Figure 4.2	Etch Department Organization chart from third quarter of 2014	30
Figure 4.3	The Etch module critical tool Uptime performance trend for Q3	32
Figure 5.1	Macro Failure Modes for Poor Tool Uptime in Etch Module	32

Figure 5.1.1	Etch Tool Maintenance Success Rate Trend for Q3 2014	34
Figure 5.1.2	Failure Mode 1 Why-Why Analysis (Figure part 1 of 5)	35
Figure 5.1.2	Failure Mode 1 Why-Why Analysis (Figure part 2 of 5)	36
Figure 5.1.2	Failure Mode 1 Why-Why Analysis (Figure part 3 of 5)	37
Figure 5.1.2	Failure Mode 1 Why-Why Analysis (Figure part 4 of 5)	38
Figure 5.1.2	Failure Mode 1 Why-Why Analysis (Figure part 5 of 5)	39
Figure 5.2.1	Failure Mode 2 Why-Why Analysis (Figure part 1 of 2)	45
Figure 5.2.1	Failure Mode 2 Why-Why Analysis (Figure part 2 of 2)	46
Figure 5.3.1	Failure Mode 3 Why-Why Analysis (Figure part 1 of 2)	49
Figure 5.3.1	Failure Mode 3 Why-Why Analysis (Figure part 2 of 2)	50
Figure 5.4.1	Failure Mode 4 Why-Why Analysis	54
Figure 5.5.1	Failure Mode 5 Why-Why Analysis (Figure part 1 of 2)	58
Figure 5.5.1	Failure Mode 5 Why-Why Analysis (Figure part 2 of 2)	59
Figure 5.6.1	Failure Mode 6 Why-Why Analysis	63
Figure 5.7.1	IPO model summary of Root Causes for Poor Tool Uptime.	64
Figure 6.1.1	Summary of Root causes that will be addressed by each area of recommendations.	68
Figure 7.1	The Vicious Cycle in which the Etch Equipment Team is trapped in.	77

List of Abbreviations & Glossary

ASIC – Application Specific Integrated Circuits

CMP – Chemical mechanical planarization department that polishes the semiconductor wafer in the factory.

CVLA – A group of Etching equipment designed to etch insulator layers.

Design IP – Intellectual property in the form of circuits designs

Etch – Etching department that uses plasma to physically remove selected material from the semiconductor wafer to build the physical circuit in the factory.

Fab – A semiconductor wafer manufacturing facility

Fabless – A company that does not have a semiconductor wafer manufacturing facility

Foundry – A contract semiconductor wafer manufacturing facility that does not produce their own products.

IDM – Integrated Device Manufacturers like Intel, Infineon and Texas Instruments.

IE – Industrial Engineering department

MEAM – A group of Etching equipment designed to etch conductor layers.

MELA – A group of Etching equipment designed to etch conductor layers.

POLY – A group of Etching equipment designed to etch poly-silicone layers.

TFD – Thin Films Dielectric department that deposits insulator layers on the semiconductor wafer in the factory.

TFM – Thin Films Metal department that deposits conductor layers on the semiconductor wafer in the factory.

IMPROVING THE PERFORMANCE OF AN EQUIPMENT ENGINEERING GROUP IN A WAFER FOUNDRY

Abstrak

Kajian ini memberi tumpuan kepada satu jabatan dalam perniagaan pembuantan wafer IC, di mana produk akan melalui beberapa kali laluan melalui setiap jabatan sebelum melengkapkan kitaran pembuatan. Pelan kajian adalah untuk mendedahkan bagaimana prestasi Uptime peralatan boleh diperbaiki untuk membantu syarikat mencapai sasaran pembuatan. Kajian in menggunakan Fishbone dan analisis Why-Why untuk mendedahkan punca sebenar yang mengakibatkan Uptime peralatan your rendah, kaedah Benchmarking digunakan untuk membandingkan kekuatan sumber manusia dengan satu lagi perniagaan pembuatan wafer IC yang berjiranan dan menggabungkan segala penemuan menggunakan Input-Proses-Outpout (IPO) untuk memberi gambaran yang lengkap terhadap masalah Uptime yang rendah. Model IPO (McGarth 1964) memberikan gambaran yang menyeluruh daripada aspek interaksi dan kepututsan. Sumber maklumat data ialah dari ukuran indeks prestasi peralatan dan temubual dengan pihak-pihak yang berkaitan. Hasil kajian boleh dikaitkan dengan teori pembangunan modal insan dan keperluan untuk mengimbangi aktiviti proaktif dengan aktiviti reaktif .Kajian ini menyediakan analisis yang komprehensif tentang punca-punca masalah Uptime rendah dengan menggunakan model IPO supaya punca sebenar ditangani dan bukan punca syptomatic. Cadangan-cadangan mempunyai lengkung pembelajaran dengan keuntungan jangka pendek yang lebih perlahan tetapi keuntungan jangka panjang yang lebih besar dengan membina budaya yang betul.

IMPROVING THE PERFORMANCE OF AN EQUIPMENT ENGINEERING GROUP IN A WAFER FOUNDRY

Abstract

The study focuses on a single department in a wafer foundry business where the product goes through multiple passes through each department before completing the manufacturing cycle. The study plan is to uncover how the equipment uptime performance can be improved to help the company achieve the required production numbers.The analysis uses the Fishbone and why-why analysis to uncover the true root cause of the poor tool uptime performance, the benchmarking tool for comparing human capital numbers with a neighbouring wafer production facility and consolidates the findings using Input-Process-Outpout (IPO) model for a complete picture of the problem. The IPO model (McGarth 1964) gives a comprehensive view of a teams interactions and outcomes. Source of information has been primary data from the companies internal equipment indices and interview with the relevant parties. The findings can be related to the theory of human capital development and the need for balancing proactive activities of improvments to reactive activities of fixing issues.This study provides a comprehensive analysis of a teams working using the IPO model so that the true root causes are addressed instead of syptomatic causes. The recommendations have a learning curve with a slower short term gain but a greater long term gain by building the correct culture.

Keywords: Wafer foundy; Etch module; IPO model; Human Capital Development.

Executive Summary

The case focuses on one particular module named Etch in a wafer foundry in Malaysia to study and evaluate how the equipment engineering team can improve their performance to deliver the required tool uptime to meet the companies production needs. The companies targeted wafer production for the fourth quarter can only be achieved if the Etch Tool Uptime meets the 87% target. The companies financial standing of profit or loss for 2014, premium paying customers' satisfaction and a one month base salary bonus payout for all employees depends on this Etch modules performance in the fourth quarter of 2014. The team did not achieve the targets for the third quarter and has caused a lot of problems for the management and the unhappy staff who did not get a bonus payout. The analysis and research is based on the Etch Equipment teams third quarter performance data. The data is analyzed using the fishbone analysis to understand the macro failures and then unpeel the root causes of each macro failure using a why-why analysis. Then the Input-Process-Output model is used to consolidate all the root causes to get a wholesome view of the problem and understand how the root causes are intertwined and interact. The root cause was determined to be firstly caused by new hires replacing experienced manpower are incapable of delivering the quality and quantity of work required. The second major root cause was the experienced manpower was being stretched to the limits and some have hit the breaking point and left the company. Third cause was the poor documentation of procedure and troubleshooting guides that did not allow the new hirers to learn from the experienced manpower and thus the team did not grow and compound their knowledge. Fourth root cause was that there were systematic issues in the parts monitoring and pass down that inhibited efficient pass

over of information. Final root cause was noted that the team was lacking the motivation to improve. There were 3 main recommendations given. First was to focus on human capital development by conducting a training needs analysis to come up with a training plan that is able to feed the knowledge, skills and attitude required for the new hires to be effective team players. The second recommendation was to improve and compound the team learning by hiring a programmer to build a database from all the teams experience and extend it to become an expert system. The final recommendation was to improve on the pass down and parts monitoring system to reduce the systematic issues observed in the department. In conclusion, the Etch Equipment team was stuck in a vicious cycle that begins with the lack of experienced manpower for tool maintenance activities and hence the experienced manpower must only focus on tool recovery. This leads to a lack of time to focus on proper training and developing the human capital. This in turn reduces the overall team efficiency and the quality of work done by the new hires and finally stretches the experienced manpower until they chose to leave. It is vital that the Etch module breaks this cycle by deliberately allocating resources to work proactively and not just reactively.

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1.0 Introduction

Mr.K is a deputy director in a Semiconductor Wafer Foundry (factory) based in Kulim. He has over 20 years of work experience in the industry and was hand-picked by the senior management and hired from Korea 5 years ago to be a senior manager in the factory. He was then in-charge of a operation department named Photo. In every wafer foundry, the primary production line is made up of 8 operations department that specialize in one category of processes on the wafer. These 8 departments are called Photo, Etch, Diffusion, Implant, Thin Films Dielectric (TFD), Thin Films Metal (TFM) and Chemical Mechanical Planarization (CMP).

Mr.K was known to be a high performance manager who always achieved his targets and well liked by his subordinates. He was a very hands-on and analytical manager. In 2012 he was promoted to the position of deputy director and was assigned an additional operation department named Etch together with the Photo department. Initially Mr.K took some time to understand the inner working of the Etch process but soon enough he was able to grasp the fundamentals to manage the department.

As Mr.K was preparing for the quarterly performance review for the third quarter (Q3) of 2014, he was very disappointed with the performance of the Etch department. The department was not able to deliver the committed tool performance required to meet the production needs. Mr.K knew that the Etch department's under performance had a negative impact on the companies business plan and customers on-time delivery in Q3.He also suspected that Etch could be the cause of the whole company loosing their bonus payout for that quarter. He was very nervous going in to the Quarterly Performance board review meeting.

Companies Business Outlook at the beginning of Quarter 3

The Board of Director of Silterra (M) Sdn. Bhd announced on 25th of June 2015 that the semiconductor industry is having a market rebound and the ordering rate from the customers are increasing during the employee quarterly engagement session. By first week of July 2015, it was announced that the factory has secured enough orders for the next 3 quarters to fill the line up close its maximum capacity.

The target for Q3 (July, August & September) was a total of 78000 wafers produced. The factories full loading capacity based on the current installed tools is actually 82000 wafers per quarter which is higher then the current goal. This goal was then divided into monthly targets as follows, 25000 wafers produced in July, 26500 wafers produced in August and 26500 wafers produced in September. The Operations and Manufacturing team was confident that these numbers could be met as the factory had sufficient capacity to cater for this volume of production without any hiccups.

Importance of Quarter 3 performance

This orders was a welcomed news since in the first 2 quarters of 2014, the orders were very low and half the tools in the fab were idling. The company went into a very tight cash flow situation and backlog of payments increased to the suppliers. Many of the tools that had problems or maintenance that required the purchase of expensive spare parts were put on hold. This third and fourth quarter orders will bring back the required cash flow to the company.

It was also important for the company to meet the third and fourth quarter targets to make sure the company's accounts was making profits with positive cash flows since Silterra was making significant losses in the first 2 quarters. If not the company will be in losses for the year ending 2014. This would look very bad to the board of directors to whom the management has committed that even if the company does not make a huge profit, it will not make any losses. The current management team which has held the helm of the company since 2011 has been able to keep the companies cash flow self sufficient annually until this year, the Q3 and Q4 orders has given the company a chance to redeem the 2014 numbers.

Another point is, based on Table 1.1 that shows the Ranking of Pure-Play Foundry Companies based on Sales Revenue for 2012. (Source: Insights, Company reports), Silterra is only ranked in the 15th position with a sales of US$213 million in 2012.

Table 1.1: Ranking of Pure-Play Foundry Companies based on Sales Revenue, 2012

Rank	Company (Headquarters Location)	2012 Sales (US $million)
1	TSMC (Taiwan)	17167
2	GlobalFoundries (US)	4560
3	UMC Group (Taiwan)	3730
4	SMIC (China)	1682
5	Hua Hong Grace (China)	940
6	Tower Jazz (Israel)	644
7	Vanguard (Taiwan)	582
8	Dongbu HiTek (S.Korea)	540
9	WIN (Taiwan)	382
10	SSMC (Singapore)	370
11	X-Fab (Europe)	260
12	Altis (Europe)	228
13	Telefunken (Europe)	220
14	He Jian (China)	215
15	Silterra (Malaysia)	213

Source: Insights, Company reports 2012

In Table 1.1, the top 8 foundries have businesses that are double the value of what Silterra has. This also shows that these foundries have bigger capacities and will be able to meet customer demands. Hence Silterra's ability to generate revenue in this business is lower due to its size and smaller capacity, Customers with big bulk orders will not be keen in doing business with Silterra. Silterra is also qualified only as secondary source or back-up source for many customers. Customers's first choice for capacity sake will always be the top 8 in Table 1.1. This means, Silterra rarely has the pricing power and has to sell below market leader pricing in order to get consistent orders. However in the Q3 and Q4 orders, the Sales team and Business Planning unit have confirmed that customers are offering premium price for on time delivery. Hence the company must meet the output to satisfy and retain these premium customers. It becomes vital for the companies business sustainability.

Incentive to meet Q3 targets

By now it was clear that failure to meet the targets was not an option. In order to motivate the employees and achieve the business plan, the board of directors announced a Performance Incentive Payout of One month base salary for every quarter if the targeted number of wafers produced is achieved for each quarter. This translates to 3 months bonus for all employees.

Q3 Business Performance

The actual wafers produced for the month of July was 22000, in August the number was 23500 and in September the number was again only 24000. Hence the total wafers produced for the quarter was 69500 wafers only as compared to the business plan of 78000 wafers. The factory fell short of 8500 wafers from its target for Q3.

Problems in achieving Q3 Targets

The wafer production capacity is planned and controlled by a team called the Industrial Engineering (IE) team. This team is tasked to study how long each tool takes to process wafers and plans how many tools are required at each processing step in order to achieve the targeted output. The wafer processing is a looped process across 8 different departments, where one raw wafer will go through each department multiple times before the product is complete. In order to calculate the capacity and cycle time (time required) to produce the wafers, the IE team has fixed the required tool productivity measurement called tool uptime which represents the amount of time in a month the tool is running production. This up time target numbers is statistically calculated by measuring the actual run time of processes on each tool and giving buffer time for tool errors and issues. The IE team is tasked to monitor and understand how the wafers in the production line are moving through each module and recommend additional tool purchases if the module becomes a bottle neck for a smooth flow of wafers.

Once the Q3 targets were not met, the IE team was immediately tasked to perform a post mortem of the line performance to understand why the targets could not be met. Each process module in the production line was analyzed and evaluated against their

committed tool uptime requirement. This is a crucial analysis cause for a production line that involves 400 processing steps across 8 different department of processes run using more then 30 types of tool sets, to see where did the wafer's movement slow down?

On the 3rd of October during the Quarterly Performance Board Review Meeting meeting, Dr. A the Vice-President of operations declared in the meeting that Silterra has Failed to meet the Q3 targets and hence there will be no Bonus for all employees. Dr.A presented the **IE teams findings** on the factories poor performance and directly pointed out the Etch department for **poor tool uptime** as the major reason for not meeting the targets.

Etch Tool Uptime Performance – IE Data

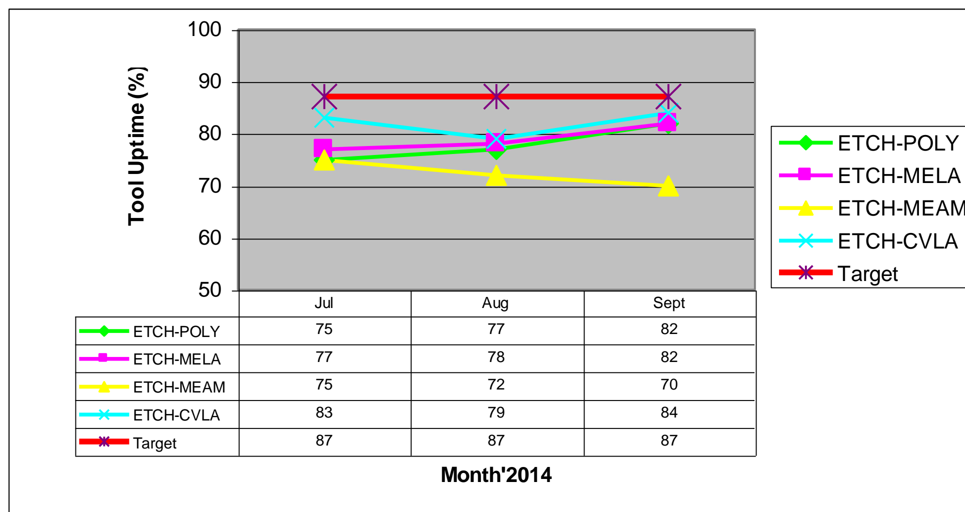
One of the key Tool performance monitoring parameter is the Tool Uptime which measures in percentage how long the tool was running production material in a month. It is a measure of a tool's productivity. This uptime percentage will be lower if the tool is down for any maintenance activities or equipment failure. Standard preventive maintenance activities are taken into consideration when setting the tool uptime targets. The business planning unit will factor in all the tools uptime targets during capacity calculations and order acceptance. Based on historical performance and Fab standards, the average target for Etch Tool Uptime is set at 87%.

The Etch Department has 4 critical tool groups which are made up of identical equipment make and configurations. Each group runs a set a specified materials and processes. The name and breakdown of each group is as listed in Table 1.2.

Table 1.2: Etch Equipment Group Description

Tool Group Name	Number of Tools	Daily Capacity Per Tool	Target Uptime	Description of process
ETCH-POLY	7	500 wafers	87%	Front-End Oxide Material Etching
ETCH-MELA	7	500 wafers	87%	Back-End Conductor Material Etching
ETCH-MEAM	4	550 wafers	87%	Back-End Conductor Material Etching
ETCH-CVLA	8	600 wafers	87%	Back-End Oxide Material Etching

Based on IE data, all 4 of the critical tool groups in the Etch module did not meet the committed uptime of 87% or more for the whole third quarter as shown in Figure 1.1. Given the nature of wafer processing steps; which must be in sequential, any move loss at a single step is very difficult to be recovered and can be considered as wasted capacity.



	Jul	Aug	Sept
ETCH-POLY	75	77	82
ETCH-MELA	77	78	82
ETCH-MEAM	75	72	70
ETCH-CVLA	83	79	84
Target	87	87	87

Figure 1.1: The Etch module critical tool Uptime performance trend for Q3
(Data Source: Internal Data; Extracted from the Industrial Engineering production indices dashboard)

Etch Equipment also caused material scraps

Dr. A also added that the problem was further compounded by the high material scrap rates in the factory. Already the tool is not producing the required number of wafers as it should but, to add to this, the wafers that were produced does not meet

the quality specifications and must be scrapped in the line. In a wafer foundry there is a strict quality requirement in terms of output measurements and defect performance. If at a particular step the output measurements or defect performance do not meet the specifications, then the material is not fit for the next process as it will not yield a saleable product. Hence the Quality department will scarp the material. The Quality manager then presented the tool related scrap trend of the factory as shown in Figure 1.2. The data pointed towards poor tool performance by the Etch Module which had the highest scrap percentage amongst the 8 departments in Q3.

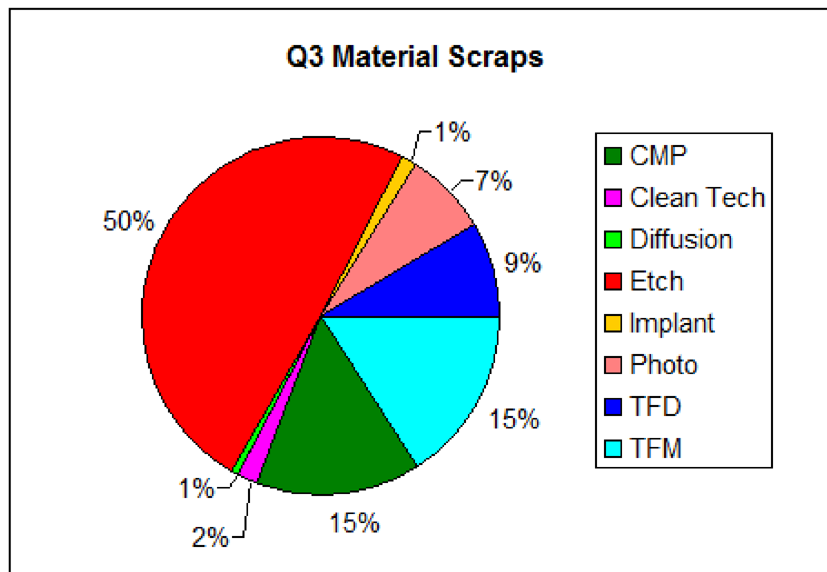


Figure 1.2: Overall Equipment Wafer Scrap Trend by Department
(Data Source: Internal Data; Extracted from the Quality Assurance Quarterly Scrap Report)

Etch modules required actions

Dr.A then looked at the Deputy Director of Etch module, Mr.K and told him to improve the tools performance to meet the committed uptime and performance so that the company does not make a financial loss for 2014. Dr.A stressed that the plan and commitment of the management to the Board of Directors now rested in the

hands of the Etch module. It was not possible for the management team to help buy additional tools to ease the problem at etch cause new tools take 6 months for delivery and another 6 months to be ready for production. At this juncture, for the company to achieve the production targets and meet the customer delivery commitments can only be achieved if the Etch Tools are running production lots as per the target uptime of 87% accurately. Mr.K took heed of the request and understood that the Financial outcome for 2014, customer on-time delivery to maintain premium customers and the quarterly one month bonus for all the employees of the company depended on the Etch Tool Uptime. Mr.K realized that drastic measures and immediate actions were required. But before that he had to understand what is causing these poor tool uptime?

The Research Questions.

Mr.K was in a dilemma and had to understand and find answers for the following questions?

What are the reasons behind the poor tool uptime performance and how can these issues be addressed?

Are the poor uptime issues across the 4 different tool groups caused by similar or different root causes?

Why are the tools output not meeting the quality standards and causing scrap?

2.0 Industry Background

The semiconductor industry started with the discovery of transistors by Bell Laboratories in 1948. The transistor was an electronic switch which can be connected in multiple combinations to make complex decisions in an electronic circuit. Almost a decade later in the late 1950's the next big discovery in semiconductors came about called integrated circuits. These integrated circuits were basically a large number of transistors built on a silicone chip. Over the years the number of transistors on these chips increased dramatically from Intel's first commercial processor, which are "computers on a chip", containing only 3500, until the current ability to jam as many as 5.5 million transistors. Texas Instruments claims that it has a technology available by which 125 million transistors can be packed on one chip. By the early 1970's it was possible to incorporate very complicated solid-state circuits on one single chip the size of a finger-nail to create the microprocessor. These tiny microprocessors were so tiny that a single of them was able to perform, what previously were performed by valve computers that occupied very large rooms created solely for this purpose. Obviously miniaturization was one of the key concepts of the industry. However the complete process from designing until the final product was produced was a long tedious process called the Semiconductor Value Chain.

Figure 2.1 depicts the Semiconductor Value Chain which in the early 1980's was vertically segregated. Big semiconductor IDM's (integrated device manufacturers) like Intel, AMD and Texas Instruments owned and operated their own manufacturing facilities (Fabs) and integrated the whole value chain within their organization.

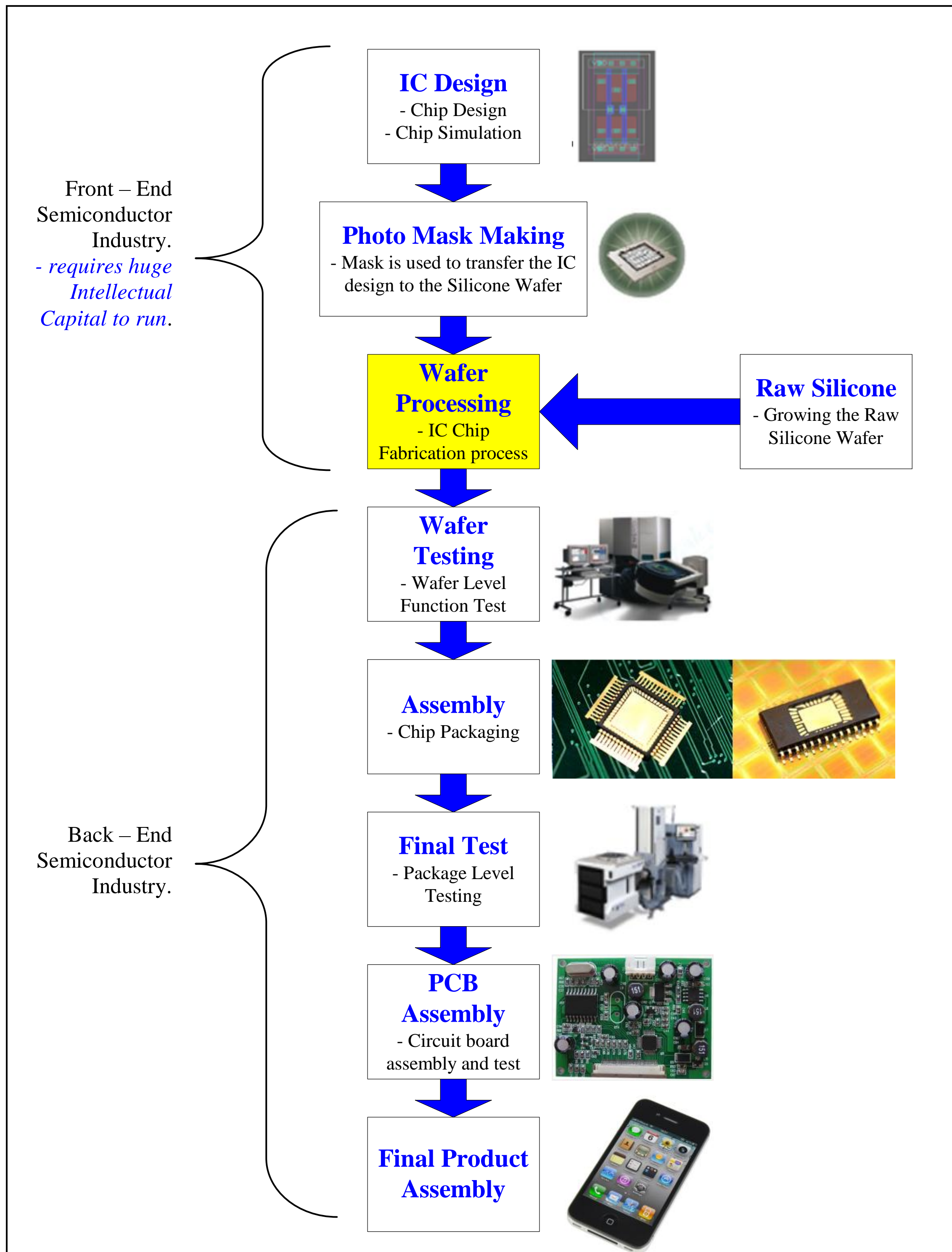


Figure 2.1: The Semiconductor Value Chain

In order to manage excess capacity and increase the ROI of the capital intensive semiconductor manufacturing process, IDMs started offering smaller firms design,

manufacturing, and packaging services. This was the start of the outsourcing revolution that we now call the Fabless Semiconductor Industry.

The first Wafer Foundry was founded by Dr. Morris Chang named Taiwan Semiconductor Manufacturing Company (TSMC). In 1987 TSMC started the foundry business 2 process nodes behind current semiconductor manufacturers (IDMs). 4-5 years later TSMC was only behind 1 node and the orders started pouring in. In 10 years TSMC caught up with IDMs and the fabless semiconductor industry blossomed enabling a whole new era of semiconductor design and manufacturing. In the last 25 years and still today the remaining IDMs are being forced to go fabless (outsourcing of the wafer manufacturing process to a wafer foundry) due to cost and daunting technical challenge . Figure 2.2 below shows the top 20 semiconductor sales leaders in the 2013 while comparing how much has their sales changed year on year compared to 2012.

2013 Top 20 Semiconductor Sales Leaders ($M, Including Foundries)

2013 Rank	2012 Rank	Company	Headquarters	2012 Tot IC	2012 Tot O-S-D	2012 Tot Semi	2013 Tot IC	2013 Tot O-S-D	2013 Tot Semi	2013/2012 % Change
1	1	Intel	U.S.	49,114	0	49,114	48,321	0	48,321	-2%
2	2	Samsung	South Korea	30,457	1,794	32,251	32,520	1,858	34,378	7%
3	3	TSMC*	Taiwan	16,951	0	16,951	19,850	0	19,850	17%
4	4	Qualcomm**	U.S.	13,177	0	13,177	17,211	0	17,211	31%
5	10	Micron***	U.S.	7,567	322	7,889	14,255	105	14,360	82%
6	8	SK Hynix	South Korea	9,057	0	9,057	12,970	0	12,970	43%
7	6	Toshiba	Japan	9,055	2,162	11,217	9,868	2,090	11,958	7%
8	5	TI	U.S.	11,376	705	12,081	10,794	680	11,474	-5%
9	11	Broadcom**	U.S.	7,793	0	7,793	8,219	0	8,219	5%
10	9	ST	Europe	6,227	2,137	8,364	5,847	2,167	8,014	-4%
11	7	Renesas	Japan	7,487	1,827	9,314	6,405	1,570	7,975	-14%
12	13	AMD**	U.S.	5,422	0	5,422	5,299	0	5,299	-2%
13	14	Infineon	Europe	3,078	1,850	4,928	3,402	1,858	5,260	7%
14	12	Sony	Japan	1,926	3,783	5,709	1,271	3,598	4,869	-15%
15	15	NXP	Europe	3,102	1,223	4,325	3,534	1,281	4,815	11%
16	22	MediaTek**	Taiwan	3,366	0	3,366	4,587	0	4,587	36%
17	17	GlobalFoundries*	U.S.	4,013	0	4,013	4,261	0	4,261	6%
18	19	Freescale	U.S.	3,180	571	3,751	3,371	636	4,007	7%
19	20	UMC*	Taiwan	3,730	0	3,730	3,959	0	3,959	6%
20	18	Nvidia**	U.S.	3,965	0	3,965	3,898	0	3,898	-2%
—	—	Top 20 Total		200,043	16,374	216,417	219,842	15,843	235,685	9%

*Foundry **Fabless ***Includes Elpida's entire 2013 sales of $2.5 billion.

Source: Company reports, IC Insights' *Strategic Reviews* database

Figure 2.2: 2013 Top 20 Semiconductor Sales Leaders

Figure 2.2 (Source: Company Reports, IC insights's Startegic Review Database) puts into persepctive the impact the wafer foundry business has on changing the landscape of the semiconductor industry as depicted in the semiconductor value chain. In this figure 2.2, 6 out of 20 market leaders are Fabless companies (indicated with **) which means they have outsourced their wafer manufacturing, while 3 out of 20 leaders are foundries (indicated with *). Even as late as 2005, this list was topped by mainly IDMs, who had the semiconductor value chain vertically integrated and created a barrier of entry for other smaller designers and innovators. But 2013 revenue data shows how many companies have achieved great revenues by going fabless for example Qualcomm and Micron that have shown huge percentage increase in revenue year on year in 2013 as compared to 2012.

Infact many of the processes in the Semiconductor Value Chain have now been outsourced by the fabless semiconductor firms to form a network of companies who specialize and focus on one particular area for enhanced performance, reduced cost and leveraged Return on Investment. This also allows new design firms and start-ups to compete in the Semiconductor Industry as entry cost barriers are significantly reduced.

This trend also has allowed the start-ups of many wafer foundries around the globe. Figure 2.3 shows the top 20 wafer foundries in the industry today based on 2012 sales revenue according to Company Reports 2012 from IC insights's Startegic Review Database. This table is crucial information that shows that there are as many as 20 high rollers in the wafer foundry business in which Silterra is competing and was in the 15th ranking in 2012 sales numbers.

Leading Pure-Play Foundry Companies

Rank	Company (Headquarters)	2012 Sales (US$ million)
1	TSMC (Taiwan)	17,167
2	GlobalFoundries (US)	4,560
3	UMC Group (Taiwan)1	3,730
4	SMIC (China) 2	1,682
5	Hua Hong Grace (China)3	940
6	Tower Jazz(Israel)	644
7	Vanguard (Taiwan)2	582
8	Dongbu HiTek (S. Korea)	540
9	WIN (Taiwan)4	382
10	SSMC (Singapore)2	370
11	X-Fab (Europe)	260
12	Altis (Europe)5	228
13	Telefunken (Europe)	220
14	He Jian (China)	215
15	Silterra (Malaysia)	213
16	ASMC (China)	149
17	LFoundry (Europe)	140
18	Mosel-Vitelic (Taiwan)	34
19	Hua Hong NEC (China)3	0
20	Shanghai Huali	0

Notes: 1 Includes UMC Japan sales 2 Partially owned by TSMC and includes Xinxin 3HHNEC & Grace merged in Q1 2012 (includes Shanghai Huali joint venture in 2012) 4 Uses GaAs processes 5 Former IBM/Infineon fab, sold in Q3 2010
Source: Insights, company reports

Figure 2.3: Ranking of Pure-Play Foundry Companies based on Sales Revenue for 2012. (Source: Insights, Company reports)

In order for Silterra to be profitable, it must at all time maximise the use of its limited capacity to get maximum returns and have to strive hard to keep their customers satisfied. With the current inability of the Etch module to perform, will impact both capacity utilization and customer satisfaction.

3.0 Company Background

3.1 Company Overview

Silterra is the brain child of the 4th Malaysian Prime Minister Tun Dr. Mahatir. It was a project of strategic national interest to promote front-end semiconductor manufacturing since most semiconductor businesses operating in Malaysia since the 1980 is from the back-end industry as shown in the Semiconductor Value Chain in Figure 2.1. It was also intended to be a catalyst for high technology investments in Malaysia. It was founded in November 1995 as Wafer Technology Malaysia Sdn Bhd and was renamed as Silterra Malaysia Sdn Bhd in December 1999.

During its start-up, Silterra had a strategic collaboration for its original technology and factory start-up prototype with a American IDM company called LSI Logic. LSI Logic had a wafer manufacturing facility in Gresham Oregon and the current Silterra Factory in Kulim is a copy exact of the LSI Logic Gresham facility.

Initial stakeholders during start up were 60% stakes by Khazanah National, 10% Stakes by LSI Logic (the technology partner), 20% stakes by Seiko (Korea) and another 10% was other local investors. Over time as the operating costs escalated, Khazanah was the only investor who continued pumping capital into the project and over the years had assumed 99% stakes in the company currently.

Silterra broke ground on its first manufacturing facility in Kulim, Malaysia in June 1999 and produced a working product in November 2000. Since its inception, Silterra has served many top-tier global Fabless design and product companies covering the consumer electronics, communications & computing, and mobile device

market.

Silterra offers CMOS design and a broad range of fabrication processes for Integrated Chips (IC) in Advanced Logic, Mixed Signal & Radio Frequency and High Voltage applications. The CMOS High Voltage Technology being used in the design and fabrication of Display Driver IC's (DDI), is widely used in the mobile devices market segment. This includes display drivers for mobile phones, GPS equipment, MP3/4 Personal Media Players (PMP), Digital Cameras and other similar applications.

Silterra provides complete design solutions for customers to create leading-edge products, optimized for its high-yielding manufacturing processes, through strategic partnerships with industry-leading Intellectual Property (IP) design library providers, Design Services and Electronic Design Automation (EDA) suppliers.

During start-up more then 250 Malaysian Engineers and 350 technicians were sent in batches to LSI Logic Gresham facility for training and technology transfer activities. The technology was compatible with the market leader TSMC Foundry specifications. By the year 2003, Silterra broke away from its technology partner, LSI Logic and started developing its own processes and technologies as the local team of experts were now capable of handling the business.

Silterra has more then 8 US Patents and many more filed for its proprietary technology development in the high voltage segment of integrated circuit

manufacturing. Silterra has also received the Semicon Top Fab Award and the Prime Minister's Hibiscus Award for a High Technology Company.

Currently the company has developed a network of highly qualified design service companies that provide comprehensive design services and design intellectual properties (Design IP) through strategic partnership. These design houses provide a range of services starting from initial design to layout and physical verification. Silterra Design Service Partners Network is as shown in figure 3.1

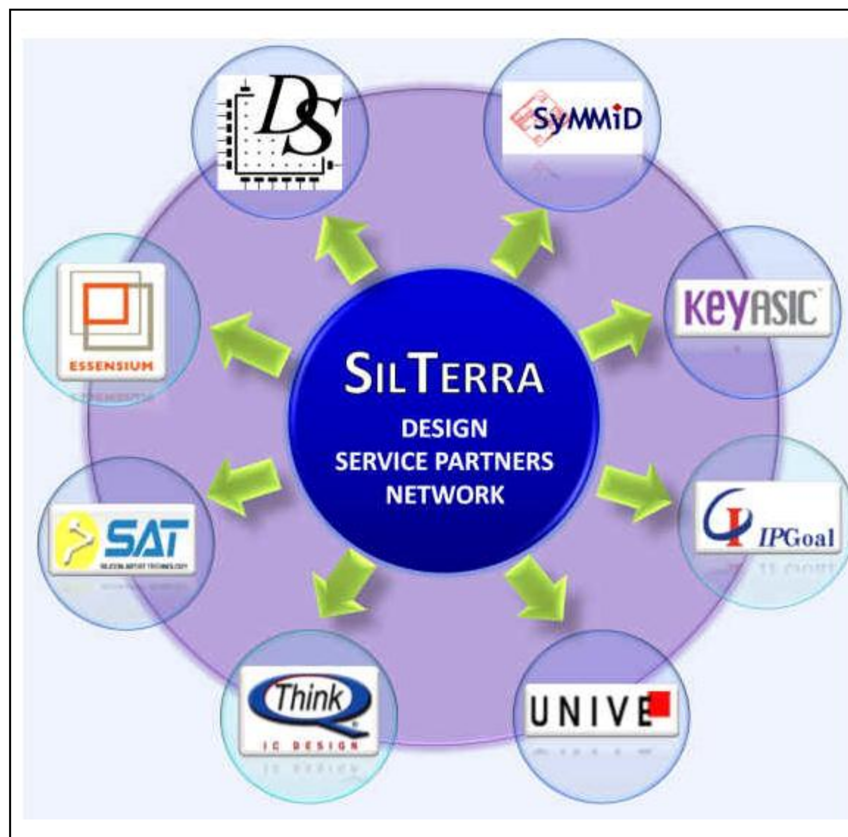


Figure 3.1: Silterra Design Service Partners Network.(Data Source: Silterra Website)

3.2 Company Vision

" Make Silterra the catalyst for expanding the Malaysian Semiconductor Industry by attracting the front-end industry players." By virtue of setting up Silterra, the fab support industry like tool vendors and service providers also setup their branches in

Malaysia. This attracted other wafer based companies like Infineon, Panasonic Solar and First Solar to also setup their factories in Kulim recently.

3.3 Company Mission

- Deliver world-class wafer manufacturing services to our customers which is matched to the current international standards set by market leaders.
- Provide our customers with excellent customer service and design IP support through our network of design service partners.
- Make Silterra a profitable enterprise that is continuously growing with innovation and knowledge and maximize the return on investment for our shareholders.

3.4 Company's Organization Structure

The principal investor of Silterra is Khazanah Nasional Berhad which is the investment holding arm of the Government of Malaysia entrusted to manage Government-held assets. One of its key corporate missions is to be a catalyst to develop strategic projects.

Khazanah selects the Board of Directors who in turn select the CEO. The CEO then appoints the key Vice-Presidents and Directors who manage the company. The Management Team Organization chart is as shown in Figure 3.4.1.

The current case is related to a Module within the Fab Operations team called the Etch Module. The Fab Operations team Organization Chart is as shown in Figure 3.4.2.

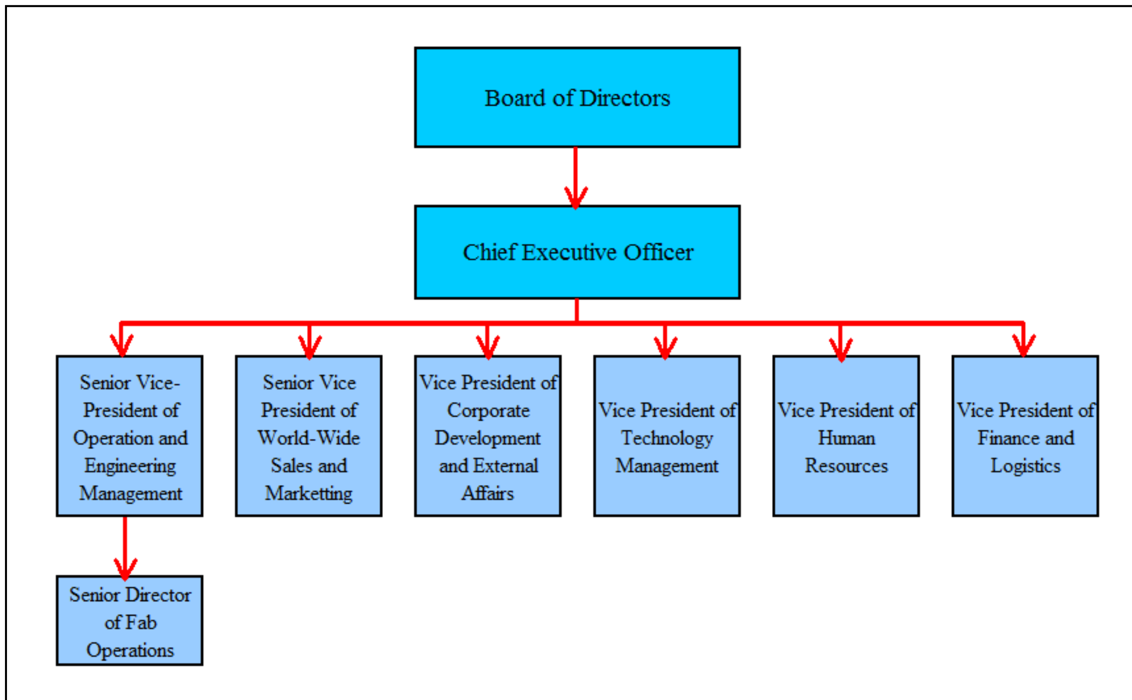


Figure 3.4.1: Silterra (M) Sdn. Bhd. Senior Management Organization Chart

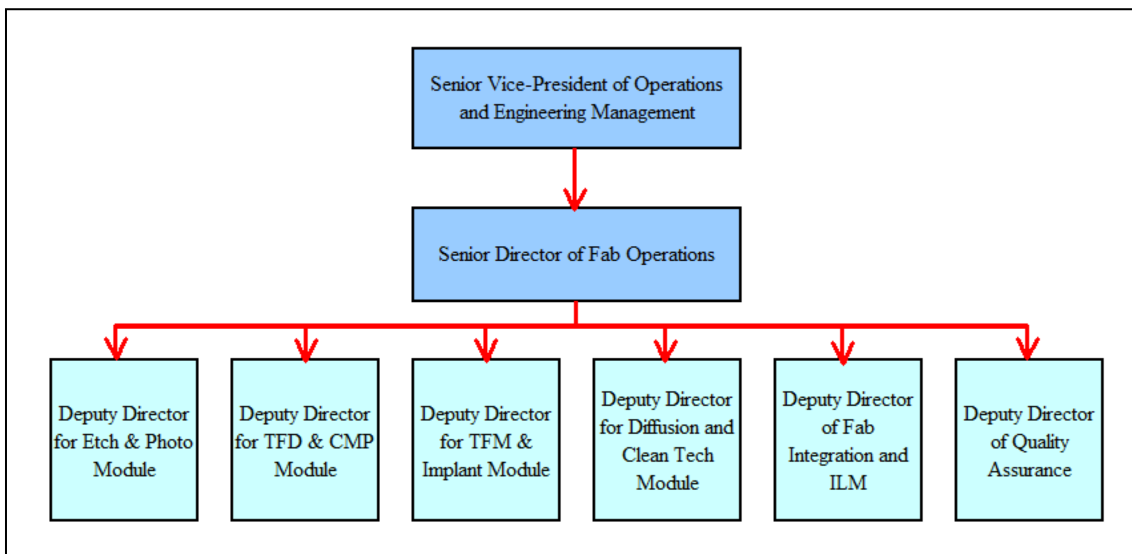


Figure 3.4.2: Fab Operations Management Teams Organization Chart

Mr.K is the Deputy Director for Etch and Photo Module in the above Fab Operations Organization Chart. We will look into how these 8 departments function in a wafer fabrication next before going into the etch department in detail.

3.5 Description of the Wafer Fabrication Process

As technology leads the way to innovative life style, almost all daily activities uses some form of an electronic device for automation. These devices operate with a little brain inside it called an Application Specific Integrated Circuit (ASIC). These ASIC are made using a Silicone Wafer. The process is called "Wafer Fabrication" and hence why the factory where this process happens is called a Wafer Fab. In Silterra the chips are fabricated on a 8 inch wafer. A single wafer can contain as many as 10000 chips based on the chip size. Figure 3.5.1 is pictorial representation of how ASIC chips are made.

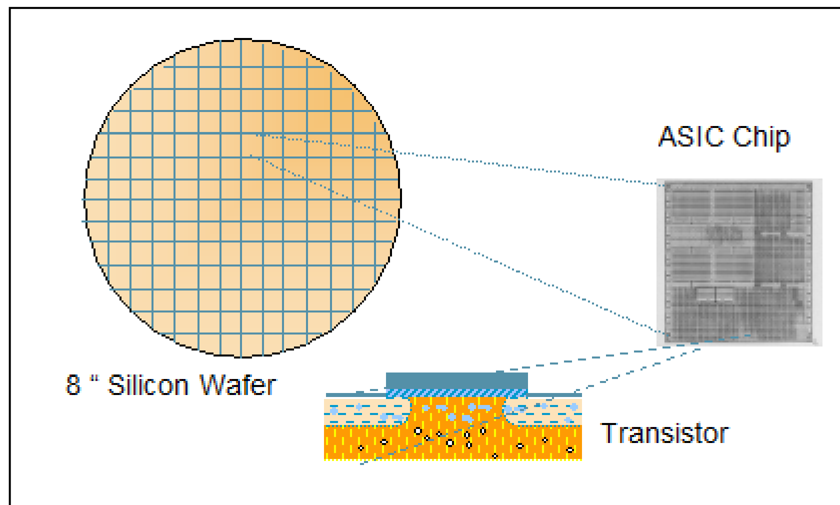


Figure 3.5.1: A zoom in on ASIC wafer construction.
(Data Source: Silterra Internal Training Material for Overview of Semiconductor Processing)

The actual component behind these brains is the Transistor. In the wafer fabrication process, millions of these transistor are built on the wafer itself. This process of building requires multiple types of materials being deposited onto the wafer and then patterning the desired shapes and then removal of the unwanted material. This process is achieved using a looped set of processes as pictured in figure 3.5.2.

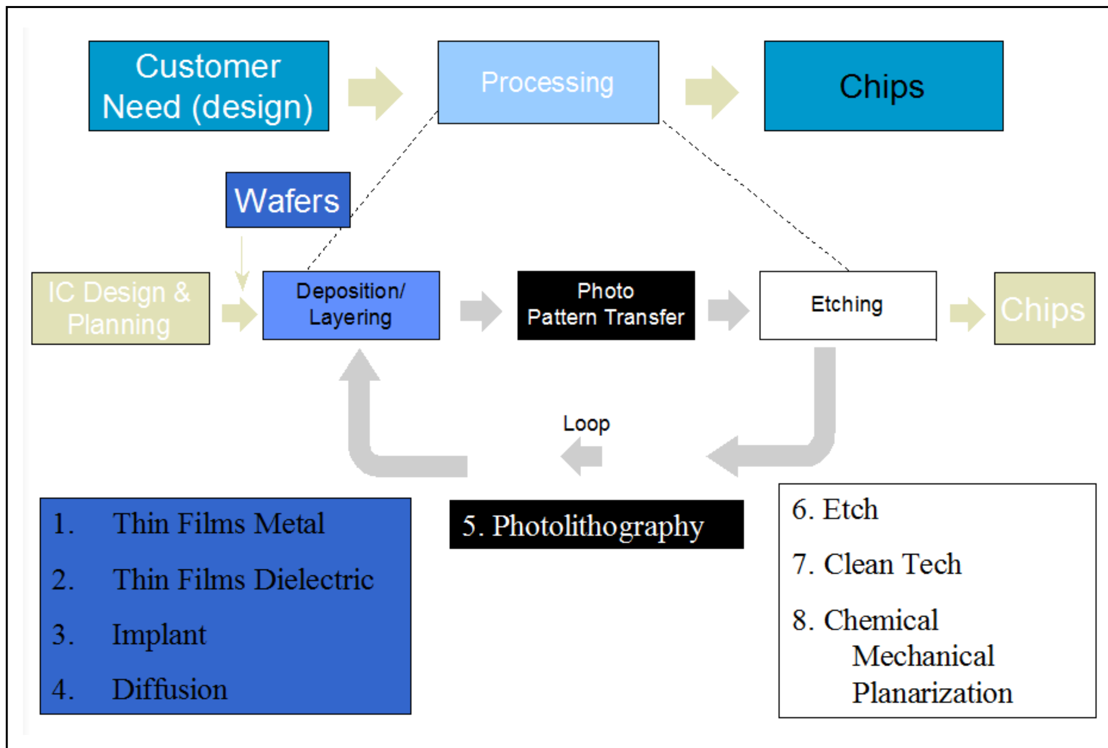


Figure 3.5.2: Wafer Fabrication Process Loop and the Departments involved
(Data Source: Silterra Internal Training Material for Overview of Semiconductor Processing)

Based on Figure 3.5.2 it can be summarized that the wafer fabrication process has 3 critical activities, namely the deposition or layering activity, the patterning activity and the removal of unwanted materials (etching) activity. It is crucial to understand how the 8 operation department interact with each other in this loop.

There are 4 departments involved in the deposition and layering activities. Thin Films Metal is in charge of depositing conductor materials on the wafer like Tungsten, Copper, Aluminium and Titanium. Thin Films Dielectric is in charge of depositing insulators materials on the wafer like Oxide and Nitride. Implant department is in charge of ion implantation on the wafer to make the semiconductor regions using Boron and Phosphorus as the implant elements. Finally diffusion layer is in charge of growing layers on the silicon wafer like native oxide and nitride.

The only department in the pattern transferring activity is the Photo department. This is the process of printing the customers Integrated Chip design onto the wafer before it is sent for selective removal of unwanted material.

The final activity in this loop is the removal of unwanted material and Etch Department is the main player in this activity. In Silterra all the etch activities is done using dry plasma etch to physically pattern the deposited material. The Clean Tech department is in charge of cleaning the wafers after the etching process. The Chemical Mechanical Planarization department is in charge of polishing the wafers to maintain a flat surface as we build more and more layers on the wafer.

At the end a circuit would have been constructed on the Silicone Wafer just like constructing a building. Figure 3.5.3 is a scanning electron microscope picture that shows how this "building" looks like in real life after completing at least 30 loops.

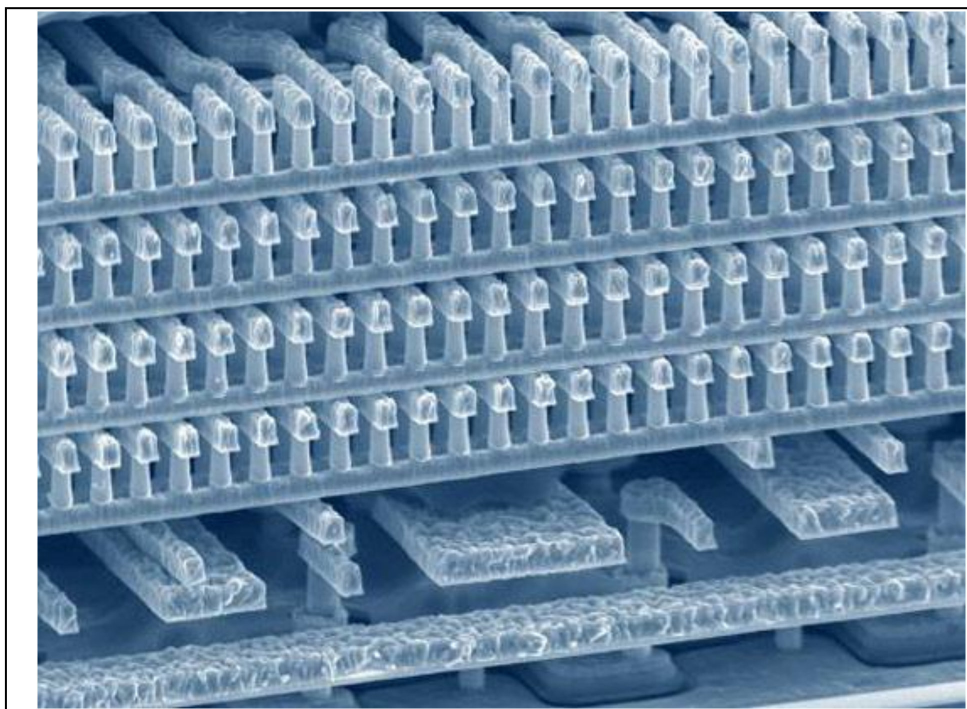


Figure 3.5.3: Scanning Electron Microscope Picture of a completed ASIC Chip
(Data Source: Silterra Internal Training Material for Overview of Semiconductor Processing)

Since the process of manufacturing a ASIC chip is looped at least 30 times and involves about 400 steps, it is apparent that any delay in one section or department will cascade to the loop and result in an overall delay of the manufacturing process. This is the main reason why the Etch Equipment Uptime for the third quarter had impacted the overall factories performance tremendously.

3.6 Description of the department and the persons involved

The Etch Module's Organization charts is shown Figure 3.6.1 .Mr.K is the Deputy Director who leads this whole module.

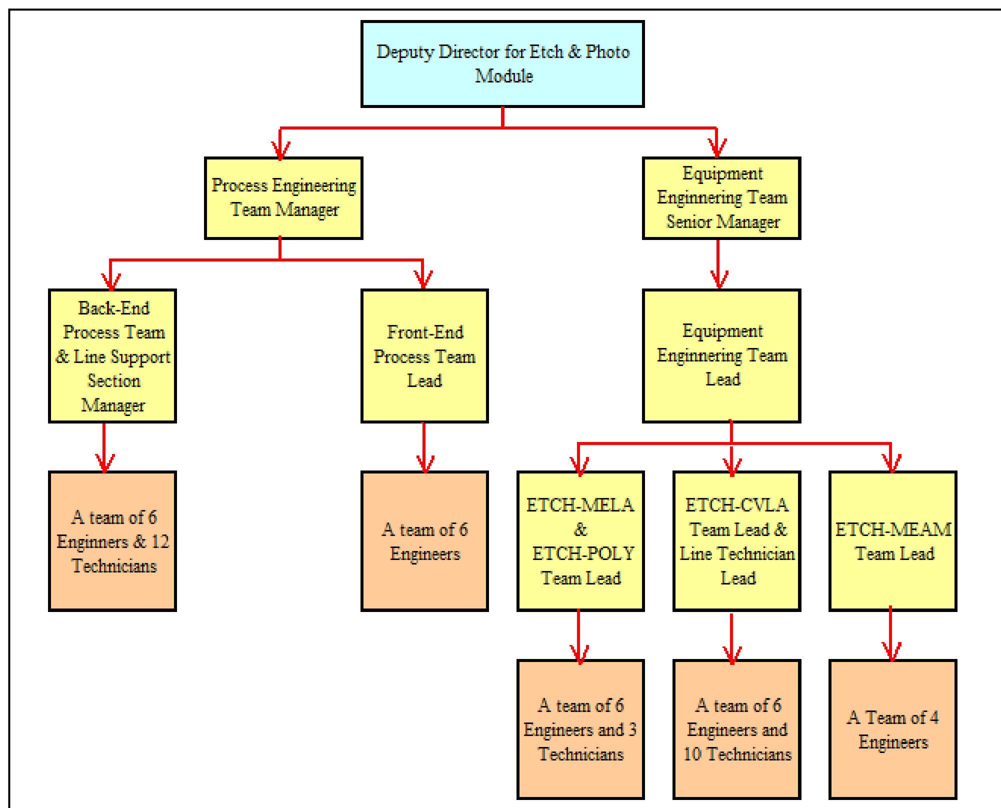


Figure 3.6.1: Etch Department Organization Chart

In this organization, after Mr.K, the team splits into two main categories namely the process and the equipment teams. The process team is in charge of developing the process and chemistry that runs on the equipments to produce the wafers. The process team also plays a complementary role to the equipment team by monitoring

the quality of the wafers produced from each tool and providing early warning if they see any potential issues based on Statistical Process Control. The process team is also the contact point to the internal and external customers for Etch. However the process team cannot function effectively if the tools used to run their process in unstable.

The second group which is of primary concern in this discussion is the Equipment team. The Equipment team is in charge of maintaining and troubleshooting the equipments in Etch module. They are also tasked to perform periodic preventive maintenance activities and monitor the tool's periodic qualification measurements to ensure the tool is in a production worthy state.

The senior manager of this Equipment Team has 18 years of experience in the Etch module and has worked in the front line as an equipment engineer at the beginning of his career. Hence he is well aware of how the tools work and is able to provide sound advice, guidance, leadership and suggestions to his team.

Next in line is the Equipment engineering team lead who has newly joined the department 12 months ago. He was originally from the process group and was assigned this role during the reorganization by Mr.K in July. He has no experience with the equipments but is tasked with handling the communication, reporting and managing the manpower for the equipment team. He is a single contact point for any updates or decision on tool activities daily.