ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT DESIGN IN DEEP SUB-MICRON TECHNOLOGY FOR AUTOMOTIVE APPLICATION

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ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT DESIGN IN DEEP SUB-MICRON TECHNOLOGY FOR AUTOMOTIVE APPLICATION

By

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TABLE OF CONTENTS

		Page
ACKNOWLEDGEMENT		ii
TABLE OF CONTENTS		iii
LIST OF TABLES		vi
LIST OF FIGURES		vii
LIST OF ABBREVIATIONS		x
ABSTRAK		xi
ABSTRACT		xii

CHAPTER ONE: INTRODUCTION

1.1	Overview	1
1.2	Problem Statement	4
1.3	Research Objectives	6
1.4	Research Scopes	6
1.5	Thesis Outline	7

CHAPTER TWO: LITERATURE REVIEW

2.1	Introduction		9
2.2	ESD Zapping		9
2.3	ESD Test Methods		11
	2.3.1	Human Body Model (HBM) ESD Test	11
	2.3.2	Machine Model (MM) ESD Test	12
	2.3.3	Charged Device Model (CDM) ESD Test	13
2.4	Transmission Line Pulse (TLP) ESD Testing		15
2.5	ESD Device for I/O Protection		17
	2.5.1	Non-Snapback Device	18

2.5.2 Snapback Device 19

2.6 ESD Protection Methodology 21

2.7 ESD Protection Techniques 26

2.7.1 Gate Coupling 26

2.7.2 Substrate Triggering 27

2.7.3 Silicide Blocking 28

2.8 Influence of Design, Layout and Processing on ESD Performance 29

2.8.1 Gate Length Dependence 29

2.8.2 Ballasting Structure Dependence/ESD Cell Design Principles/Influence of Processing on ESD 33

2.9 Summary 36

CHAPTER THREE: ESD RESEARCH METHODOLOGY

3.1 Overview 38

3.2 ESD Protection Selection Methodology and Criteria 39

3.3 Gate Length Dependency 41

3.4 Ballasting Design Methods 42

3.4.1 Back-End-Ballast (BEB) Design 43

3.4.2 Resist Protection Oxide (RPO) Design 45

3.5 Proposed ESD Power Clamp 47

3.6 ESD Measurement 52

3.7 Summary 55

CHAPTER FOUR: RESULTS & DISCUSSION

4.1 Overview 56

4.2 Experiment Setup 56

4.3 Experiments Result and Discussions 57

4.3.1 Gate Length Driven Effect 57
4.3.2 Improved Ballasting Layout Schemes 61
4.3.3 New ESD Power Clamp Implementation 64
4.4 Summary 66

CHAPTER FIVE: CONCLUSION

5.1 Conclusion 67
5.2 Future Work 68

REFERENCES 70

LIST OF TABLES

		Page
Table 2.1	Literature review of ESD protection techniques	40
Table 3.1	Different gate length variant to evaluate the effect of ESD	45
Table 3.2	ESD zapping level with ramp up voltage	60
Table 4.1	ESD protection gate length characterization	61
Table 4.2	The effect of ballast resistor toward high-speed LVDS driver	67
Table 4.3	Comparison of proposed transient clamp and conventional static clamp	72

LIST OF FIGURES

		Page
Figure 1.1	A common source of ESD phenomena	2
Figure 1.2	Images of various types of ESD failures: (a) junction breakdown, (b) gate-oxide breakdown and (c) metal damage	2
Figure 1.3	Narrower ESD design window due to technology shrinkage	5
Figure 2.1	Zapping conditions (a) PS-mode (b) NS-mode (c) PD-mode (d) ND-mode	10
Figure 2.2	Human body model corresponding circuit	12
Figure 2.3	Rise/decay time for human body model of ESD test	12
Figure 2.4	Machine model ESD setup (left) generates the waveform (right)	13
Figure 2.5	Charge device model corresponding circuit	14
Figure 2.6	Comparison between HBM, MM and CDM ESD test	15
Figure 2.7	Fundamental TLP system	16
Figure 2.8	Example of TLP device characteristics	17
Figure 2.9	Simple forward bias p-n junction diode (a) schematic (b) I-V curve	18
Figure 2.10	GGNMOS (a) basic structure (b) I-V curve	19
Figure 2.11	SCR (a) Cross-section (b) Basic schematic	21
Figure 2.12	Typical schematic of pad-based protection	22
Figure 2.13	(a) NMOS transistor along with the p-type substrate; (b) equivalent circuit of n-type source and drain	23
Figure 2.14	Electrons generated by the avalanche process flow into the drain	23
Figure 2.15	Curvature effect of electric field in drain junction	24
Figure 2.16	TLP characteristic of grounded gate NMOS (GGNMOS) transistor	25
Figure 2.17	One finger snapback and carrier spread to other fingers	26
Figure 2.18	Single finger turns on where the power is localized	26

Figure 2.19	Trigger voltage V_{t1} reduced below V_{t2} by applying a small positive gate bias	27
Figure 2.20	Cross section of a fully silicided GGNMOS test structure	29
Figure 2.21	I_{t2} as a function of gate length for five different transistors in three different process nodes	31
Figure 2.22	Transistor parameters effect based on gate length, *L* for NMOS transistor in 0.18 um technology. (a) I_{t2} as a function of gate length (b) *M* and β as a function of gate length (c) *Rsub* as function of gate length	32
Figure 2.23	I_{t2} versus gate length analysis for different diameters, D on NMOS and PMOS devices	33
Figure 2.24	Cross-section of an NMOS transistor associated with the parasitic lateral NPN device	34
Figure 2.25	Back-End Ballasting (BEB) layout	36
Figure 2.26	Current defocusing due to segmentation	36
Figure 3.1	Research flow chart	40
Figure 3.2	Cross-section and layout sketch of the ESD NMOS structure	42
Figure 3.3	Snapback IV curve for uniform ESD current conduction	44
Figure 3.4	Layout illustration of ESD BEB structure	44
Figure 3.5	Illustration of layout of RPO ESD structure	46
Figure 3.6	The new RPO ESD schematic	47
Figure 3.7	The ESD current discharge path during pin-to-pin ESD event	48
Figure 3.8	ESD clamp schematic	49
Figure 3.9	The new ESD power clamp schematic	50
Figure 3.10	The new ESD power clamp layout	51
Figure 3.11	TLP testing methodology	52
Figure 3.12	Example of TLP measurement results	53
Figure 3.13	Various test conditions for HBM and MM ESD	54
Figure 4.1	ESD test setup	57
Figure 4.2	Two-probes ESD wafer level testing	57
Figure 4.3	TLP result for different gate lengths structures	59

Figure 4.4 HBM ESD performance for different gate lengths structures 60

Figure 4.5 I_{t2} performance for different gate lengths structures 60

Figure 4.6 SEM image (a) top-view (b) zoom-in of BEB ballast after 25V ESD stress 63

LIST OF ABBREVIATIONS

Abbreviation	Meaning
BEB	Back-End Ballast
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DCP	Drain Contact to Poly
DUT	Device Under Test
ESD	Electrostatic Discharge
ESDA	Electrostatic Discharge Association
GGNMOS	Grounded Gate N-MOS
HBM	Human Body Model
IC	Integrated Circuit
JEDEC	Joint Electronics Device Engineering Council
JEITA	Information Technology Industries Association
LDD	Lightly Doped Drain
LVDS	Low-Voltage Differential Signaling
MFT	Multi-Finger-Transistor
MM	Machine Model
OD	Oxide Diffusion
PLL	Phase-Locked Loop
RPO	Resist Protection Oxide
SCP	Source Contact to Poly
SCR	Silicon Controlled Rectifier
TLP	Transmission Line Pulse

REKA BENTUK LITAR PERLINDUNGAN NYAHCAS ELEKTROSTATIK DALAM SUBMIKRON DALAM UNTUK APLIKASI AUTOMOTIF

ABSTRAK

Kebanyakan produk semikonduktor moden mudah terdedah kepada kerosakan nyahcas elektrostatik (ESD) dan ini menjadikan perlindungan ESD salah satu keperluan utama bagi litar bersepadu (IC). Walau bagaimanapun, spesifikasi ESD ketika ini menyebabkan kecerutan untuk mencapai tahap ESD yang lebih ketat terutamanya untuk segmen industri automotif berbanding dengan aplikasi lain. Aktiviti penskalaan agresif teknologi semikonduktor oksida logam gabungan (CMOS) terhadap rejim nanometer menjadikan IC mudah terdedah kepada kegagalan ESD dan pelaksanaan rangkaian perlindungan ESD akan menjadi lebih mencabar. Kajian ini bertujuan untuk membangunkan penyelesaian perlindungan ESD yang berkesan melalui metodologi reka-bentuk bersama prestasi litar. Dua kes ujian sebenar penambahbaikan ESD telah dikaji secara terperinci. Kajian ini menunjukkan bahawa isu LVDS ESD berkelajuan tinggi boleh diselesaikan dengan mengoptimumkan kedua-dua pemandu LVDS berkelajuan tinggi dan reka bentuk MOS ESD. Selain itu, kajian ini juga menunjukkan bahawa kekukuhan ESD yang rapuh dalam domain kuasa kecil boleh dipertingkatkan dengan memperkenalkan pengapit ESD novel. Pelaksanaan penambahbaikan ESD ini berjaya memenuhi kedua-dua spesifikasi ESD automotif yang ketat iaitu sebanyak 2000V bagi model badan manusia (HBM) dan 200V bagi model mesin (MM) dan membolehkan pengecilan CMOS yang berterusan.

ELECTROSTATIC DISCHARGE PROTECTION CIRCUIT DESIGN IN DEEP SUB-MICRON TECHNOLOGY FOR AUTOMOTIVE APPLICATION

ABSTRACT

Many modern semiconductor products are susceptible to the damage of electrostatic discharge (ESD) and this make ESD protection a must for integrated circuits. However, current ESD specifications cause a bottleneck for ESD qualifications especially for the automotive industry segment, which requires more stringent qualification requirements than other applications. The advancement of complementary metal-oxide-semiconductor (CMOS) transistors scaling into the nano-metric regime makes ICs more vulnerable to ESD failures and the implementation of an effective ESD protection designs become very difficult. This research aims to develop a robust ESD protection solution through circuit performance co-design methodologies. Two real test cases of ESD improvements have been studied in detail. This research has shown that the low voltage differential signaling (LVDS) ESD issue can be resolved by optimizing both the high-speed driver gate length and the ESD MOS design. In addition, it is also demonstrated that the fragile ESD robustness in small power domain can be enhanced by introducing a novel ESD clamp. By implementing these ESD improvements, the automotive ESD stringent requirements for both the 2000V human body model (HBM) and the 200V machine model (MM) could be met and enabled the continuation of CMOS scaling.

CHAPTER ONE

INTRODUCTION

1.1 Overview

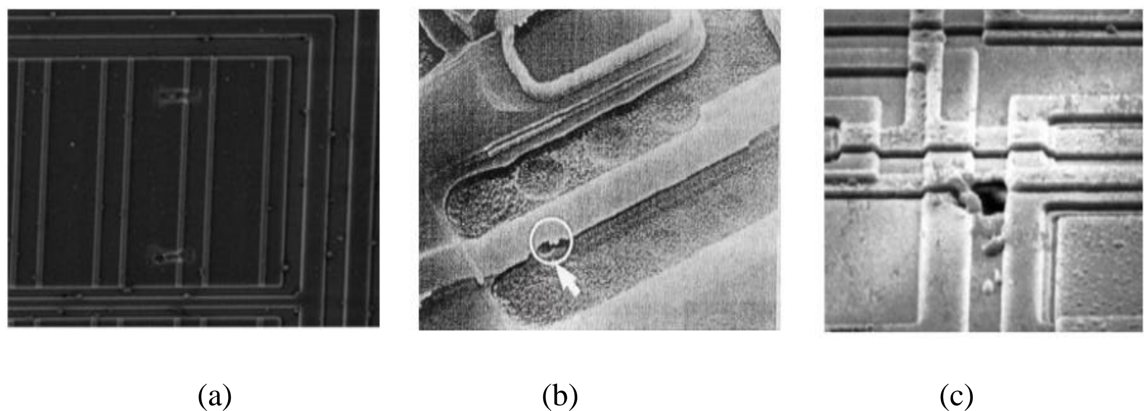
Electrostatic Discharge (ESD) is a very common phenomenon that happen naturally even in controlled environments. When two objects come into contact and then separate, a static charge is developed by friction as indicated in Figure 1.1. The fundamental cause of ESD shock is the car-door spark when touching the door knob, or walking on a carpeted floor [1]. This process causes a pain felt by human due to the static charge build up on their body for an extremely short period of time. An ESD event is defined as a rapid current surge between two surfaces of objects with different electrostatic potentials. When these two objects with different electrical potentials are rubbed and then separated, a static charge is generated. It is projected that approximately 35% of all damage to microchips are related to ESD which results in revenue losses of several hundreds of million dollars annually [2].

There are several factors that can induce the electrical charge, for example the triboelectric charging effect, electrostatic induction, bombarding ions or contact with other electrically charged object. Among all these phenomenon, triboelectric charging is the most usual mechanism occurring in ICs. The mechanism of electrostatic charge creation by the frictional contact and separation of two objects is classified as triboelectric charging [1]. ESD events can occur anytime without any notice throughout the entire product life cycle. The damaging of electronic device due to ESD could be possibly caused by the human body, equipment, assembly or maintenance during their product lifetime. This raises a serious concern to electronic devices and affects the operation of the electronic systems.

The cause of ESD damage driven by static potential on the charged surfaces exposed to ESD event is detectable when the energy is dissipated.

Figure 1.1: A common source of ESD phenomena

Different ESD failure can be modeled and it requires different types of protection and control. Basic failure mechanisms include gate-oxide breakdown or metal-interconnect burnout. Figure 1.2 shows typical ESD damages. The total amount of electrostatic charge accumulated on electronic devices can easily exceed several kilovolts. This high voltage will create a very high electric field and current in ICs that simply ruptures thin gate-oxide in electronic devices. The main outcome from an ESD event is the generation of tremendous heat in a localized area quicker than the heat to be able to dissipate, which results in a temperature increase in surplus of the safe functional range.



(a) (b) (c)

Figure 1.2: Images of various types of ESD failures: (a) junction breakdown, (b) gate-oxide breakdown and (c) metal damage

It is increasingly difficult to meet ESD challenges in the electronics industry because of the current trend to move towards higher speed and smaller device sizes. A major challenge in developing a robust ESD protection scheme is the necessity of occupying a small footprint or using existing device availability, and extra processing steps or introduction of new masks are not recommended due to cost constraints. For over two decades, IC component-level ESD targets for both the Human Body Model (HBM) at 2000V and the Machine Model (MM) at 200V have essentially remained unchanged. However, the MM test standard is rapidly being discontinued across the industry because it is considered redundant to the HBM and does not create relevant ESD failures that differ from the HBM and the Charged Device Model (CDM).

In addition, it was shown that MM testing consumes more resources and create time-to-market delays while only providing failure modes that HBM and CDM have already covered [3]. Although MM was downgraded or eliminated by major ESD standards authority such as the Joint Electronics Device Engineering Council (JEDEC), Electrostatic Discharge Association (ESDA) and the Japan Electronics and Information Technology Industries Association (JEITA), it is still widely used amongst Japanese manufacturers, especially in the automotive field, mostly as a legacy requirement.

Current ESD specifications cause a bottleneck for ESD qualifications while making it very challenging to uphold the essential device high-speed performance [4]. The advancement of complementary metal-oxide-semiconductor (CMOS) transistors scaling into the nano-metric regime makes ICs vulnerable to ESD failures and the implementation of ESD protection circuits become more challenging. ESD-induced failures becomes one of the major reliability issues for advanced technologies and impacts revenue due to field returned ICs.

Typically, the gate oxide failure is directly proportional to the reduce of gate-oxide thickness [5]. The high electric field could cause irreversible gate-oxide rupture. Because of device scaling, a thinner gate-oxide and narrower junction depth are adopted which results in significant increase of gate-oxide damage because of ESD events in advanced technologies. The introduction of silicidation process in advanced technologies further reduces the ESD robustness due to the reduction of ballast resistance capability provided by the drain contact spacing to the gate poly edge.

Interconnect scaling and the migration to Cu-based routing are more prone to ESD induced “fuses” effect happening in all metal layers and this will lead to functional failure of IC devices. The high current contributed by the ESD event will impact electrical failures in narrow linewidths and eventually cause interconnect failures. Both interconnect scaling and reduction in metal width affects the ESD robustness in an advanced CMOS technology generation process.

1.2 Problem Statement

ESD test requirements have essentially stayed relatively unchanged for the past 20 years. The automotive ESD protection level requirement of the HBM tests of 2kV and the MM test of 200V were easily met by IC manufacturers. However, starting from the 90nm process technology, ESD reliability qualification encountered significant bottlenecks. The ESD failure become more notable because of the persistence of the CMOS technology scaling. It is also predicted that the availability of a highly effective ESD protection circuit could potentially lead to the advancement of the next-generation technologies [6].

The impact on the ESD protection design window when moving towards advance technologies is depicted in Figure 1.3. This window is controlled by the ESD current at vertical axis versus the oxide breakdown voltage at lateral axis. The graph in this

framework represents the correlation between ESD current and oxide breakdown voltage with respect to the HBM failure. A shrinkage of the breakdown voltage transistor is surpassed by the dropping of V_{DD} core supply and eventually cause the adverse effect on the ESD design window [7]. It was increasingly challenging to constantly meet the expected automotive ESD requirements at 2kV and 200V levels. It is much more difficult to preserve high speed performance while trying to accomplish these stringent ESD requirements [4].

The ESD sensitivity is getting worse with thinner gate-oxide and thinner metal interconnect needed for device speed performance improvements. ESD damage occurs when the dielectric breaks down due to the high electric fields. When ESD event occur, the gate-oxide ruptures or in advanced technologies, soft gate-oxide breakdown could cause degradation on device reliability.

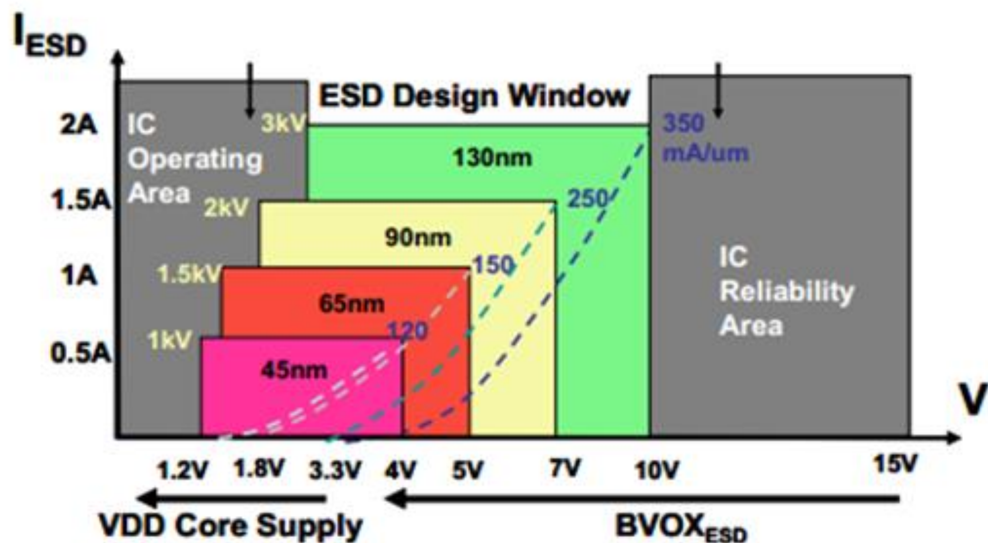


Figure 1.3: Narrower ESD design window due to technology shrinkage [3]

The key area to address ESD protection design challenges are driven by the following factors: warrant appropriate energy equilibrium inside the device, appropriate current level to achieve equilibrium on the clamp, appropriate total current level, and

effectively produce a suitable triggering and holding voltages appropriate to the voltage limit for the pin being protected [8].

ESD protection schemes are becoming more expensive and challenging to develop. The cost of implementing robust ESD solution is inversely proportional to the transistor channel length as the technology node continue to shrink (for example 130 nm to 45 nm). However, there is an opportunity to improve ESD robustness to allow the progressive reduction of CMOS transistor size. This is the area of investigation, particularly in high-speed low-voltage differential signaling via design co-optimization methodologies.

1.3 Research Objectives

The aim of the research is:

(i) To investigate the implications of various ESD protection designs to maximize ESD current handling capability using multiple test vehicles in 55 nm CMOS process and tested with ESD zapping, as well as transmission line pulse (TLP) measurement method.

(ii) To address ESD protection design challenges for advanced technologies by improving ESD strength through circuit level co-design methodologies to fulfil more stringent ESD requirement in the automotive industry.

1.4 Research Scopes

Designing the ESD protection scheme around the desired MM and HBM target levels may be challenging as devices become smaller and faster with technology node advancement. Implementing a robust ESD protection device requires an effective ESD design approach in order to fulfil stringent ESD requirements particularly for automotive applications. This research focuses on ESD design schemes, characterization results, failure analyses and ESD device/circuit design fix solutions for 55 nm CMOS process.

All ESD tests will be carried out using JEDEC (Joint Electronics Device Engineering Council) testing methodology for ESD, MM, HBM and CDM and data will be collected across multiple test vehicles. The overall ESD test plan is a two-step process consisting of failing voltage identification and followed by failure isolation. The failures will be confirmed by way of the curve trace method and in-house functional testing. The failure samples will undergo failure mode characterization by way of backside infrared emission followed by silicon layer de-process methods.

1.5 Thesis Outline

This chapter highlights the scaling effects and ESD protection design challenges. The ESD protection design window is illustrated for ESD protection schemes.

Chapter 2 delivers the literature review to serve for theoretical study. This chapter starts with a general overview of the characterization of the ESD phenomena as a preliminary information to provide a context of this research. In addition, the ESD failure modes and the types of testing are discussed. In addition, ESD protection techniques in previous research are also provided.

Chapter 3 focuses on the design and implementation of the proposed ESD protection design methodology. A well-defined workflow is established to guide the process of ESD protection strategy for different applications.

Chapter 4 presents all the results obtained. Based on the real test cases result, a proposed design approach from MM/HBM target classification to design optimization, discharge path analysis, and finally ESD and performance characterization are streamlined. It is shown that the localized heating by current crowding effects driven by non-uniform

lateral bipolar conduction has significantly degrades ESD performances. Improvement in performance is realized by adopting the proposed methodology.

Finally, chapter 5 recaps the key aspects and important elements, as well as the research contributions. The limitation and future research directions for ESD protection design research is also been discussed.

CHAPTER TWO

LITERATURE REVIEW

2.1 Introduction

ESD event is being recognized as the significant contributor causing a range of harmful effects of electronic devices. The ESD stress carries amperes of electric current from hundreds of picoseconds to hundreds of nanoseconds in a very short period of time [9]. Such events damage electronic component, ICs, production yield, manufacturing cost and product quality. ESD still costs the electronics industry billions of dollars every year. Therefore, thousands of semiconductors companies are paying more attention to the industry accepted elements of ESD static control.

The ESD requirements are very demanding for the automotive industry segment. Safety plays a very dominant role in car developments, followed by a low return rate requirement and a long life-span without reliability failure. Therefore, a stringent safety requirement exists to cater for the ESD threats in the automotive industry. This makes ESD protection design engineering a challenging task that could potentially delay the roadmap of automotive technologies [10]. To qualify the ESD immunity of IC products, there are various test methods and standards (so-called ESD zapping test) developed by various organizations, which will be discussed in section 2.2.

2.2 ESD Zapping

The input/output pin will need to be stressed with ESD zapping in both the positive polarity and negative polarity with reference to the power supply V_{DD} pin and ground. In general, ESD events can be categorized into four separate zapping conditions [11]. These categories are referred as PS-mode, NS-mode, PD-mode and ND-mode as shown in Figure 2.1. During ESD stress, a positive voltage is applied to the test pin in PS-mode with the

V_{SS} pin grounded and the remaining V_{DD} and input/output pins unconnected. In the case of NS-mode, the negative voltage polarity is applied, while the rest of the condition is identical to PS-mode. Similarly, PD (ND) mode describes the categories where a positive (negative) voltage is applied to a pin with V_{DD} grounded and remaining V_{SS} and input/output pins unconnected. The stress voltages describe above have proven to damage sensitive circuity apart from input/output devices and the ESD protection circuit.

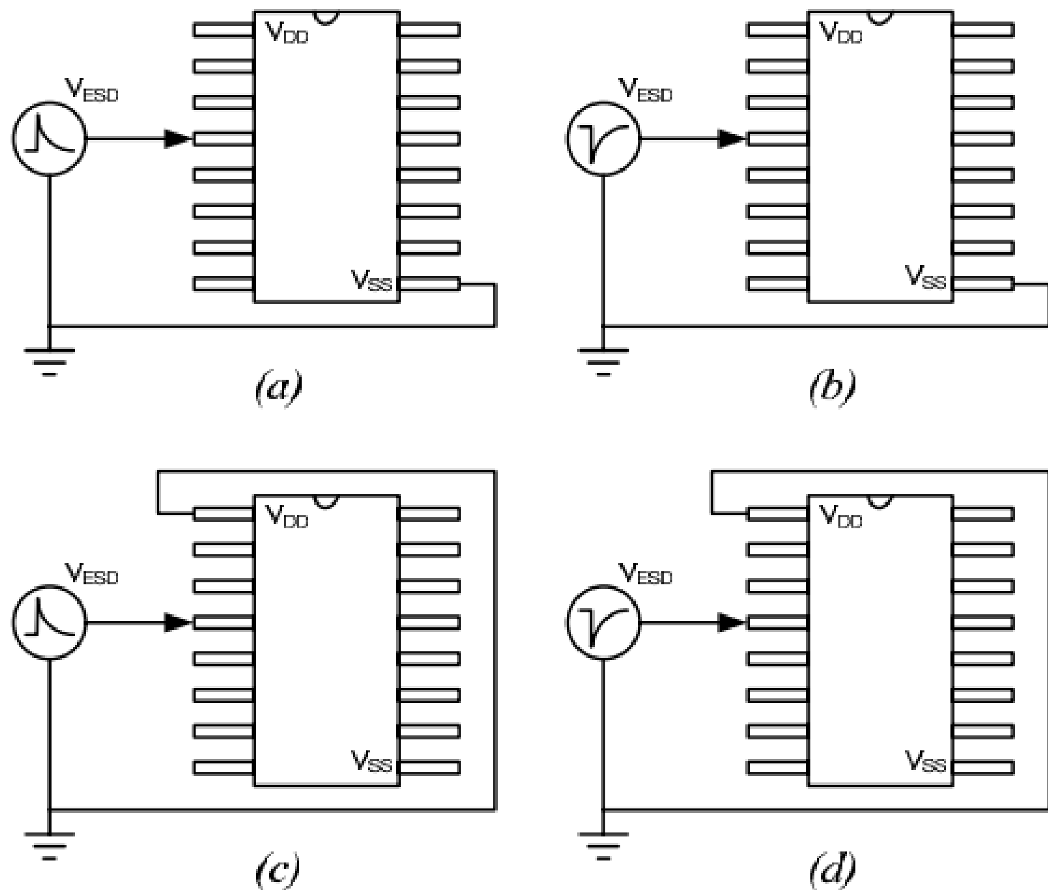


Figure 2.1: Zapping conditions (a) PS-mode (b) NS-mode (c) PD-mode (d) ND-mode

Among these four zapping conditions, the lowest (in absolute value) of ESD-sustaining voltage is considered as the ESD failure threshold level. For example, the ESD failure threshold is clearly defined as 1kV if ND mode ESD stress can only withstand 1kV ESD voltage although the remaining three ESD stresses (PS, NS and PD modes) exceeded 3kV ESD voltage.

2.3 ESD Test Methods

ESD test is a destructive test and the performance of a tested device is non-recoverable upon testing. The ESD test replicates various form of damages and quantifies the effects contributed by the different types of ESD stress subjected in an IC device. ESD test specifies the waveforms of discharge current for a given pre-charge voltage and generate different voltage and heat up the device structure tested. Basically, the real world of common standard ESD test methods is segregated into three separate categories when the IC devices come into testing. They are human body model (HBM) that simulate the discharge when human touch an electronic device, machine model (MM) that simulates the ESD discharge coming from a charged machine/tools to a grounded IC and lastly is charge device model (CDM) which represents an ESD event when a part of the electronic circuit accumulates electrical charge while it is assembled comes into contact with grounded.

2.3.1 Human Body Model (HBM) ESD Test

Human body model (HBM) is a very common model used in the ESD industry sector. HBM simulates ESD events that occur when a charged human body come into contact with an electronic device. This model evaluates the ability of the device to absorb the energy of an ESD event. The typical industry standard used to be specified at 2kV. With the improvement in factory ESD control and higher device performance requirements, HBM specification is trending toward lowering to 1kV [3]. Figure 2.2 shows the equivalent circuit of HBM ESD test condition. In principle, HBM standard describes a current waveform for the discharge of 100 pF capacitor via a 1.5k Ohm resistor and a 0 Ohm load for various discharge voltages [12]. Figure 2.3 shows that the time of the HBM pulse is around 10ns and approximately 150 ns for the decay time [13].