THE DEVELOPMENT OF A CAPACITIVE PARASITIC ELEMENT EXTRACTION AND ESTIMATION METHODOLOGY TO IMPROVE DESIGN CYCLE

By

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LIST OF ABBREVIATIONS

ANOVA	Analysis of Variance
CMP	Chemical Mechanical Planarization
DEF	Design Exchange Format
DFM	Design for manufacturability
DOE	Design of Experiments
DRC	Design Rule Check
EDA	Electronic Design Automation
HDL	Hardware Descriptive Language
IC	Integrated Circuit
ITF	Interconnect Technology Format
LEF	Library Exchange Format
LSD	Least Significant Difference
LSI	Large Scale Integration
LVS	Layout versus Schematic
MSI	Medium Scale Integration
PLL	Phased Locked Loop
RCBD	Randomized Complete Block Design
RTL	Register Transfer Level
SPEF	Standard Parasitics Exchange Format
SSI	Small Scale Integration
ULSI	Ultra Large Scale Integration
VHDL	VHSIC Hardware Descriptive Language
VHSIC	Very High Speed Integrated Circuit
VLSI	Very Large Scale Integration

PEMBANGUNAN METODOLOGI PENGEKSTRAKAN DAN PENGANGGARAN ELEMEN PARASITIK KAPASITIF UNTUK MEMPERBAIKI KITARAN REKABENTUK

ABSTRAK

Dalam industri cip masa kini, sasaran utama organisasi pembangunan cip adalah untuk membangunkan dan mamasarkan cip dalam tempoh masa yang singkat bagi bertapak di pasaran. Keperluan ini menjadi semakin sukar untuk dipenuhi apabila rekabentuk dan pembikinan cip menjadi lebih kompleks disebabkan oleh kemajuan teknologi proses. Justeru itu, objektif penyelidikan ini adalah untuk membentuk aliran kitar rekabentuk cip yang mampu memperbaiki jangka masa di peringkat pengekstrakan elemen parasitik. Aliran rekabentuk ini menggunakan emulasi logam pengisi, dimana ianya berbeza dengan aliran sekarang yang menyertakan logam pengisi secara terus. Dengan menggantikan struktur logam pengisi dengan kaedah emulasi di iterasi awal aliran rekabentuk, penjimatan masa dapat dicapai bagi peringkat penyertaan pengisi. Kaedah rekabentuk eksperimen menggunakan RCBD, ANOVA dan LSD Fisher telah dilaksanakan untuk menentukan lebar logam pengisi emulasi yang sesuai bagi meningkatkan ketepatan emulasi. Eksperimen dilakukan ke atas teknologi proses 45nm dan 65nm dengan kes ujian pelbagai saiz, dari 1000 get ke 21000 get, bagi memerhatikan perbezaan pada keluaran. Apabila dibandingkan dengan aliran rekabentuk umum, 92% daripada semua net dalam rekabentuk mempamerkan perbezaan kapasitans terekstrak kurang 15% bagi 45nm dan 88% pula bagi 65nm. Ini adalah dalam lingkungan ralat 20% yang dibenarkan untuk pengekstrak parasitik 2.5D. Penjimatan masa adalah antara 41% ke 43% berbanding dengan aliran rekabentuk umum bagi 15 iterasi. Bagi penggunaan industri, aliran ini sesuai digunakan untuk rekabentuk yang baru apabila bilangan iterasi adalah tinggi disebabkan oleh pengoptimuman rekabentuk.

THE DEVELOPMENT OF A CAPACITIVE PARASITIC ELEMENT EXTRACTION AND ESTIMATION METHODOLOGY TO IMPROVE DESIGN CYCLE

ABSTRACT

In the chip industry today, the key goals of a chip development organization is to develop and market chips within a short timeframe to gain foothold on market share. Despite this requirement, chip design and manufacturing are increasing in level of complexity due to advancement in process technology. Thus, the objective of this research is to propose a design flow around the area of parasitic extraction to improve the design cycle timeline. The proposed design flow utilizes the usage of metal fill emulation as opposed to current flow which performs metal fill insertion directly. By replacing metal fill structures with an emulation methodology in earlier iterations of the design flow, this is targeted to help reduce runtime in fill insertion stage. Design of experiments methodology utilizing RCBD, ANOVA and Fisher's LSD are used to select an appropriate emulated metal fill width to improve emulation accuracy. The experiment is conducted on 45nm and 65nm process technologies and test cases of different sizes, ranging from 1000 gates to 21000 gates to observe differences exhibited in the outcome. When compared with the general design flow, around 92% of all the nets in the design show differences of lesser than 15% in capacitance value for 45nm and 88% for 65nm. This is in line with the permissible error of a 2.5D parasitic extraction engine to achieve within 20% difference in extracted capacitance values. Runtime reduction achieved was from 41% to 43% lesser than the general design flow for the number of 15 iterations. In industrial usage, this flow is appropriate for new designs where number of iterations required due to design optimization is high.

CHAPTER 1

INTRODUCTION

1.1 Background

In the Very-Large-Scale Integration (VLSI) circuit design scenario today, the key challenges faced by design engineers are shorter time frames in product roadmaps from product definition up to manufacturing and achieving high volume high yield manufacturing. In addition to that, engineers today are also required to address the issues of increasing complexity in design and development which are results of aggressive process technology advancement driven by both market needs and fabrication plants. While the time frame allocated from product definition right up to market penetration is greatly reduced, design engineers are required to ensure that customer requirements are met and high quality and reliability standards maintained if not improved further. The need for design flows and methodologies to assist in reducing project execution timeline has become significantly important.

Process technology scaling is a method employed in foundries to improve on power efficiency, increased performance and area utilization in a chip. While the benefits in power, performance and area are improved, parasitic effects have grown to become a more dominant problem in design [1, 2]. Issues that were negligible in older process technologies are required to be addressed when working with new process technologies. Some examples of such issues are increased noise susceptibility, dominance of interconnect parasitics and system reliability. Newer design flows and methodologies are introduced for improved verification to address these issues to ensure that the fabricated chip is capable of proper operation.

Another major difficulty arising from process technology scaling is to ensure successful chip fabrication with high yield and maintain chip reliability over its lifespan. Design for manufacturability (DFM) is the terminology defining additional methodologies in the existing design flow to improve chip fabrication levels as well as providing sufficient verification for process technologies that are smaller and more difficult to fabricate. While the introduction of such methodologies provides assurance of fabrication output, the design cycle time requires adjustment to accommodate for these methodologies.

In area of parasitic capacitance and resistance extraction, the turn-around time required for large designs is long due to the iterative nature of the processes in physical design execution. The required times for parasitic extraction is further increased with relation to the number of metal layers used in fabrication and interconnect wire routing strategies used in the design. Furthermore, this is further impacted by DFM requirements such as the insertion of dummy metal fill structures in the layout to improve design uniformity and manufacturability. The ability to improve the turn-around time during the physical design iterative processes is able to contribute to shorter design time frames and finally improve the design cycle of a chip.

1.2 Problem Statement

A major issue that arises as process technology advances is the change in parasitic effects. Smaller process technology nodes allow transistors of smaller channel length and narrower interconnect wires. While interconnect nets can be placed closer to each other in the layout, this also results in a particular interconnect net being more

susceptible to negative effects such as crosstalk. The insertion of dummy metal fill into the layout of a design is to ensure that the metal density for each metal layer in the layout achieves a value in a defined range as stated by DFM requirements according to a specific process technology node. It is proven that with the insertion of these dummy metal fills, parasitic effects are affected and this leads to the degradation of performance of the design. While the stage of dummy metal fill insertion is dependent on different implementations in the design flow, design engineers do not have the luxury of flexibility in optimizing and modifying of the design towards the end of the design cycle. In certain scenario's, DFM density value requirements comes in late in the design cycle. Thus, modeling interconnect parasitic capacitance as accurate as possible in the earliest design stage possible is crucial.

1.3 Research Objectives

There are two main objectives focused in this research project :

1. To explore and examine the physical VLSI design flow around the area of parasitic extraction and estimation with metal fill methodology.
2. To develop an alternative design flow utilizing metal fill emulation.
3. To compare the runtime and accuracy performances of the developed design flow versus the conventional design flow which uses metal fill insertion.

1.4 Scope of Research

The scope of this research was focused on design flows employed in the area of parasitic extraction within the structural and physical design phases in IC design. The

process technologies utilized in this research were limited to Intel Corporation's restricted 65nm and 45nm process technologies.

1.5 Contributions of Research

This research contributes to the improvement of the physical design flow focusing on parasitic extraction by reducing the runtime in this area. This in turn helps to achieve shorter turn-around-time and time-to-market which are the key goals of chip design and fabrication organization. In addition to that, this research provides information about the digital integrated circuit design flows from the stage of design ideas and planning to the layout stage.

1.6 Thesis Organization

This report consists of six chapters. Chapter 1 provides information about the motivation, objectives and contributions of this research.

Chapter 2 introduces VLSI design and the ideas behind the VLSI design flow which is widely adopted in industries worldwide. The theory of parasitic devices and their effects towards on-chip interconnect nets are covered next. This is followed by a discussion of the objective of parasitic extraction in the design flow. Subsequently, the changes in parasitic effects and properties as aggressive process technology scaling takes place in circuit fabrication industries are covered. The relation between parasitic changes due to process technology scaling and growing fabrication challenges that lead to the requirement of design for manufacturability is covered. The chemical-mechanical planarization process in integrated circuit fabrication and the importance of metal fill DFM to the fabrication process is discussed. Finally, the

implications of metal fill insertion towards on-chip interconnect performance are illustrated.

Chapter 3 follows up with a review of related design methodologies used around the area of parasitic estimation and extraction around the insertion of metal fill structures in the design layout.

In Chapter 4, the proposed design flow that targets the design cycle improvement in the area of parasitic extraction is introduced. This is followed by an explanation of the methodology of investigation and the process of developing experimental setups which are used during this investigation.

In Chapter 5, analysis of the data sets obtained from the experimental setups is discussed. Analysis is performed using Analysis of Variance and Fisher's Least Significant Difference on the data collected using the Design of Experiments method of Randomized Complete Block Design. From the analysis, the emulated metal fill width that obtains a good accuracy in interconnect capacitance is selected to be used in the proposed design flow. Runtime is tested on a large IP block to observe the runtime improvements in the design cycle when comparing to the conventional metal fill insertion method.

Finally, Chapter 6 concludes the findings from this research and provides recommendations and suggestions in expanding the scope for future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction to Digital Integrated Circuit (IC) Design

In the 1980s, the level of integration for VLSI was achieved. Integrated circuits can fit more than hundreds of thousands of transistors on a single die. VLSI is defined as the process of fabricating integrated circuits which consists of a large number of transistors which is more than 100,000. The concept of circuit integration was deduced back in the 1960s where the first integrated circuits created consist of multiple transistors and provided functionality of a combination of a few logic gates. This level of integration was known as small-scale integration (SSI).

Advancement in integrated circuits in the late 1960s allowed medium-scale integration (MSI), enabling more transistors to be packed into integrated circuits and capability to perform more complex functions. The trend of increasing number of transistors on an integrated circuit continued into the 1970s with the introduction of large-scale integration (LSI). At that point, thousands of transistors could be fitted on a circuit. The term ultra-large-scale integration (ULSI) was proposed for integrated circuits with transistor counts of more than 1,000,000 [3].

Figure 2.1 illustrates the number of transistors that is packed on a single die from 1971 until 2011. Moore's Law which was proposed by Gordon Moore states that transistor count that is packed on a single die continues to double every two years [4]. This achieves a pattern of exponential increase in the number of transistors on a single die.

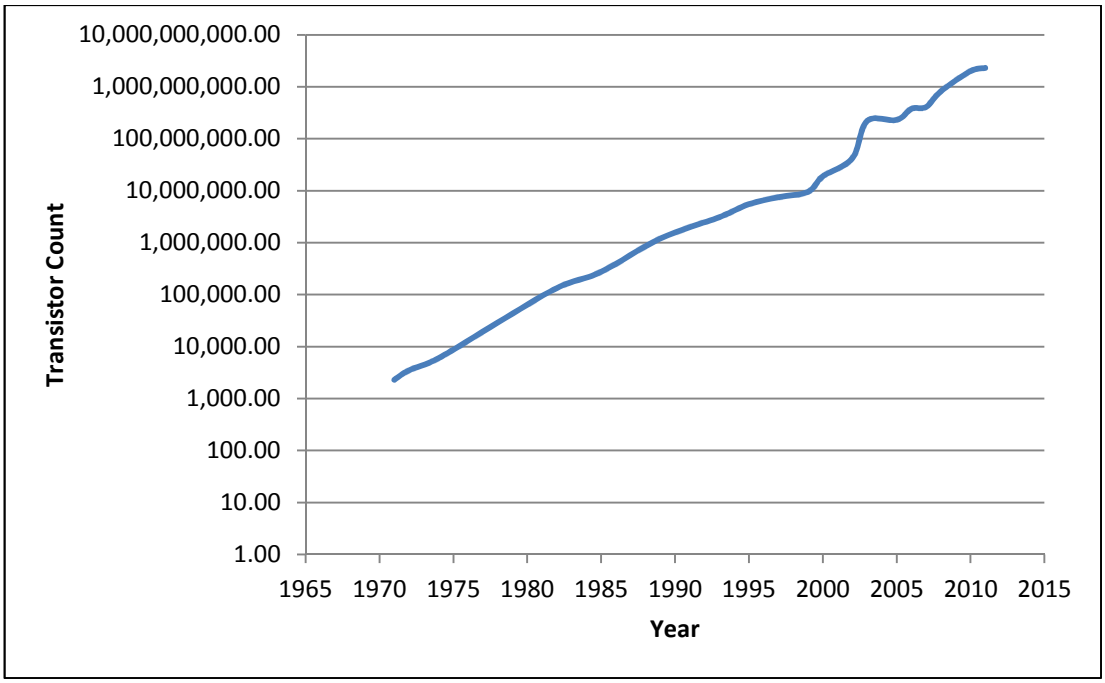

Figure 2.1: Increase in Transistor Count on Single Die (1971-2011) [3]

2.1.1 The General Digital IC Design Flow

With the current level of complexity of functions and operations in an IC, it is difficult to design an IC using previously proposed flows for LSI and MSI. There was a need for systematic and effective methods to ease the task of designing complex ICs.

The IC design flow describes a series of steps needed in the process of designing a chip from the generation of the idea right into fabrication. In order to handle the difficulties encountered during the designing process, the general IC design flow employs the concept of abstraction. The concept of abstraction revolves around iterative processes used to refine an idea of a designated product into a device that can be fabricated.

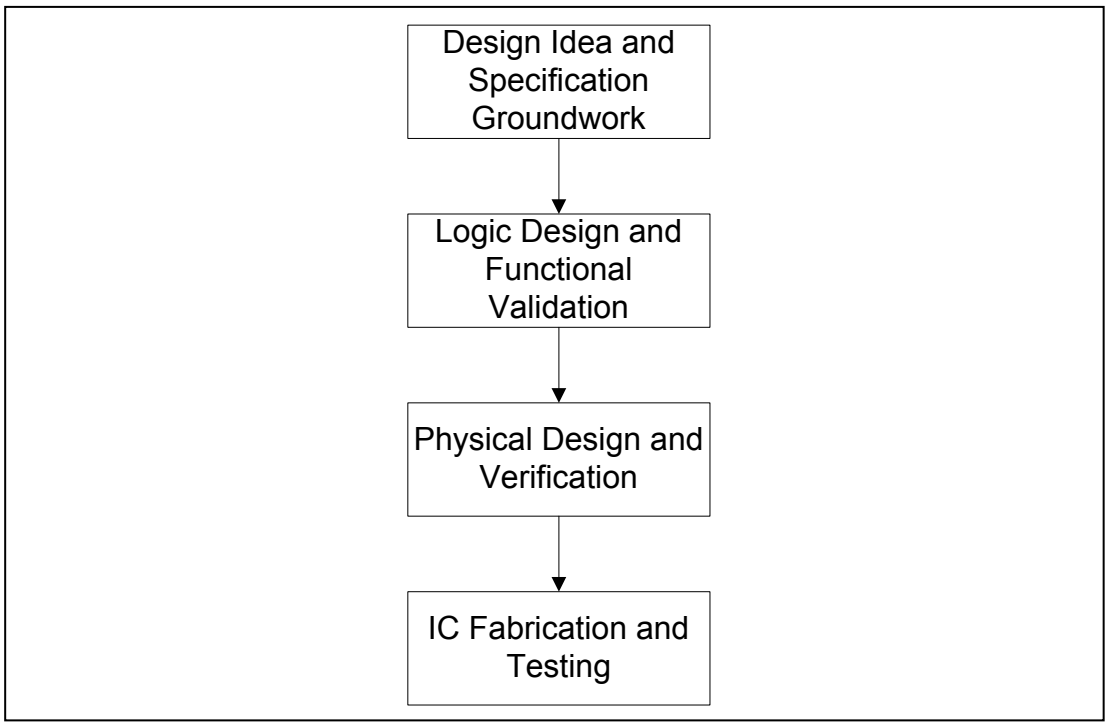

Figure 2.2 : Generalized Digital IC Design Flow [4]

Figure 2.2 illustrates the design stages of a general digital IC design flow, from the development of ideas for the design until fabrication of the chip. More information of the stages is discussed in the subsequent sections.

(a) Design Idea and Specification Groundwork

First, the key functions and goals of the design are defined. At this stage, a high level architectural overview of the IC is drafted. The in-depth level of details is developed and documented as design specifications. Design specification closure is required to be achieved. With fixed target specifications, the next step is to draft the design and schedule plan as well as the delivery schedule is defined to ensure sufficient time for design and fabrication.

(b) Logic Design and Functional Validation

At this stage of design, the main task is to define the design in behavioral model. Hardware descriptive languages (HDL) such as Very High Speed IC (VHSIC) Hardware Descriptive Language (VHDL) and Verilog are widely used to describe the functional operation of each block in the design. In order to achieve a synthesizable design, a lower level of abstraction which is the register transfer level (RTL) is required. RTL describes the data transfer within registers in a design. Validation is performed on the design to ensure that the blocks within the design are functioning as required. Validation is done in an exhaustive manner to ensure survivability of the design as all possible scenarios within the operation of the design needs to be tested.

(c) Physical Design and Verification

The design is implemented as a collection of standard cells, memories, embedded blocks, registers, etc. Physical design covers the entire process of developing the layout of the chip, from planning, physical cell placements, routings, and physical verification to ensure that the IC will work according to specifications.

(d) IC Fabrication and Testing

Once the design layout is completed and verified with high confidence for fabrication, the design will be sent to fabrication plants. After fabrication, the IC testing is performed to determine if it is fully functioning as per specification.

Manufacturing defects are also tested for. If the IC meets its functional and performance requirements with minimal defects, it is cleared for mass production.

2.1.2 Process Technology Scaling

In the context of VLSI design, the term process technology refers to a series of procedures employed in the process of fabricating VLSI circuits on a silicon wafer. Advancements in process technology along different generations are the results of improvement of ability to fabricate transistors on the silicon die which are smaller in terms of dimension when compared to previous generations. Process technology generations are identified according to the dynamic random access memory (DRAM) half-pitch sizing, which is broadly used as a tight indicator of each process technology generation [6]. This identification is also commonly referred to as a process technology node.

Table 2-1 : Process Technology Nodes and Their Year of Introduction [4]

Year	Process Technology Node
2000	130 nm
2002	90 nm
2006	65 nm
2008	45 nm
2010	32 nm
2011	22 nm

Table 2-1 above illustrates the changes in process technology node according to the year the process technology was introduced for a period of 12 years from year 2000 until year 2011.

Advancements in process technology are driven by the fundamental requirements of VLSI circuit improvements in terms of performance, area and power

utilization. It is observed that as process technology scales further into the submicron region, gate dimensions and delay are reduced by approximately 30%. In addition, scaled-down dimensions of transistors allow even higher transistor densities to be placed on a die. As observed, the transistor density should approximately double in number for every technology generation. Last but not least, power utilization of a chip is projected to reduce every technology generation.

While process technology scaling from generation to generation is proven to be beneficial in terms of performance, power and area, the challenges in other areas of VLSI design are increasing. In the area of parasitic effects, it is observed that process technology scaling results in the growing significance of interconnect parasitics compared to gate parasitics [7].

2.1.3 Design for Manufacturability

DFM is defined as methodologies that are introduced along with the design flow in order to ensure that a design is able to be successfully manufactured repeatedly, consistently, reliably, and cost effectively. All these DFM requirements are defined by foundries and implemented throughout the processes of design, manufacturing and assembly. There are two key motivations behind the introduction for DFM. The first motivation is regarding minimizing of production costs of a project. The second motivation is focused on minimizing potential losses which are associated to defective parts and products in manufacturing. This results in a clear need in the industry where potential issues and problems which may affect the revenue of a given product needs to be detected and eliminated as early as possible in the product design and development cycle [8].

In the past, both design houses and foundries were working as separate entities. IC designs were developed independent of fabrication requirements. A major negative outcome due to individuality of both bodies was that high percentage of chip designs were unable to be manufactured. Some designs could be manufactured, but achieved low yield rates. To overcome this longstanding issue, both design houses and foundries came up with the DFM methodology. DFM incorporates manufacturing requirements and considerations into the design flow.

While DFM is crucial in terms of quality manufacturing, cost effectiveness and high yield, it actually increases the complexity in the design process. Design engineers will now have to consider DFM requirements apart from changes along process technology generations. An example of DFM required is the sufficiency of metal density in a design.

2.2 On-chip Interconnect Structures and Parasitic Devices

In an IC, interconnect structures are used as a medium for signal propagation among devices. Continuous advancement in process technology has resulted in smaller device dimensions, but increased functionality and complexity. While the device dimensions have shrunk due to feature size reduction, interconnect dimensions are also scaling but at a lower rate [9].

2.2.1 Interconnect Structures in an IC

In an IC, wires are also termed as on chip interconnects. The interconnect network in an IC is formed out of multiple metal layers stacked above each other with a separating layer of oxide between metal layers. These layers are connected to each

other using a structure called vias. Each metal layer has an alternate orientation. For example, odd numbered metal layers are specified for horizontal connections and even numbered metal layers are specified for vertical connections. A net in a layout may be routed using more than one layer of metal.

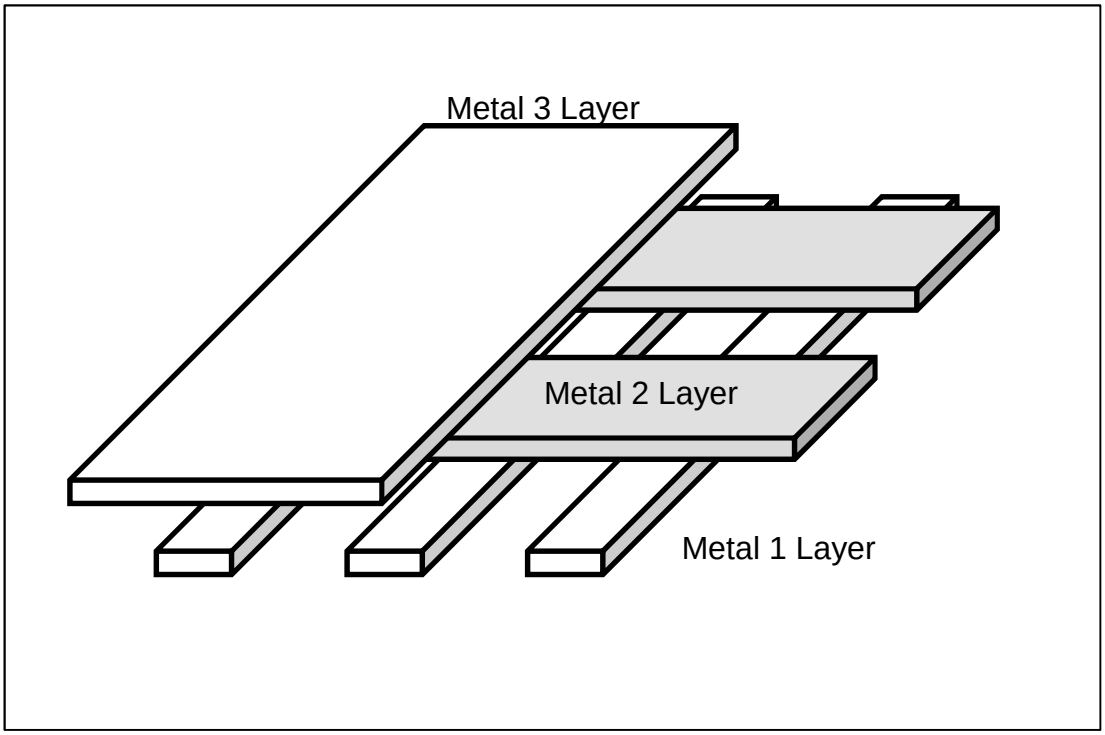

Figure 2.3 : A 3D view of interconnect structures in an IC

Figure 2.3 depicts a sliced out portion of how metal layers that form interconnect structures are laid in the IC. In an ideal situation, it is assumed that signal propagation from cell to cell through an interconnect structure instantly without any effects of delay. However, in a practical scenario, signal propagation is affected by the effects of parasitic devices found on the interconnect structures. Effectively, an interconnect structure can be modeled similarly to a transmission line model. Figure 2.4 illustrates the representation of an interconnect net modeled similarly to a transmission line [10].

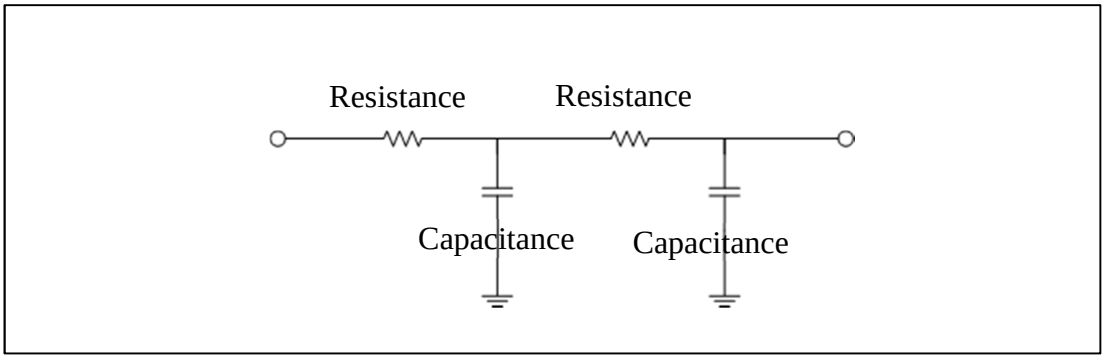

Figure 2.4 : A representation of an interconnect net as a transmission line [10]

2.2.2 Parasitic Resistance

Resistance is defined as the property of a particular material of interest which opposes the flow of current through that material in the unit of ohms. Since resistance is an electrical property that is not affected by any field or fringe effects, resistance of a metal interconnect strap can be computed if the resistivity parameter and dimensions of the material is known. Resistance of a metal interconnect strap can be computed with the following equation :

$$R = \rho\left(\frac{L}{Wt}\right) = R_s\left(\frac{L}{W}\right) \quad 2.1$$

where R represents resistance of the metal interconnect strap, ρ is the resistivity of the metal strap material, L is the corresponding length of the metal strap, W is the corresponding width of the metal strap, and t is the thickness of the metal strap.

In design library notations, R_s denotes the sheet resistance of the interconnect material which is a function of resistance over the thickness of the material. Such values in the design library are represented with unit of ohms per unit thickness.

Material resistivity is determined mainly by its chemical composition. On the other hand, geometrical parameters of length, width and thickness are dependent on the fabrication capability of a certain process technology. For example, minimum width and metal thickness are defined parameters in a process technology that states the smallest interconnect width and metal thickness that can be fabricated in a particular process technology. With routing information available in any layout, a layout extractor tool is able to compute the parasitic resistance of interconnect nets with high accuracy.

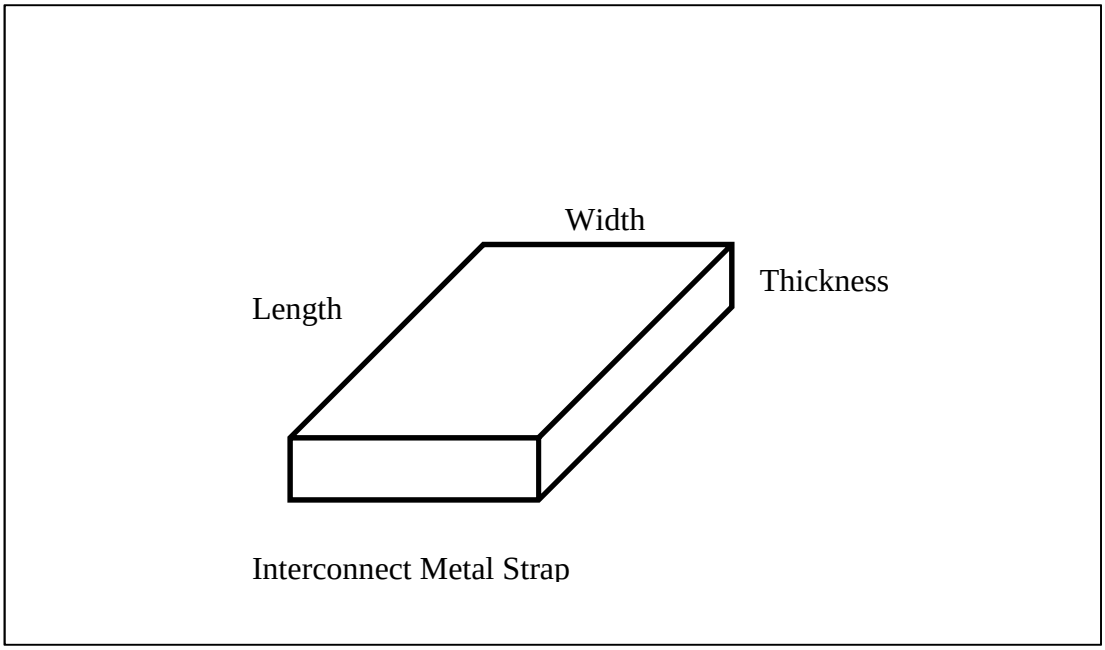

Figure 2.5 : Geometrical parameters of a metal interconnect for resistance estimation

2.2.3 Parasitic Capacitance

In the past, delay was mainly associated with the gate level parasitics. Due to process technology scaling, the dimension of devices have shrunk at a higher rate compared

to interconnect dimensions. At present, the propagation delay in an IC is largely due to the interconnect capacitances and device and the interconnect resistances. While parasitic resistance was simple to estimate, parasitic capacitance requires more consideration and advanced methods for estimation due to field effects. Accurate capacitance estimation requires taking into account fringing effects and also interconnect locality with respect to other interconnects which are routed close together.

Total capacitance, C_T, of a node is given as the summation of all capacitive elements :

$$C_T = C_{PP} + C_C + C_{fr} \tag{2.2}$$

where C_{PP} refers to total parallel plate capacitance at the node which accounts for both interlayer and intralayer parallel plate effects, C_{fr} is the capacitance from fringing effects, and C_C is the coupling capacitance effects [11].

(a) Parallel Plate Capacitance

Parallel plate capacitance describes the basic occurrence of a capacitive-like structure in the chip. An interconnect metal strap running in parallel with the silicon substrate separated by a dielectric layer will form such capacitance. Parallel plate capacitance, C_{PP}, between the interconnect metal strap and the substrate layer can be represented by the equation :

$$C_{PP} = \varepsilon_{OX}\left(\frac{WL}{t_{OX}}\right) \tag{2.3}$$

where ε_{OX} is the value of the dielectric constant, W is the width of the corresponding interconnect metal strap, L is the length of the interconnect metal strap, and t_{OX} is the thickness of the dielectric layer.

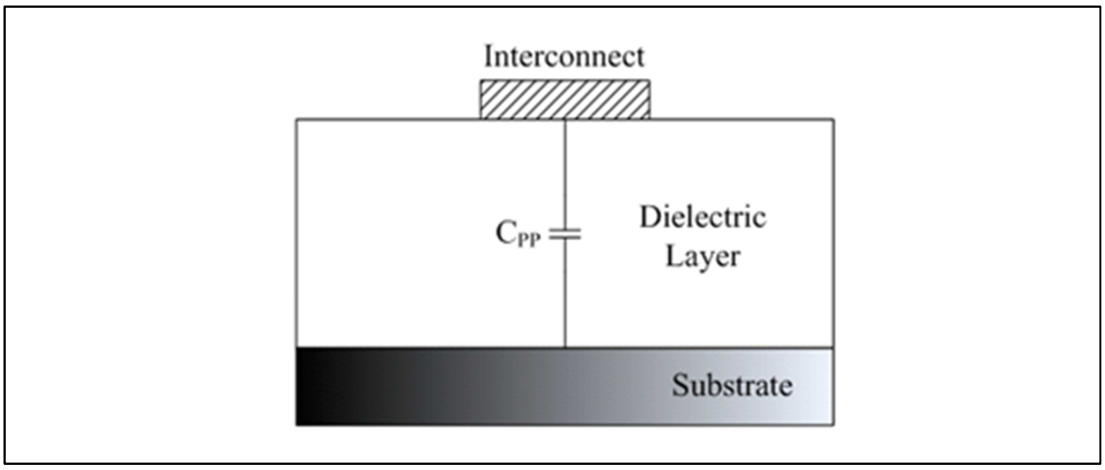

Figure 2.6 : Parallel plate capacitance [12]

The structure of the formation of parallel plate capacitance is illustrated in Figure 2.6. C_{PP} is the capacitance formed when the interconnect metal and substrate form a parallel structure. A noticeable change as interconnect geometry scales down is lower values for parallel plate capacitance as the effective area of the metal interconnect forming a parallel plate structure is reduced.

(b) Fringing Capacitance

For a similar structure as in the case of a parallel plate capacitance, interconnect nets with current passing through it emits electric fields from their edges. Fringing fields are affected by the circumference and the thickness of the interconnect line. Fringing capacitance also contributes to higher total capacitance of an interconnect structure.

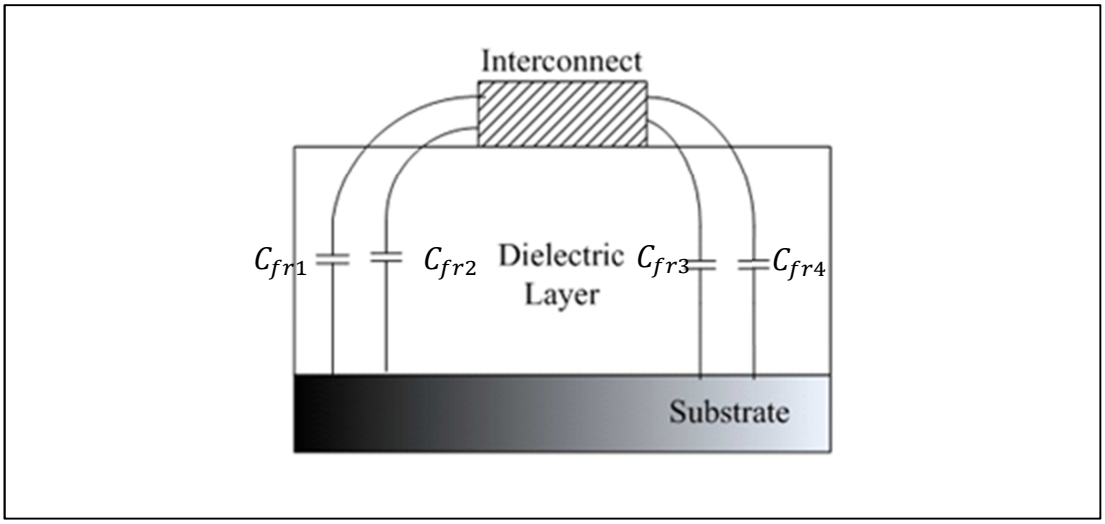

Figure 2.7 : Fringing capacitance in a parallel plate structure [11]

(c) Coupling Capacitance

In an IC that contains multiple layers of metal for interconnect building, electric field lines exists among interconnect lines. Capacitance that exists due to such circumstances is known as coupling capacitance. Coupling capacitance is a major contributor of crosstalk noise among interconnects.

In Figure 2.8, a structure with multiple metal layers for interconnects illustrates the formation of coupling capacitance among interconnect pairs. The terminology for coupled pairs of interconnects on the similar metal layer is called intralayer coupling, which is depicted by capacitance C_{c1} and C_{c2}. Coupling among interconnect pairs of different layers is known as interlayer coupling. Interlayer coupling is depicted by capacitance C_{c3}, C_{c4} and C_{c5}.

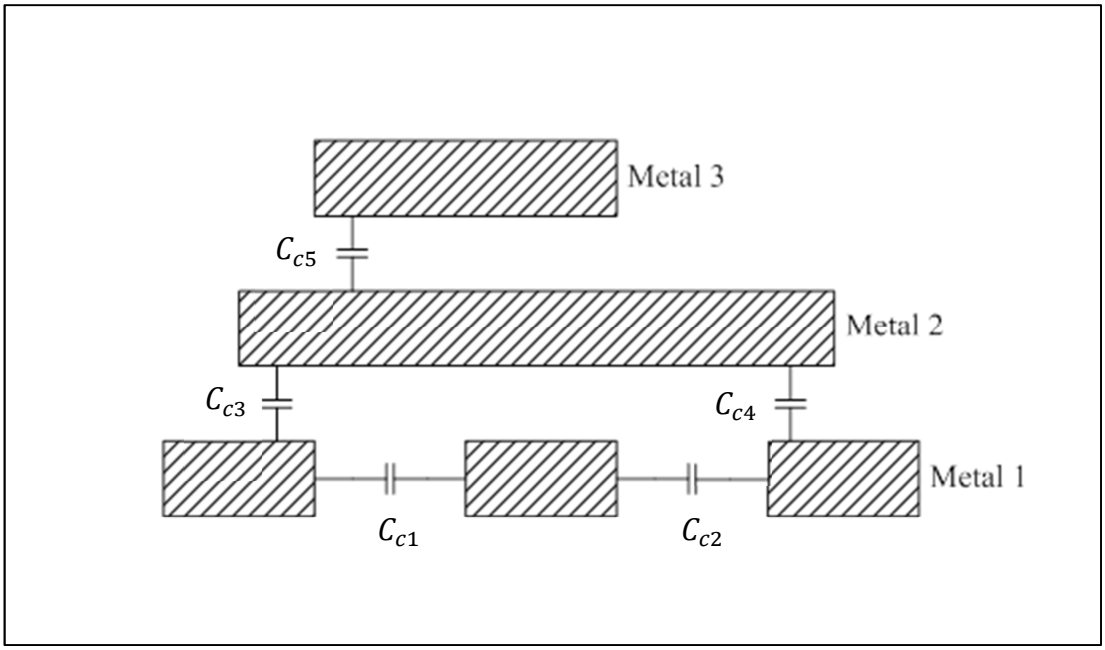

Figure 2.8 : A depiction of coupling capacitances on multiple interconnect nets

2.2.4 Effects of Parasitic Devices towards Interconnect Nets in an IC

(a) IR Drop Issues

IR drop is defined as drop in voltage when current flows through any material with resistive property [12]. In an IC, interconnect nets are collections of multiple connected metal straps connected together with bridging elements called vias. These metal straps exhibit resistive property, which increases as the length of metal straps used, becomes longer.

In accordance to Ohm's Law, voltage at the start point of a net and the end point of the net is different. With reference to Figure 2.9, IR drop over this metal strap when current flows from left to right, V_{12}, can be represented with :

$$V_{12} = V_1 - V_2 = IR \qquad 2.4$$

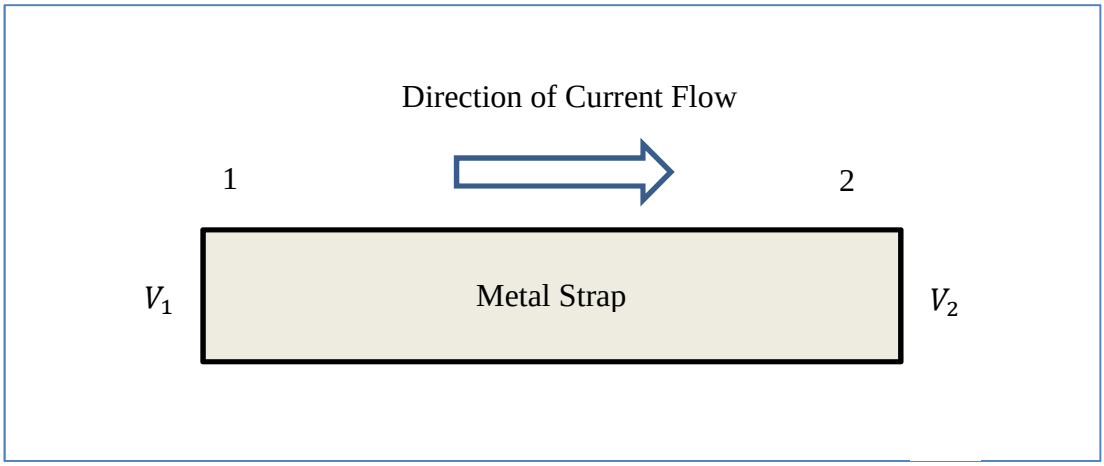

Figure 2.9 : Voltage difference over two points of a metal strap in an IC

where V_1 is the voltage potential at end 1 of the metal strap, V_2 is the voltage potential at end 2 of the metal strap, *I* is the current that flows through this metal strap, and *R* is the resistance of the metal strap.

In the IR drop problem, net types such as power nets are more commonly affected. At smaller process technologies, less power is required for transistor switching. Lower required voltage threshold also translates into lower noise margin, which increases difficulty in differentiating noise versus signal. Thus, a stable supply of power is required and only a small IR drop margin is permitted. Insufficient supply of power to transistors due to excessive IR drop may cause the circuits not to function as intended. This problem is more severe for large chips where power nets are routed longer and narrower due to smaller net widths for smaller process technologies.

(b) Electromigration

Electromigration is a process where atoms of a conducting material are displaced when current flows through the material [13]. This is a gradual process and happens over a period of time. In an IC, this phenomenon occurs on metal straps used as interconnect wires. Metal ions are forced to drift in the similar direction as electron flow if current density over the metal strap is too high. Thus, there is a required limit of permissible current flow through the metal straps in an IC.

Two issues that arise from excessive electromigration are voids and hillocks. A void will take place when more metal ions drift out of position than the number of metal ions drifting into position to fill the gap. Over a certain period of time, the metal strap may break and cause an open circuit at the breaking point. Alternately, the hillock situation occurs when too many metal ions drift into position as opposed to the outflow of ions, causing them to pile up at certain location. If this location is close to a neighboring net, the piling up of metal ions may cause a short circuit. Both of these occurrences will result in chip failure.

(c) RC Delay

Ideally, it is assumed that a propagated signal arrives at its destination instantly. However, in practical implementation, delay exists in signal propagation from one point to another through nets in an IC. This delay is the resultant of parasitic effects of the material used for interconnects. This problem is more severe with technology scaling, where interconnect delay is the dominant component of propagation delay compared to gate delay. Delay caused by parasitic resistance and capacitance increase as wire length used for routing is increased.

2.3 Parasitic Estimation and Extraction in Digital IC Design Flow

In various stages of the design flow, different methodologies are employed to obtain parasitic data. As the design process advances through different stages, more information becomes available. Hence, parasitic data with higher accuracy can be obtained in later stages.

2.3.1 Parasitic Estimation in Pre-Layout

At this stage of design, there is little or no physical information available for parasitic estimation. A commonly used delay model in this stage is the wire-load model. The wire-load model estimates average wire lengths, capacitance and resistance based on block size or chip size and the number of fanouts on a particular net [14]. Wire length is modeled as a function of number of fanouts.

Once the wire length is estimated, interconnect capacitance can be computed with the following equation :

$$C_{net} = LC \tag{2.5}$$

where C_{net} is the interconnect net capacitance, L is the estimated length of the interconnect net, and C represents the estimated capacitance per unit length coefficient from design library. At this stage, fringing effects of capacitance are not considered.

Similarly, interconnect resistance can be computed using the following equation :

$$R_{net} = LR \tag{2.6}$$

where R_{net} is the interconnect net resistance, L is the estimated length of the interconnect net, and R represents the estimated resistance per unit length coefficient from design library.

Once the capacitance and resistance values are available, interconnect delay can be computed. Different RC tree models are available to model real world cases for delay computation. The best case tree is modeled with the assumption that the load is adjacent to the driver. The balanced tree provides the model of a situation where each path leading to all the loads connected has equal resistance and capacitance. The worst case tree models the connection in a way that driver and loads are physically located far away from each other. In this case, it is assumed that each path from driver to load is affected by total capacitance and total resistance which was pre-calculated earlier.

One downside of the wire-load model is the accuracy of parasitics estimated as it is based on predefined values in the design library which does not account for external influences and wire length estimation might not be accurate at this point. However, the wire-load model is still utilized to provide designers with a rough estimate of parasitics early in the design cycle.

2.3.2 Parasitic Estimation during Post-placement, Pre-route Stage

After the synthesis, design planning and placement, location of devices in the floorplan is defined although routing topology is still unknown at this stage. At this point, since the source and destination is known, the wire length and possible routing can be predicted more accurately. Wire length is estimated using distance based algorithms such as the shortest Manhattan distance. In the shortest Manhattan

distance algorithm, wire length is estimated by the shortest right angle routing distance from the initial point to the endpoint.

Resistance and capacitance are calculated using equations, but the process of determining wire length needs to account for routing strategy and congestion issues. Algorithms are deployed to determine track congestions and select appropriate and logical routing strategies to determine wire length.

2.3.3 Layout Parasitic Extraction

At this stage, device placements are refined and interconnect wires are routed. Actual geometry, orientation and location of interconnect and via polygons are known. At this stage, parasitic resistance is able to be extracted accurately. Parasitic capacitance extraction at this stage provides higher accuracy as fringing and coupling effects between interconnect polygons is simulated. Parasitic extraction at this stage may employ different solving strategies for improved accuracy.

2.4 Metal Fill in IC Design

Metal fills are structures that are used to pad areas in the layout that is sparse in order to promote layout pattern uniformity and to achieve minimal metal density for each metal layer in the layout. Metal filling is a crucial requirement in DFM to ensure that an IC can be fabricated successfully with high yield and minimal defects. The insertion of metal fill structures into a layout does not affect or modify the functionality of the chip. These structures are also known as dummy fill as they do not serve any operational purpose within the chip. The following sections relate the need of metal fill insertion due to the fabrication process.