DESIGN OF A LOW POWER 5-Gb/s FULLY BALANCED AND DIFFERENTIAL OUTPUT TRANSIMPEDANCE AMPLIFIER

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2013

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by

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Thesis submitted in fulfilment of the requirements for the degree of Master of Science

JULY 2013

DECLARATION

I hereby declare that the work in this thesis is my own except for quotations and summaries which have been duly acknowledged.

2 July 2013 Balasubramaniam Shammugasamy

S-LM0226

ACKNOWLEDGEMENTS

Firstly, I would like to thank my supervisor, Dr. Tun Zainal Azni Zulkifli, for his fullest support throughout the project. His guidance and technical expertise in the area of analog IC design have been the key support for the completion of this thesis. The continuous ideas for improvement and the time spent on the project undertakings are very much appreciated. I would like to thank him not only as a supervisor but as a friend for the motivational support as being in the industry and doing research require a lot of compromising.

Secondly, I would like to thank USM's RMIC team members for their contributions towards the completion of this project. My sincere appreciation goes to Dr. Harikrishnan Ramiah for his technical guidance on the project execution and the publication of two papers to fulfill thesis requirement. Next, my thank-you goes to Dr. Norlaili Mohd Noh, Pn. Nor Amalia Sapiee and RMIC lab mates who have given me fullest technical support in implementing the project.

Amongst my friends, I would like to thank Sureshkumar Kandasamy, Selvarajah Krishnarajoo, Nanthakumar Dorairaj, Chandramohan Muthusamy, Joel Samson and Ling Kian Teck for their continuous motivational support whenever I am in the down-time throughout the project undertakings. A special thank-you goes to my former manager, Saravanakumar Kuppusamy who had given me the opportunity to be in the IC design field.

I would like to acknowledge as well Albert Victor Kurdesch of Silterra for the collaboration and MOSIS for the IBM Process Design Kit (PDK). The MOSTI grant number is 03-01-05-SF0302

Finally, my sincere thank-you goes to my loving family who always motivate me to go for tertiary studies. A special thank-you to my mother, Kamatchy Ramoo for making a glass of milk every time I sleep late working on the thesis.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

HDMI High Definition Multi-media Interface

TMDS Transition Minimized Differential Swing

EMI Electromagnetic Interference

TIA Transimpedance Amplifier

dB Decibel

GHz Gigahertz

RFI Radio Frequency Interference

CMOS Complementary Metal-Oxide-Semiconductor

HDTVs High Definition Televisions

PCs Personal Computers

BJT Bipolar Junction Transistor

IP Intellectual Property

IBM International Business Machine

RGC Regulated Cascode

CMFB Common-Mode Feedback

DC Direct-Current

PVT Process, Voltage, Temperature

Rx Receiver

Tx Transmitter

NRZ Non-Return-to-Zero

MUX Multiplexer

CMU Clock Multiplying Unit

LA Limiting Amplifier

CDR Clock and Data Recovery

DEMUX Demultiplexer

AGC Automatic Gain Control

RF Radio Frequency

ISI Intersymbol Interference

BER Bit-Error-Rate

rms Root-Mean-Square

CG Common-Gate

KCL Kirchhoff's-Current-Law

CS Common-Source

LVS Layout-vs-Schematic

DRC Design-Rule-Check

NMOS N-type Oxide Semiconductor

LPF Low Pass Filter

Vref Voltage Reference

SF Source Follower

PM Phase Margin

ESD Electrostatic Discharge

PSRR Power Supply Rejection Ratio

SNR Signal-to-Noise-Ratio

VCSEL Vertical Cavity Surface-Emitting Lasers

CDS Cadence Design Systems

EDA Electronic Design Automation

LIST OF SYMBOLS

Ω	Ohm
γ	Coefficient of channel thermal noise
C_{gd}	Gate-drain capacitance (F)
v_b	Transistor bias voltage (V)
V_{ds}	Drain-Source voltage (V)
i_b	Transistor bias current (A)
C_{gs}	Gate-source capacitance (F)
C_{ds}	Drain-source capacitance (F)
C_p	Parasitic capacitance (F)
C_{pd}	Photodiode capacitance (F)
C_s	Degenerative capacitance (F)
R_s	Series Resistance (Ω)
R_D	Load Resistance (Ω)
q	Electron charge ($1.6\times10^{-19}C$)
I_{DC}	Signal DC Current (A)
BW	Bandwidth (Hz)
Z_T	Transimpedance gain (dBΩ)

v_{out}	Output Voltage (V)
v_{in}	Input Voltage (V)
i_{in}	Input Current (A)
f_T	Transition Frequency (Hz)
f	Frequency (Hz)
g_m	Transconductance of the MOS device (S)
k	Boltzmann constant (k =1.38 $\times 10^{-23} J/K$)
L	MOSFET's channel length (μm)
R	Photodiode Responsivity (A/W)
I_{PD}	Photocurrent (A)
P_{in}	Input Optical Power (dBm)
RC	Carrier Transit time (s)
f_{-3dB}	-3-dB Bandwidth (Hz)
$i_{n,in}$	Input-referred noise current (A_{rms})
i_s^{pp}	Minimum input current signal to TIA (A)
Q	Quality Factor
$I_{n,TIA}^{rms}$	TIA Input-referred rms noise current (A_{rms})
$i_{n,in}^2(f)$	Input-referred noise current spectrum (A^2/Hz)
i_{eq}^2	Equivalent input noise current spectral density (A^2/Hz)

Z_{in}	Input Impedance (Ω)
r_o	Output impedance of MOS device in saturation region (Ω)
$v_{n,out}^2$	Output referred noise voltage (V^2/Hz)
R_F	Shunt feedback resistor (Ω)
A_V	Open loop voltage gain (dB)
r_e	Extinction ratio (dB)
A	Amplifier voltage gain (dB)
P_1	Optical power generated when light source is "ON" (dBm)
P_0	Optical power generated when light source is "OFF" (dBm)
C_{ox}	Oxide capacitance per unit area (F/cm^2)
T_{ox}	Oxide thickness (Å)
$K'n$	Transconductance parameter in saturation region ($\mu A/V^2$)

PUBLICATIONS

B. Shammugasamy, T.Z.A Zulkifli and H. Ramiah, “A 24mW, 5Gb/s Fully Balanced Differential Output Transimpedance Amplifier with Active Inductor and Capacitive Degeneration Techniques in 0.18-μm CMOS Technology," *IEICE Electronic Express*, 7(4):308-313,Feb 2010.

B. Shammugasamy and T.Z.A Zulkifli, “A 10-Gb/s Fully Balanced Differential Output Transimpedance Amplifier in 0.18-μm CMOS Technology for SDH/SONET Application," IEEE Asia Pacific Conference on Circuits and Systems, pages 684-687,Jan 2009.

REKABENTUK PENGUAT TRANSIMPEDANS SEIMBANG PENUH DAN KELUARAN KEBEZAAN BERKUASA RENDAH 5-Gb/s

ABSTRAK

Tesis ini membentangkan sebuah rekabentuk penguat transimpedans (TIA) untuk antaramuka multimedia berdefinasi tinggi (HDMI) yang beroperasi pada kadar data 5-Gb/s. TIA direka dengan konfigurasi seimbang sepenuhnya dan keluaran kebezaan daripada satu bekalan kuasa 1.8-V untuk penolakan hingar yang lebih baik bagi mencapai sensitiviti optik masukan yang optimum. Rekabentuk ini dilaksanakan dengan menggunakan teknologi pelengkap logam oksida semikonduktor (CMOS), 0.18-μm kerana ia menyediakan lebar jalur yang lebih tinggi berikutan penskalaan teknologi. TIA menggunakan litar kaskod dikawal selia (RGC) sebagai blok masukan pengasingan kapasitan fotodiod dan diikuti dengan peringkat suap balik pirau untuk amplifikasi pembezaan ayunan. Untuk memenuhi keperluan lebar jalur pada 4-GHz dalam rekabentuk TIA, teknik aktif induktor dan kapasitif de-generasi telah dilaksanakan dalam blok RGC dan senibina suap balik pirau yang sedia ada. Kedua-dua perlaksanaan ini melanjutkan lebar jalur tanpa menggunakan sejumlah besar arus terus (DC) untuk memacu beban output kapasitif. Rekabentuk TIA juga menggunakan suap balik mod-am (CMFB) dan litar pembatalan rangkaian ofset DC untuk membentuk pembezaan TIA yang seimbang sepenuhnya, khusus untuk peningkatan penolakan hingar mod biasa

dan sensitiviti masukan yang lebih baik bagi antaramuka HDMI optik. Simulasi telah dijalankan untuk mengukur gambarajah mata keluaran, penghitungan masukan hingar yang dirujuk, gandaan pembezaan transimpedans dan kestabilan system gelung. Simulasi akhir menunjukkan bahawa pembezaan TIA mencapai gandaan sebanyak 66-dBΩ dengan lebar jalur 4-GHz pada -3-dB. Rekabentuk TIA dapat mencapai sensitiviti optik masukan sebanyak -19-dBm dan hanya menggunakan kuasa 24-mW dari bekalan 1.8-V tanpa penampan untuk memacu beban 50-Ω. Keluaran mata-rajah plot pada pelbagai kadar data sehingga 5-Gb/s menunjukkan pembukaan mata yang luas, yang membolehkan rekabentuk TIA dilaksanakan dalam penerima optik antaramuka HDMI.

DESIGN OF A LOW POWER 5-Gb/s FULLY BALANCED AND DIFFERENTIAL OUTPUT TRANSIMPEDANCE AMPLIFIER

ABSTRACT

This thesis presents the design of a Transimpedance Amplifier (TIA) for the HDMI interface operating at data rate of 5-Gb/s. The TIA design employs a fully balanced and differential output configuration from a single 1.8-V power supply for better noise rejection to achieve good input optical sensitivity. This design is implemented using 0.18-μm Complementary Metal-Oxide-Semiconductor (CMOS) technology as it provides higher bandwidth due to technology scaling. The TIA uses the Regulated Cascode (RGC) circuit as an input block for photodiode capacitance isolation and shunt feedback stage for differential swing amplification. To meet the requirement for 4-GHz bandwidth in the TIA design, an active inductor and capacitive de-generation techniques have been implemented in the existing RGC and shunt feedback architecture, respectively. These two implementations extend the bandwidth without using a large amount of Direct-Current (DC) current to drive output capacitive load. The TIA design also employs the Common-Mode Feedback (CMFB) and DC offset cancellation circuit to form a fully balanced and differential output configuration, specifically for the improvement of common mode noise rejection and better input sensitivity for HDMI optical interface. The simulation was carried out to measure the output eye diagram, input-referred noise calculation, differential transimpedance gain and the system

loop stability. The final simulation shows that the differential TIA achieves the gain of 66-dBΩ with the -3-dB bandwidth of 4-GHz. The TIA is able to achieve the input optical sensitivity of -19-dBm and it only consumes 24-mW power from a single 1.8-V supply without a buffer to drive 50-Ω load. The output eye-diagram plot at various data rates up to 5-Gb/s shows a wide eye opening, which enables the TIA to be implemented in optical receiver design in HDMI optical interface.

CHAPTER 1

INTRODUCTION

Today's consumers market are equipped with the high-end electronic products that benefit consumers with a number of multimedia applications. The overwhelming growth in the multimedia networking system have enhanced the data communications going to gigahertz range in which have paved the way for High Definition Multi-media Interface (HDMI) standard. HDMI is an interface established for digital data transmission by providing a solution to transmit a large uncompressed video and audio quality signals over a single cable connector. HDMI technology is a global industry standard for connectivity high-definition products like High Definition Televisions (HDTVs), Blu-Ray Disk player, Multimedia Personal Computers (PCs), gaming systems, digital cameras and many more (HDMI.org, 2003). HDMI uses Transition Minimized Differential Signaling (TMDS) which is a technology optimized for robust digital data transmission while minimizing Electromagnetic Interference (EMI). TMDS features a number of techniques. In general, when high speed data are being sent over a long cable, the process of sending the data becomes difficult in term of signal quality while transmitting, however TMDS is enhanced with a number of techniques that the receiving device is able to reconstruct the exact data bits by the source device. HDMI standard of version 1.0 to 1.2 set the maximum data rate of 5-Gb/s for digital transmission. The latest HDMI 1.3 standard have doubled the data rate up to 10-Gb/s for the future needs. The increased in the bandwidth enables HDMI 1.3 to have a higher

display resolution and improved colour depth on the high quality picture. Eventhough HDMI 1.3 is operating at the data rate of 10-Gb/s, it is still fully backwards compatible with previous versions of HDMI standard.

However when it comes to HDMI data transmission, there are two options, which are copper or fiber optics connection. For a low data rate, both copper and fiber connection plays about the same advantage, but it is different when comes to full motion uncompressed video signals. Due to nature of digital signals with the natural impedance and inductance of copper, fiber optic conversion technology is usually the best connection medium for longer length HDMI signal extension. As the high bandwidth data is being transmitted, the impedance of many copper cables can cause signal loss which results in poor signal quality at the receiving end. Generally fiber optic connection is preferred over copper cable as they can be deployed in environment with large EMI and Radio Frequency Interference (RFI). With fiber optic conversion technology, there is theoretically zero impedance and thus zero loss as the digital electrical system is converted into light-waves at the video source and the signal travels in light form until it reaches the display and is reconverted into digital electrical signals.

1.1 Problem Statements

Focusing on the optical communications system in demand with the higher data rate transfer for HDMI interface, the enhancement on the existing optical receiver is needed on the analog front-end part which consists of a photodiode and a pre-amplifier which is specifically referred as TIA. As the data rate for electronic consumers products keep increasing, the need for high bandwidth design is given due diligence. With the in-

crease in design bandwidth, generally the power consumption of a circuit is increased together with the area growth on a chip. In the recent days, the optical receiver design with CMOS technology have provided a number of advantages over the Bipolar Junction Transistor (BJT) process like the low power, low cost, less design complexity, ease of integration on a single a chip with other Intellectual Property (IP) blocks. In the past, many papers featuring an optical receiver operating at 10-Gb/s in 0.18-μm CMOS were published. But due to the implementation of on chip spiral inductor for the bandwidth extension purpose, the design is not feasible for data rate range of 5-Gb/s in the economical perspective. In today's on die system design, many chip manufacturers are targeting small die area, thus the market competition is there, means bulky on chip spiral inductor is not preferred although functionally the design is capable to extend bandwidth. An optical receiver for HDMI application was implemented in using 0.18-μm CMOS as in (Yun et al., 2009), but the data rate is only up to a 4-Gb/s. A low power 5-Gb/s TIA was published in (Goswami et al., 2009), but it was fabricated using a high cost 0.13-μm CMOS. In this thesis, a low voltage, low power and fully balanced differential output TIA is designed to operate up to a 5-Gb/s data rate using the International Business Machine (IBM) and Silterra 0.18-μm mixed signal CMOS process technology for comparison studies.

1.2 Objectives

This project is focused on bandwidth extension, area minimization and power reduction to overcome the issues stated in Section 1.1:

1. To explore the alternative method on bandwidth extension aimed at 5-Gb/s.

2. To design the TIA from a single power supply, in this case only 1.8-V power supply is targeted compared to previous designs using multiple power rails for bandwidth extension in the differential configuration. The differential architecture is aimed to reduce the overall input-referred noise for high input sensitivity.

3. To perform a comparative study between the IBM and Silterra 0.18-μm CMOS process on the performance of the design parameters on selected blocks.

1.3 Project Scope

The project will focus on optical receiver system with narrowing down to TIA system design. The TIA is the critical block in the analog front-end of optical receiver system, thus the improvement are aggressively planned to control the TIA performance over a number of factors, namely the gain, sensitivity, power consumption and area. Therefore, the scope of the project is targeted for the improvement of the TIA system. The project is focused on circuit simulation and layout implementation to meet the design requirement.

1.4 Organization of the Thesis

The thesis is organized as follows:

The thesis introduction together with the design motivations, problem statements, project objectives and organization of the thesis are given in Chapter 1.

In Chapter 2, a brief discussion about optical receiver system is presented. The

topic covers the design criteria of the low power, high bandwidth TIA design. The analysis of the existing TIA architecture is discussed for the high bandwidth and low power application. As overall, this chapter described about the various type of TIA topologies implemented in CMOS technology.

Chapter 3 explains the thorough design study on the sub-blocks used to implement the TIA. The various block like the modified RGC for bandwidth extension, shunt feedback, high gain differential amplifier, CMFB for DC cross over control, DC offset cancellation cirucit and output buffer to drive the load are discussed.

Chapter 4 presents the integration of the sub-blocks discussed in Chapter 3 to build a differential TIA design. The differential design enhanced the overall TIA gain and directly reduced the input-referred noise. The complete layout of the sub-blocks and differential TIA is also briefly discussed.

Results and discussion were discussed in Chapter 5. The simulation results of sub-blocks used in differential TIA is analyzed based on pre and post simulation. The comparison between IBM and Silterra process is also presented on the performance over Process, Voltage and Temperature (PVT) variation.

In Chapter 6, the thesis is summarized and the future work are discussed to further improve on Receiver (Rx) design.

CHAPTER 2

LITERATURE REVIEW

In this chapter, a brief discussion on the optical transceiver system consists of a Transmitter (Tx) and Rx is presented. Further explanation will be focused on the optical receiver system inline with the project objective. The design requirement of a optical Rx system is explained briefly with referenced to the formulas. At the end of chapter, the topologies of different type of TIA's are discussed that is analyzed for the actual architecture selection.

2.1 Overview of Optical Transceiver System

The optical transceiver system is made of two main blocks consists of Tx and Rx. Figure 2.1 exhibits a block diagram of a modern optical link system. The optical system uses the Non-Return Zero (NRZ) data pattern for the signal transmission. In general the Tx function is to convert the electrical signal to optical signal, whereby the receiver on the other hand re-convert the optical signal back to electrical signal. Depicted in Figure 2.1, the data provided to the transmitter are in low speeds in many channels. A Multiplexer (MUX) converts the parallel data streams to a serial high data rate bit stream. This data streams multiplexing is done together with the Clock Multiplying Unit (CMU) which generates the high frequency clock signal. Next the serial data bit stream is driven by a Laser Driver which steers the large amount of

current to the Vertical Cavity Surface Emitting Lasers (VCSEL) laser diode in order to convert electrical signal to optical signal at end of Tx. At the Rx system, the optical signal is converted to an electric current signal by a device called photodiode. Next the current signal is translated to a voltage signal by TIA and amplified further by Limiting Amplifier (LA). A Clock and Data Recoverey (CDR) circuit is added in between LA and Demultiplexer (DEMUX). The purpose of the CDR is to extract the clock signal from the data stream and re-time the data to the new synchronized clock signal. At the end of Rx, the re-timed high data rate signal is divided in parallel sequences of lower data rate signal by the DEMUX. Next explanation is focused on optical receiver system.

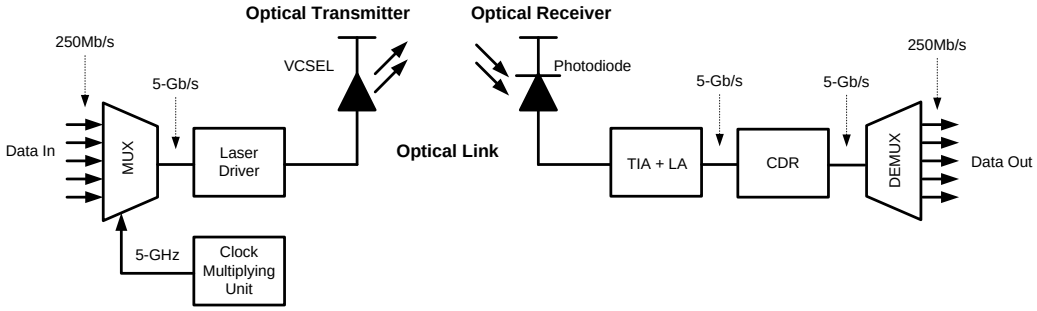

Figure 2.1: Optical Transceiver System

2.2 Optical Receiver Analog Front-End

The analog front-end of optical Rx are consists of photodiode, TIA and LA. As discussed in 2.1, the photodiode device converts the optical power into an electrical current signal. The type of photodiodes and its characteristics will be discussed in the following subsequent topic. Next, the TIA amplifies the electrical current signal to a voltage signal. Generally the converted current signal's amplitude is small, thus the TIA's gain need to be designed large and at the same time the input-referred noise to

be small. As the data in the Rx need to go through the CDR block for clock synchronization, an additional gain stages are needed to further amplify the TIA output voltage signal. The voltage signal amplification is further performed by a circuit referred to LA. It amplify the small input voltage signal in the range of 5-mV peak to peak to a large voltage swing that saturated at power supply rail, thus provides the fixed output signal for a wide dynamic range input current. In some application, where the TIA to tolerate with a long distance signal transmission, the Automatic Gain Control (AGC) circuit is employed in the Rx design to control on the output TIA signal, thus the signal will not be distorted which directly have the impact on eye-diagram. It is known that the optical Rx front-end is a single ended system, thus the conversion to a differential signal is done along the TIA design for better Common-Mode Rejection Ratio (CMRR). The DC offset cancelation circuit is another important block to be integrated with TIA design when it comes to differential design. The next topic will focus the background studies on photodiodes and TIA topologies as in line with the project objectives. Figure 2.2 shows the block diagram of the optical receiver system as discussed by (Sackinger, 2005).

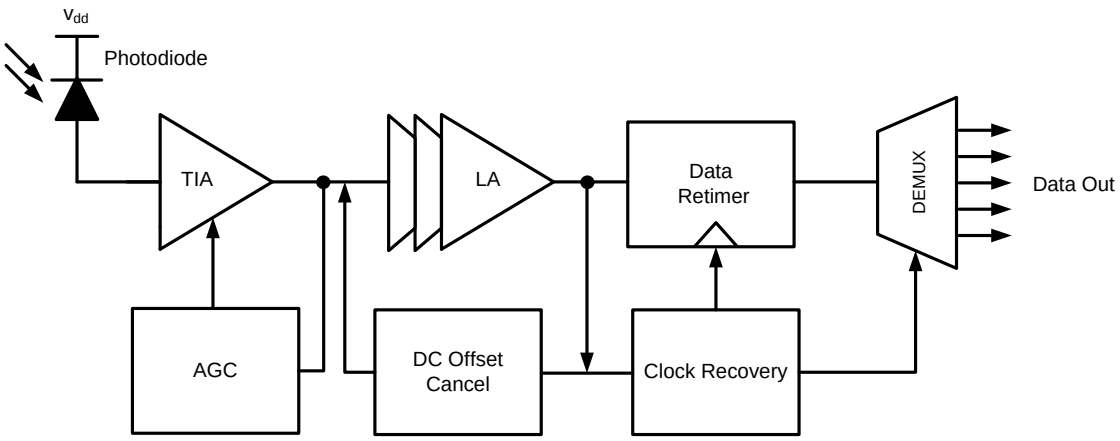

Figure 2.2: Block Diagram of Optical Receiver System

2.3 Photodiodes

Photodiode is a semiconductor device in the optical Rx system that converts optical signal to an electrical signal. Among the factors that are considered in the design of photodiode are noise, power, cost and sensitivity. The performance of a photodiode can be characterized by various figures of merit. These includes responsivity of the detector, it's bandwidth and noise factor which is generated by the photodiode itself. Table 2.1 below shows the 3 main parameters that affect the performance of a photodiode which directly determines the Rx optical sensitivity.

Table 2.1: Photodiode Parameters

Parameter	**Unit**
Bandwidth	Hz
Responsivity	A/W
Noise	μA-rms

2.3.1 Responsivity

Responsivity is the measurement of the light to current conversion efficiency of a photodiode. Generally a high photodiode responsivity improves the Signal to Noise Ratio (SNR) of a Rx system. The responsivity of a photodiode, R is defined as

$$R = \frac{I_{PD}}{P_{in}}. \tag{2.1}$$

where I_{PD} is the photocurrent, P_{in} is the received optical power. The unit for R is given as A/W. For a given photodiode responsivity, the sensitivity of the input optical power

of the receiver can be calculated based on the minimum detectable input current to the TIA. The typical responsivity of a photodiode for high data rate application is in the range of 0.5-A/W to 1.0-A/W as discussed by (Sackinger, 2005).

2.3.2 Bandwidth

Bandwidth of a photodiode is defined as the frequency of which the responsivity of a photodiode dropped by -3-dB from its low frequency value. The bandwidth is mainly limited by carrier transit time, *RC* time constant (Bass, 2010). Carrier transit time is the time taken by photogenerated carriers to travel across the high-field region. The *RC* time constant is determined by the equivalent circuit parameters of the photodiode and the load circuit. The diode series resistance, load impedance and parasitic capacitance of the p and n junction contribute to the *RC* time constant. A simple equivalent circuit of p-n photodiode is given in Figure 2.3. If the parasitic capacitance, C_p and series resistance, R_s are negligible, the photodiode bandwidth is given by

$$f_{RC} = \frac{1}{2\pi R_L C_{pd}}. \tag{2.2}$$

where R_L is the load resistance, C_{pd} is the photodiode capacitance. For discrete photodiodes, the value R_L is assumed to be 50-Ω to match the Radio Frequency (RF) test instruments of having the input impedance of 50-Ω.

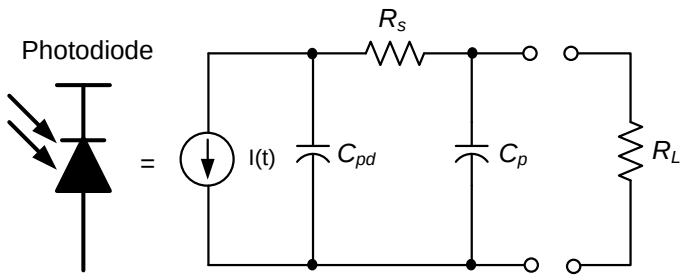

Figure 2.3: Simple *RC* Photodiode model

2.3.3 Noise

Noise is another important factor that degrades the performance of a photodiode on the converted light to current signal. The photodiode produces the current signal together with self generated noise. Shot noise and thermal noise are two dominant sources of noise in high-speed photodiode. Shot noise current is the result of the photocurrent being composed of a large number of short pulses that are distributed randomly in time. Each pulse corresponds to an electron hole pair created by photon. The formula is given below as discussed by (Sackinger and Fischer, 2000).

$$\overline{i_n^2} = 2qI_{DC}BW_n. \tag{2.3}$$

where, q is the electron charge, I_{DC} the signal current and BW_n is the bandwidth in which the noise current is measured. It is observed that the shot noise is dependent directly to the input signal current decided by the received optical input power. Besides the shot noise and thermal noise, the photodiode also produces dark current. The dark current is generated by a photodiode during the periods where it is not actively being exposed to light. The dark current produced depends on the depletion region, temperature and is due to random generation of electrons and holes from the electric field applied across diode junction. The addition of dark current and shot noise impact

the received signal at the Rx input but for high data rate signal, it is less significant as stated by (Sackinger, 2005).

2.4 Overview of Transimpedance Amplifier

TIA converts the input current signal to a output voltage signal in the optical Rx system. As the input current is transformed from the light wave by the photodiode device, the current signal could range from a very small to a large amplitude with the noise added in. As such, before implementing TIA, a number of factors need to be taken into consideration, namely the transimpedance gain, bandwidth, input-referred noise and power consumption (Li, 2007). To address the mentioned factors in solving the TIA's design issue, a simple circuit as in Figure 2.4 below is analyzed.

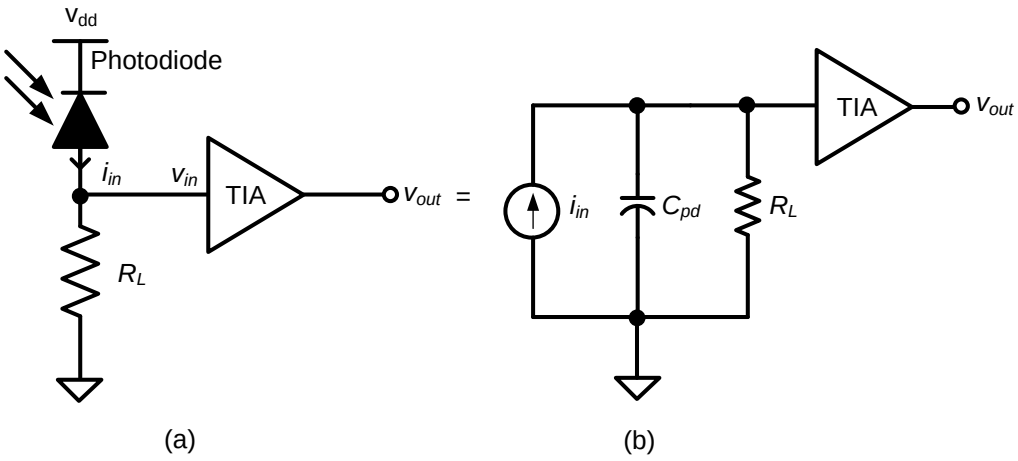

Figure 2.4: (a) Basic Optical Receiver and (b) Small Signal Model of TIA

2.4.1 Transimpedance Gain

The transimpedance gain, Z_T is defined as the ratio of output voltage to the input current.

$$Z_T = \frac{\Delta v_{out}}{\Delta i_{in}}. \tag{2.4}$$

The unit of transimpedance gain is defined in Ω or dBΩ. The Ω unit is the direct division of TIA's output voltage to the input current. For example, if the output voltage is 10-mV and the input current is 10-μA, then the gain is 1000-Ω. When the unit is translated into dBΩ, it will be $20 \times log \times 1000$ = 60-dBΩ.

2.4.2 Bandwidth

The bandwidth of TIA refers to the frequency at which the transimpedance gain of the amplifier drops by -3-dB below its passband plot. The TIA bandwidth is typically chosen to be equal to 0.7 times of the bit rate to overcome the issue of Intersymbol Interference (ISI) and noise as discussed by (Razavi, 2003) and (Sackinger, 2005). However, the wide bandwidth TIA reduces optical Rx sensitivity. From Figure 2.4, the -3-dB bandwidth of the simple TIA is given by

$$f_{-3dB} = \frac{1}{2\pi R_L C_{pd}}. \tag{2.5}$$

where R_L is the load resistance and C_{pd} is the photodiode capacitance. This shows that the overall TIA bandwidth is limited by the C_{pd} and input impedance of TIA. Thus to operate TIA at higher data rate, the R_L need to be reduced and at the same time the optimum C_{pd} selection is proposed.

2.4.3 Input-Referred Noise Current

One of the most important parameter to consider in the TIA design is the input-referred noise current, $i_{n,in}$. A very small input-referred noise yields a high optical receiver sensitivity. The sensitivity of the Rx is determined at the minimum level of input power detection by a system at a given Bit-Error-Rate (BER), 10^{-12} as discussed by (Kim et al., 2001). The minimum accepted input power and the related sensitivity is described as

$$P_{in} = \frac{2SNR \times \sqrt{I_{n,total}^2}}{R}. \tag{2.6}$$

where P_{in} is the minimum input power, R is the photodiode sensitivity, SNR is the ratio of signal to noise and $\sqrt{I_{n,total}^2}$ is the total input-referred noise current of Rx. The total noise are contributed from photodiode, TIA and LA. The sensitivity of Rx in optical power can be described as below (Cheng, 2003)

$$Sensitivity = 10 \times log \times (\frac{P_{in}}{1mW}). \tag{2.7}$$

On the other hand, when the input noise current in root-mean square (rms) is known, the input sensitivity i_s^{pp} is also described in the amplitude current as (Sackinger, 2005)

$$i_s^{pp} = 2 \times Q \times I_{n,TIA}^{rms}. \tag{2.8}$$

where Q is the quality factor of desired BER and $I_{n,TIA}^{rms}$ is the input referred rms noise current. The equation gives the minimum peak to peak input current signal that will be

detectable by the TIA in the presence of noise. Figure 2.5(a) shows a noiseless TIA with an equivalent noise current source, $i_{n,in}$ at the input. This presents the actual noisy output signal that the TIA produced after amplifying the input signal and the noise current. The input-referred noise current spectrum, $i^2_{n,in}(f)$ is frequency dependent as shown in Figure 2.5(b). The overall noise of the TIA is measured from the low frequency at (1/f) and up to 2 times of the -3-dB bandwidth of the system which covers the large spectrum of the output noise.

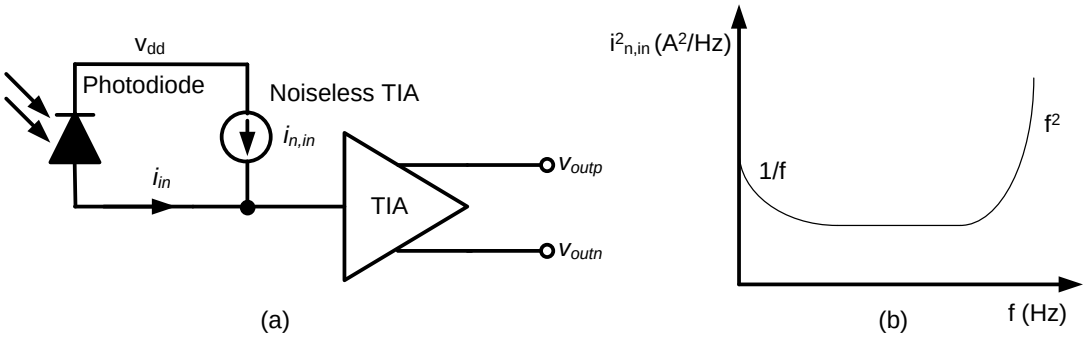

Figure 2.5: (a) Noiseless TIA model and (b) Input-referred noise current response

2.5 Transimpedance Amplifier Topologies

In this Section a few TIA topologies are identified and compared for the possible implementation in the proposed project. The TIA's that will be discussed are based on open loop and feedback configuration which are generally used in the optical Rx design depending on the data rate, sensitivity and power consumption. After discussing briefly the available topologies based on advantages and disadvantages with referred to design requirement, the architecture selection will be discussed in the next Section.

2.5.1 Common-Gate TIA

The conventional open loop TIA is called Common Gate (CG) TIA. The primary reason of having a CG TIA in optical Rx due to its low input impedance characteristics. Figure 2.6 shows the typical CG TIA architecture and its small signal model (Razavi, 2003). v_b is the bias voltage of M_1, i_b is the current source and R_D is the load resistor of the CG TIA circuit. In the small signal model, v_x is defined as the AC voltage source of the design in Figure 2.6.

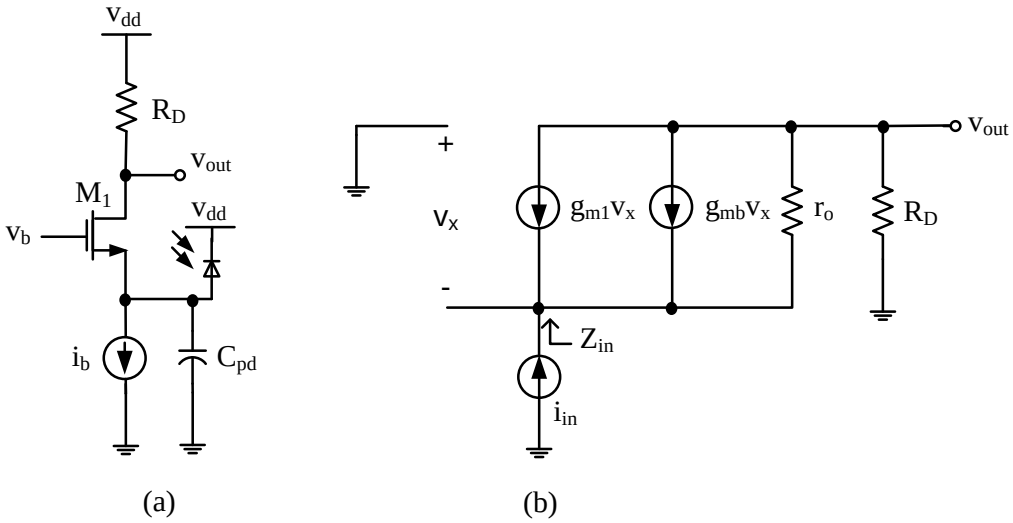

Figure 2.6: (a) CG TIA and (b) Small Signal Model

From the small signal model, the input impedance, Z_{in} of the circuit is equal to v_x/i_{in}, where i_{in} is the input current from photodiode, the current that flow through r_o is equal to (i_{in} + $g_{m1}v_x$+$g_{mb}v_x$) and by taking the Kirchhoff's Current Law (KCL) across the input node of CG TIA, the v_x voltage is set below

$$(i_{in} + (g_{m1} + g_{mb})v_x)r_o + i_{in}R_D = v_x, \tag{2.9}$$

the input impedance is derived below,

$$Z_{in} = \frac{v_x}{i_{in}}, \tag{2.10}$$

$$= \frac{r_o + R_D}{1 + g_{m1} r_o + g_{mb} r_o}, \tag{2.11}$$

with the assumption $g_{m1} r_o >> 1$, $r_o >> R_D$, $g_{m1} r_o >> g_{mb} r_o$, the input impedance is further simplified as follows

$$= \frac{1}{g_{m1} + g_{mb}}. \tag{2.12}$$

g_{m1} is the transconductance and g_{mb} is the bulk transconductance. The equation assures the r_o of M_1 is large. For long channel devices operating in saturation region, r_o tend to be large and thus above equation is valid with the Z_{in} is independent to R_D. Due to low input impedance obtained with this configuration, the -3-dB bandwidth of CG TIA is not dominated by C_{pd} to some extend, provided C_{pd} is in the smaller range compared to the output loading capacitance of CG TIA. For example, if the input C_{pd} is in the range of 0.2-pF to 0.5-pF, the input pole is still being the non-dominant pole, but when the input C_{pd} reaches up to 1-pF range which is about the same output capacitance loading, then the output pole is being the non-dominant pole, thus the -3-dB bandwidth is dominated by C_{pd} in this case. With the assumption of C_{pd} is smaller than CG TIA output capacitance loading, the overall bandwidth is now determined by R_D and output load capacitance, C_L of CG. The input pole is derived by (Razavi, 2003) as

$$f_{in} = \frac{C_{pd}}{g_{m1} + g_{mb}}, \tag{2.13}$$

and the output pole which set the -3-dB bandwidth of CG TIA is given by

$$f_{-3dB} = \frac{1}{2\pi R_D C_L}. \tag{2.14}$$

Eventhough CG TIA is benefiting the design by minimizing Z_{in}, the critical issue in the design is on noise factor. The total noise current generated by R_D and device transistor M_1 contributed to the input referred noise. Figure 2.7 below shows the CG circuit and equivalent noise sources. (Razavi, 2003)

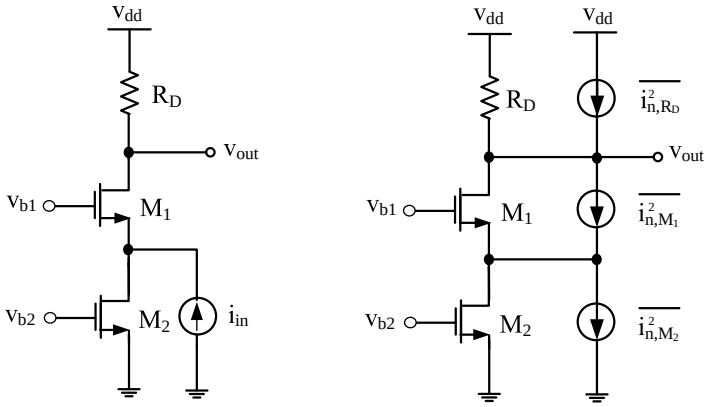

Figure 2.7: (a) CG TIA and (b) Noise analysis

From Figure 2.7, the output noise voltage contributed by the circuit can be derived as follows from (Razavi, 2003),

$$\overline{v_{n,out}^2} = (\overline{i_{n,M_2}^2} + \overline{i_{n,R_D}^2})R_D^2, \tag{2.15}$$

$$= 4kT(\gamma g_{m2} + \frac{1}{R_D})R_D^2. \tag{2.16}$$

where T is the resistor temperature in Kelvin, k is the Boltzmann's constant $(1.38 \times 10^{-23} J/K)$, γ is the coefficient of channel thermal noise, i_{n,M_2} and i_{n,R_D} are the noise sources of M_2 and R_D, g_{m2} is the transconductance of M_2. Both M_1 and M_2 gates are biased through v_{b1} and v_{b2}. The equation assumed that the noise source is statistically independent. To calculate the input-referred noise current, the output referred-noise voltage, $\overline{v_{n,out}^2}$ is divided by the overall CG TIA gain as follows

$$\overline{i_{n,in}^2} = 4kT(\gamma g_{m2} + \frac{1}{R_D}), \tag{2.17}$$

$$= \overline{i_{n,M_2}^2} + \overline{i_{n,R_D}^2}. \tag{2.18}$$

By looking the equation for $\overline{i_{n,in}^2}$, it can be explained that the noise contribution from M_2 and R_D are the trade-off between each other. Noise contribution from R_D can be minimized by maximizing R_D but this will have the limitation on output DC current setting for wide signal swing. On the other hand, the noise contribution from M_2 can be improved by minimizing g_{m2}. To keep M_2 in saturation region, the drain-source voltage need to be large for smaller input noise. The only way to keep both the Direct-Current (DC) and R_D high is by increasing the power supply voltage, but this will have impact on additional power consumption. Thus to optimize the noise of CG, R_D and g_{m2} need to be tuned accordingly.

2.5.2 Shunt-Shunt Feedback TIA

Other than CG topologies used in TIA design to minimize Z_{in}, a feedback configuration TIA are also implemented. The feedback TIA senses the voltage at the output node and returns a proportional current to the input. This configuration lowers the Z_{in} which directly making the input pole pushed to higher frequency. Thus the overall bandwidth is only decided by the pole at the output node. It is also known that feedback TIA have a wide input dynamic range capability to operate the Rx in a various input current range. A most common conventional feedback TIA is called Shunt-Shunt feedback. Figure 2.8 shows the schematic of shunt-shunt feedback TIA with a Common Source (CS) gain stage as discussed by (Razavi, 2003). The basic function of the CS stage in term of gain, input and output impedance are discussed by (Razavi, 2001).

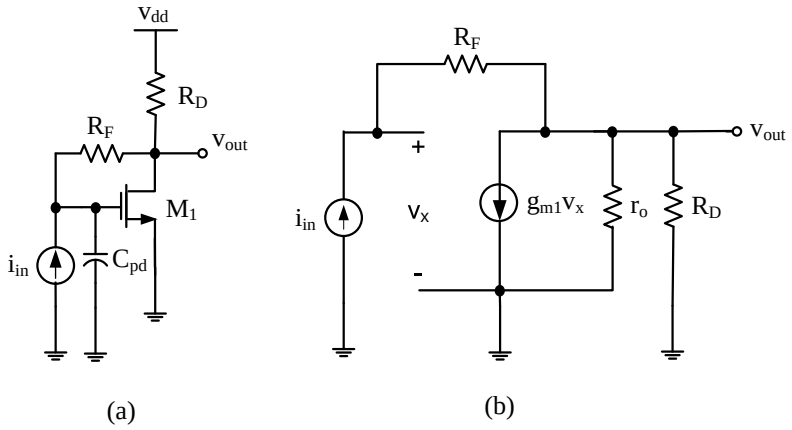

Figure 2.8: (a) Shunt Feedback and (b) Small signal analysis

In this configuration, a feedback resistor, R_F is connected between the output and input nodes of CS stage. v_x is the biasing voltage for M_1. From the small signal model in Figure 2.8, $v_x = i_{in}R_F + v_{out}$ and $g_{m1}(i_{in}R_F + v_{out}) + v_{out}/R_D = i_{in}$, thus the gain of shunt-shunt feedback design is given by (Razavi, 2001)

$$\frac{v_{out}}{i_{in}} = -\frac{g_{m1}R_F - 1}{g_{m1}R_D + 1}R_D, \tag{2.19}$$

with the assumption $g_{m1}R_F, g_{m1}R_D \geqslant 1$, the gain of shunt feedback design is summarized as

$$\frac{v_{out}}{i_{in}} = -R_F. \tag{2.20}$$

The input impedance of the feedback TIA is given by

$$Z_{in} = \frac{v_x}{i_{in}}, \tag{2.21}$$

$$= R_F - \frac{g_{m1}R_F - 1}{g_{m1}R_D + 1}R_D, \tag{2.22}$$

$$= \frac{R_F + R_D}{g_{m1}R_D + 1}. \tag{2.23}$$

As Z_{in} of shunt feedback design is derived, the -3-dB bandwidth is summarized as follows

$$f_{-3dB} = \frac{A}{2\pi R_F C_{pd}}, \tag{2.24}$$

in which the overall bandwidth is improved by adding the gain stage, A which is derived as $g_{m1}R_D$. On the other hand, the input noise current of this stage are summarized

below (Razavi, 2003)

$$\overline{i_{n,in}^2} = \frac{4kT}{R_F} + \frac{\overline{v_{n,A}^2}}{R_D^2}. \tag{2.25}$$

$v_{n,A}^2$ is the noise source of the gain stage A. It is observed that the noise of R_F is directly referred to the input, thus the overall noise is minimized by increasing R_F, but at the same time the increase in R_F degrades the -3-dB bandwidth. Thus the trade-off is between the noise and bandwidth for the shunt feedback design.

Other topologies that is used as a feedback TIA is a CMOS inverter gain stage. In this topology, a P-type Oxide Semiconductor (PMOS) transistor is implemented instead of normal resistive load for a larger DC gain but at the same time, it suffers from large parasitics loading contributed by PMOS as well as Miller effect as stated by (Schrodinger et al., 2002). Figure 2.9 represent the CMOS feedback circuit.

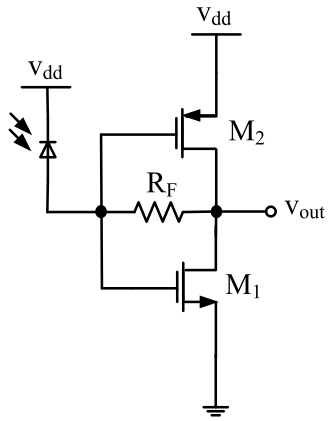

Figure 2.9: Inverter Feedback TIA

2.5.3 Regulated Cascode TIA

The CG TIA discussed in Subsection 2.5.1 are used typically in the optical Rx design due to its ability to isolate C_{pd}, thus the bandwidth is not determined by the input pole dominated by C_{pd}. However, to minimize the input-referred noise of the CG TIA, the g_m of the input transistor need to be set large which directly helps in lowering input impedance but the trade-off here is the increased in the DC bias current. At the same time, maximizing the size of input transistor also adds the total input capacitance, C_{in} which degrade the overall bandwidth. To address this issue, the RGC architecture is implemented as described by (Park and Yoo, 2004). The RGC design enhances its ability to isolate C_{pd} by lowering the input impedance with the large feedback loop factor. Figure 2.10 shows the RGC TIA circuit.

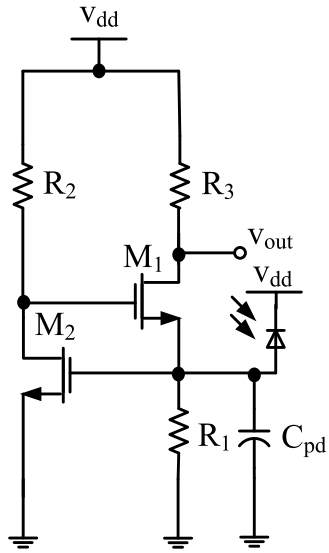

Figure 2.10: Regulated Cascode TIA

The RGC configuration consists of a CG transistor M_1 with a resistive load, R_3. R_1 resistor sets the DC bias current through the CG transistor. The local feedback loop is formed by the transistor M_2 and the resistor R_2 which reduces the input impedance

of the RGC design approximately the value of the voltage gain. From (Park and Yoo, 2004), the input impedance of the RGC circuit is simplified as

$$Z_{in} = \frac{1}{g_{m1}(1 + g_{m2}R_2)}, \tag{2.26}$$

where g_{m1} and g_{m2} are the transconductance of M_1 and M_2 respectively. With this approximation, the input impedance is $(1 + g_{m2}R_2)$ times smaller than CG design. Therefore the input pole of the RGC design is given by

$$f_{in} = \frac{1}{2\pi Z_{in}C_{pd}}, \tag{2.27}$$

and the output pole which sets the -3-dB bandwidth is further summarized as

$$f_{-3dB} = \frac{1}{2\pi R_3 C_L}. \tag{2.28}$$

On the other hand as discussed by (Park and Yoo, 2004), the RGC design introduced a zero in the transfer function of the system created by the local feedback loop, which causing a peaking in the frequency response that may contribute instability of the TIA system. Thus the thorough device optimization need to be done to overcome this issue.

Figure 2.11 shows the low frequency small signal model of the conventional RGC TIA. The input photodiode, device capacitances and bulk transconductance, g_{mb1} of M_1 are ignored in this small signal model for simplification. The nodal current analysis at node 1 gives