DESIGN AND IMPLEMENTATION OF LOW PASSBAND RIPPLE DIGITAL DOWN CONVERTER FILTER FOR SOFTWARE DEFINED RADIO TRANSCEIVER

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UNIVERSITI SAINS MALAYSIA
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DESIGN AND IMPLEMENTATION OF LOW PASSBAND RIPPLE DIGITAL DOWN CONVERTER FILTER FOR SOFTWARE DEFINED RADIO TRANSCEIVER

By

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DEDICATION

To

My parents.....

My wife.....

My children: Alyaa, Ahmed, Sura, Anfal, Ban,Amjad, Al-ameen, Buraq and Bilal

For their love, patience and sacrifice during my study.

MAJID

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I would like to express my heart-felt to my parents in memory and my family for their support along my study. Without their sacrifices, I would not have the chance to come so far. There is no word that can describe my appreciation to my wife for her willing to help, support and encouragement. I am very grateful to my brother, “Hadi”, Nephew “Firas Aziz” and all friends for their support along the duration of more than three years. It is very meaningful to my life.

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LIST OF ABBREVIATIONS

ADC	Analogue-to-Digital Converter
A/D	Analogue- to – Digital
ASICs	Application Specific Integrated Circuits
AWGN	Additive White Gaussian Noise
BER	Bit Error Rate
CIC	Cascaded Integrator Comb
CFIR	Compensating Finite Impulse Response
CDMA	Code Division Multiple Access
DAC	Digital-to-Analogue Converter
dB	Decibel
DUC	Digital Up – Converter
D/A	Digital – to – Analogue
DSP	Digital Signal Processing
DDC	Digital -Down Converter
DRC	Design Rule Check
EDK	Embedded Development Kit
EDIF	Electronic Design Interface File
FPGA	Field Programmable Gate Array
FIR	Finite Impulse Response
Fs	Sampling frequency
Fs,y	Output Sampling Frequency
Fs,x	Input Sampling Frequency
GC	Gray Chip
GSM	Global System for Mobile Communications

GQBPS	Generalized Quadrature Band Pass Sampling
GPPs	General Purpose Processors
GPRS	General Packet Radio Service
GUI	Graphical User Interface
HDL	Hardware Description Language
IFIR	Interpolated Finite Impulse Response
IC	Integrated Circuits
I / Q	In-phase and quadrature
ISR	Ideal Software Radios
IF	Intermediate Frequency
ISE	Integrated Software Environment
IP	Intellectual Property
IS	Interim Standards
LAN	Local Area Network
LUT	Look Up Table
LVDS	Low Voltage Differential Signal
MAC FIR	Multiply-Accumulate Finite Impulse Response
MIT	Massachusetts Institute of Technology
NAND	Not And
NOR	Not Or
NCO	Numerically Controlled Oscillator
NGD	Native Generic Database
NCD	Native Circuit Description
OSE	Operational Spectrum Effectiveness
PFIR	Programmable Finite Impulse Response

PA	Power Amplifier
PAR	Place And Route
QAM	Quadrature Amplitude Modulation
RF	Radio Frequency
RNS	Residue Number System
RRC	Root Raised Cosine
RTL	Register-Transfer Level
SDR	Software Defined Radio
SOPOT	Sum-Of-Power-Of- Two
SRC	Simple-Rate Converter
SRR	Software radio receiver
SAR	Software Assisted Radio
S/N	Signal-to-Noise Ratio
SPI	Serial Programming Interface
TP	Tile Processor
TSR	True Software Radio
UMTA	Universal Mobile Telecommunication System
USR	Ultimate Software Radios
UCF	User Constraints File
VIF	Verification Interface Format
VLSI	Very-Large-Scale Integration
VHDL	Very high speed Hardware Description Language
WLAN	Wireless Local Area Network
WCDMA	Wide band -Code Division Multiple Access
WIMAX	Worldwide Interoperability for Microwave Access

XST	Xilinx Synthesis Technology
3G	Third Generations
4G	Four Generation

LIST OF SYMBOLS

A_S	Stop band attenuations
$A_d\ (\omega)$	Desired amplitude
A_p	Passband attenuation
$A(\omega)$	Actual amplitude response
B	Bandwidth of baseband Signal
b[k]	Filter coefficients
$C(f)$	Channel Frequency Response Characteristic
D_c	Dynamic Range of Converter
$E(\omega\ )$	Error function
$F(\omega)$	Frequency response of the filter
f_{BB}	Baseband Frequency
f_c	Carrier Frequency(centre frequency)
f_{IF}	Intermediate Frequency
f_{new}	Sample Rate after Sampling Rate Conversion Process
f_{old}	Sample Rate before Sampling Rate Conversion Process
f_{pass}	Pass Band Frequency of Pulse Shaping Filter
f_s	Sampling Frequency
f_{stop}	Stop Band frequency of Pulse Shaping Filter
$I(n)$	In-Phase Channel
M	Amplitude Loss Factor
m	Arbitrary number of replications
N	Order of desired filter

$Q(n)$	Quadrature Phase Channel
$W(\omega)$	Weight function
ω_p	Passband-edge digital frequency
ω_s	Stopband-edge digital frequency
δp	Passband allowed deviation
δs	Stopband allowed deviation
ε	Maximum error
ω	Operating frequency range of the filter
β	Roll off Factor
$x(n)$	Input Signal
M_{sec}	Number of multiplication per second
R	Rate change factor
g[k]	Filter coefficients

REKABENTUK DAN PELAKSANAAN
PENAPIS PENUKAR TURUN DIGITAL DENGAN RIAK JALUR-LULUS YANG RENDAH UNTUK KEGUNAAN RADIO TERTAKRIF PERISIAN

ABSTRAK

Tujuan utama kajian ini ialah rekabentuk dan pelaksanaan algoritma penuras penukar turun digital (DDC) dengan riak jalur-lulus rendah dan atenuasi tinggi dalam penolakan bersebelahan dan keperluan penyekat dalam sambutan penuras bagi penghantar-terima radio tertakrif perisian (SDR) untuk menurunkan penggunaan kuasa dan mengelakkan ganggan dalam saluran. Algoritma yang dicadangkan menggabungkan algoritma Remez dengan algoritma Mini-max untuk mengurangkan kadar ralat dalam sambutan penuras. Penuras DDC ialah kombinasi penuras sikat bersepadu kaskad (CIC) berperingkat 5 dengan 2 penuras FIR sama-riak (CFIR dan PFIR) berfasa linear. Riak jalur-lulus, penolakan bersebelahan dan keperluan penyekat dibangunkan dengan mengawal lebar peralihan, tertib penuras dan fungsi permberat penuras FIR dengan menggunakan perisian MATLAB dan Xilinx System Generator. Di samping itu, bahagian jalur-dasar dalam penghantar dan penerima bagi penghantar-terima SDR telah direkabentuk dan dilaksanakan di bawah hingar saluran untuk mengesahkan prestasi penuras dalam penerima SDR. Isyarat masukan dan isyarat keluaran dianalisa dengan menilai isyarat tersebut dalam masa nyata dan disahkan dengan menggunakan kod Verilog dalam pelaksanaan FPGA. Keputusan simulasi dan pelaksanaan penuras DDC menunjukkan bahawa algoritma yang dicadangkan memberi pembangunan penting iaitu 40% dalam riak jalur-lulus, 18% dalam penolakan bersebelahan dan 11% dalam keperluan penyekat, dan mengguna hampir 20% hirisan dan LUT kurang daripada rekabentuk yang sedia ada. Maka, keputusan tersebut mengesahkan kesahihan algoritma yang dicadangkan, dan teknik yang digunakan menyokong keperluan GSM bagi sistem komunikasi tanpa wayar.

DESIGN AND IMPLEMENTATION OF LOW PASSBAND RIPPLE DIGITAL DOWN CONVERTER FILTER FOR SOFTWARE DEFINED RADIO TRANSCEIVER

ABSTRACT

The main aim of this research is the design and implementation of the Digital Down Converter (DDC) filter with low passband ripple and high attenuation in the adjacent rejection and blocker requirements in the filter response for Software Defined Radio (SDR) transceiver to decrease the power consumption and avoid the interference in the channel. The proposed DDC filters incorporate of Remez algorithm and Mini-max algorithm to reduce the error rate in the filter response. The DDC filter is a combination of 5-stages Cascaded Integrated Comb (CIC) filter and two linear phase Equiripple FIR filter (CFIR and PFIR). The passband ripple, adjacent rejection and blocker band is developed by controlling the transition width, filter order and weight function of the FIR filter using MATLAB and Xilinx System Generator environment. Additionally, the transmitter and receiver baseband section of SDR transceiver has been designed and implemented under channel noise to verify the filter performance in the SDR receiver. The input and output signals are analyzed and evaluated on a real time basis by translating all signals in Verilog code and verified using ModelSim for the FPGA implementation. The simulation and implementation results of DDC filter show that the proposed algorithms provide an important developments of 40% in the passband ripple, 18% in the adjacent rejection, 11% in the blocker requirements and consume less FPGA logic elements by almost 20 % in term of slices and LUTs as compared with current design. These results confirm the validity of the proposed algorithms and the techniques used are promising to support the SDR requirements of wireless communication system.

CHAPTER 1

INTRODUCTION

1.1 General Overview

The SDR is simply defined as “radio in which some or the entire physical layer functions are software defined” by the SDR Forum. This implies that the architecture is flexible such that SDR may be configured in real time to adapt itself to various wireless standards and waveforms, frequency bands, bandwidths, and modes of operation. A data rate conversion section is the most important process in the technology of Software Defined Radio (SDR). It is a measure of a sampling speed of the incoming signal into the SDR receiver. A high speed data rate conversion can be achieved by designing a Digital Down Converter (DDC) with a compact multi-stages filter in a single block. One of the novel designs in obtaining a high efficiency of DDC filter has been proposed by (Eugene, 1981), for decimation and interpolation using Cascaded Integrator Comb (CIC) filter approach. That filter was designed from a combination of few integrator elements and comb structure. A lot of method has been established to investigate deeper into the idea. This was forced by the fast acceleration progress of the modern mobile cellular phone (Giannini, 2008).

The first idea of Software Defined Radio technology was introduced by Mitola, (1995). That device was recognized as a radio that could process multi-stages signal form subsystem as illustrated in Figure 1.1. Mitola accustomed in the area of signal processing and has work for that subject very well since 1991. Steinbrech was further investigated deeper into the idea then come out to enhance the system. He has shared the idea regarding the SDR in the first European conference on Software Radio in May 1997. The modern technologies can be designed from numerous

choices of the algorithms under the software defined radio technology using MATLAB programs.

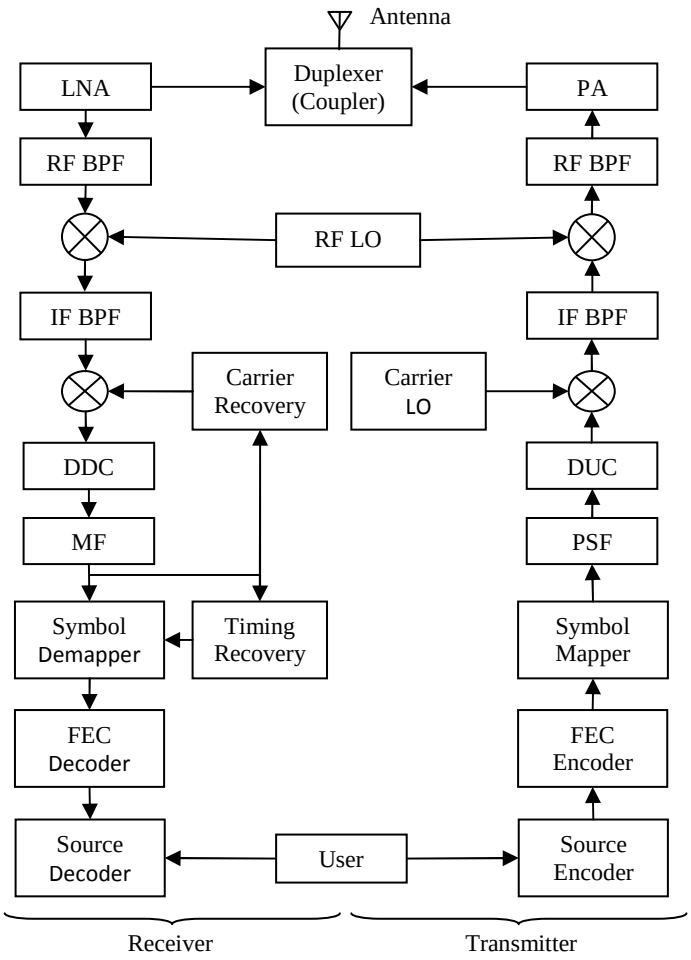

Figure 1-1 Software Defined Radio system (Mitola, 1995)

1.2 Motivation to the Research

The widespread of mobile communication devices requires more efficient system in signal processing in terms of size and energy saving. The energy consumption in a communication system depends on the technology of the processor and the number of processing stages. Programmability in the decimation filter,

allows it to adapt to the different channel bandwidths, interferers requirements of the different standards, while maintained the power consumption at a minimum. The appearance of various standards in communication technologies in the world requires a good technique that able to provide a compatible standard replacing any part of the system by the software defined radio receiver technology (Gray and Meyer, 1995)

The multi-stages cascaded integrated comb presented by (Eugene, 1981), was to convert the high rate of signals to a lower rate after the A/D converter with high gain in the desired bands. After that, other researchers have added further stages to compensate the gain with drawback of high ripple in the pass-band. Digital down converter is one of a typical type of data rate converter that could be used to satisfy the Software defined radio applications.

1.3 Problem Statement

A lot of researches have been done in introducing an efficient digital down converter (DDC) filter for software defined radio receiver. All of them claimed that they have introduced novel techniques to improve the efficiency of DDC filter; however there were some limitations in the designs. For example, the method introduced by Douglas et al., (2008) and Shahana, et al. (2008) that will be elaborated more detail in Chapter 2. In brief the pass-band ripple of the filter is still high even they claimed that their methods can overcome the design introduced by the researchers before them. The method introduced by Tjerk et al., (2006), too many numbers of multiplier was used which make the computation time become longer due to the complicated structures hence more power consumption. A Digital down Converter (DDC) filter with pass-band ripple of -0.03 dB, adjacent rejection of -25

dB and blocker requirements of -105 dB has produced by Texas instruments, (2009). The adjacent rejection and blocker requirements in the DDC filter performance is other important parameters need to improve and enhance the filter capability to avoid the interference and prevent the effect of spectral replicas of undesired signals. The DDC decimation fitter require to design with full flexibility in terms of pass band ripple, adjacent band rejection and blocker requirements. This will be done by optimizing the FIR filter design based on software defined radio.

1.4 Research Objectives

The main goal of this thesis is to design a low pass-band ripple digital-down converter (DDC) filter for SDR transceiver. Align to the main goal; there will be few objectives to be achieved such as stated below:

1. To decrease the passband ripple of Digital Down Converter (DDC) filter less than 0.03dB peak to peak which introduced by Texas ins, (2009) by estimate a minimum length of the PFIR filter which provide minimum ripple using programme shown in Figure 4.7.

2. To increase the adjacent band rejection and blocker requirements of the Digital Down Converter (DDC) filter more than -25dB and -105dB respectively which introduced by Texas ins, (2009) using different weights at different stop band frequencies, and specify its locations accurately.

1.5 Scope of works

This project will focus on the designs of Digital Down Converter (DDC) filter for Software Defined Radio (SDR). The first design is to introduce a combination of CIC, CFIR, and PFIR filters for SDR receiver with low pass-band ripple. The design cover simulation, implementation and comparison between both results was examined in order to ensure that it meet the design objectives.

The second design is a Software Defined Radio (SDR) for wireless communication system to verify the DDC filter performance under channel noise affect. The design covers the simulation and implementation of transmitter and receiver parts of the wireless communication system. This model is capable to transmit and receive a 2.5 M symbol/s under 20 dB AWGN channel. Both the DDC filter and SDR transceivers were design and simulated with help of MATLAB (M-file and SIMULINK block set). The implementation of DDC filter and SDR model were done using System Generator, ISE software and FPGA Vertix-4.

1.6 Contribution of Thesis

The contribution of research is the design and developing a Digital Down Converter (DDC) filter for GSM system which provides sufficient evidence of idea and insight in the design of this filter. The main contributions of this thesis are as follows:

1. The development of overall pass band ripple in the Digital Down Converter (DDC) filter response by minimize the PFIR filter order that reduce the maximum absolute weighted error.

2. The improvement of adjacent band rejection and blocker band of the DDC filters by inserting different weight in different stopband frequency at 100 KHz and 108 kHz in the PFIR filter response.

1.7 Thesis Layout

Chapter 1: A necessary background, motivation, objectives and contributions of thesis are the major subjects of chapter one.

Chapter 2: A literature review of decimation filter and SDR initially exists, which includes the general environment in sequence of SDR and DDC filter. The related work of the Digital Down Converter (DDC) filter design and Software Defined Radio (SDR) is present in the second section of this Chapter.

Chapter 3: The fundamental of Sample Rate Conversion and multi stage filter design theory is the first section in this chapter. The error rate reduction theory and FIR filter design methods is the seconded section of this chapter while the optimization of FIR filter design and error rate correction is the third section. The FPGA implementation and timing constraints mythology is also present in this chapter. The 16-QAM modulation scheme is the final section of this chapter.

Chapter 4: The design and simulation of Digital Down Converter (DDC) filters using MATLAB M-file and SIMULINK block set is the first section in this chapter. The Software Defined Radio (SDR) model design and simulation in MATLAB is the second section of this chapter. The verification and implementation of these models using System Generator and ISE software is the third section of this chapter.

Chapter 5: The simulation results of Digital Down Converter (DDC) and SDR model are discussed, evaluated and compared in the first section of this chapter. The implementation results of DDC filter is compared with simulation results and examined in order to ensure that it meet the design objective in the second section of this chapter.

Chapter 6: Lastly, brief summary will highlight the contribution of the project including the novelty of the designs and the advantage of each model. However some of the investigations are still need to be further tuned deeper in order to come out with other conclusion. The expected areas to be suggested in the future work recommendation in order to open the science gate for other researchers to extend the finding.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

A digital down converter DDC filter is important part in SDR receiver. The power consumption and performance of DDC filter in the desired band will have an effect on the size of hardware and signal quality. The Digital Down Converter (DDC) filter is quite important in the communication device when the system need to connect with different standards. For example, if the GSM system needs to connect with Internet through WLAN, it may be helpful to use this type of converter designs using SDR technology to change the specifications of this filter by only changing the filter programming without affecting the complete hardware in this case (Tjerk et al., 2006).

2.2 Overview of SDR Wireless Communication System

A general structure of SDR contains a transmitter, channel and a receiver path in the wireless communication system as shown in Figure 2.1. This system is divided into three sections, RF, IF and baseband. In the IF section, the sample rate of the signal has convert from low rate to high rate within the transmitter by using so called digital up-converter (DUC) while from high to low rate in the receiver path by using digital down converter (DDC) (Pallavi, 2005).

Digital down Converter (DDC) in the receiver path is used to convert the intermediate frequency (IF) to the baseband for more processing and isolate the desired signal. The sampling rate conversion of the received signal has to be optimizing to protect this signal from interference and undesired signal as well as to

avoid any aliasing phenomena during sampling process. In addition, the power consumption by the sampling rate process is more important factor to satisfy the user requirements (Pallavi, 2005).

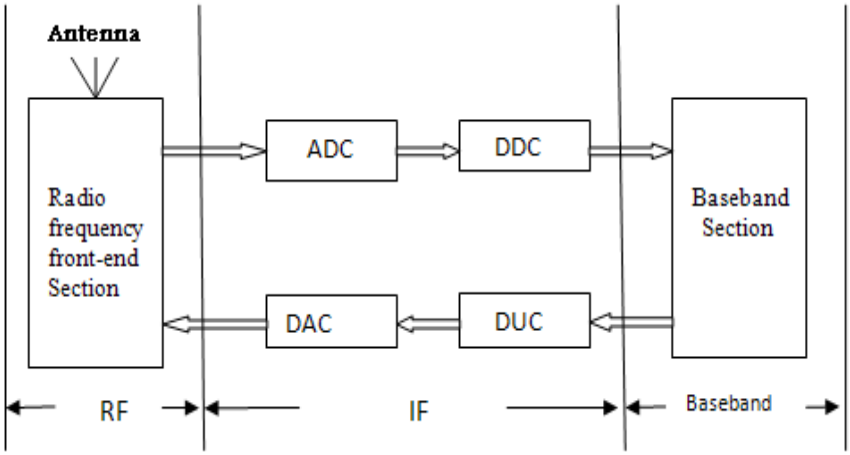

Figure 2-1. Practical structural of SDR system (Pallavi, 2005)

2.3 SDR Front-end Receiver Architectures

According to the application of SDR receivers, the RF front-end can be divided into three main architectures (Shi and Ismail, 2002), (Elwan et al., 2001). In the first architecture, as shown in Figure 2.2., the ADC is located at baseband. The signal traverses two down conversion stage with filter and is improved at RF by a LNA. The purpose is to shift the desired signal to the baseband. Such architecture is now adopted mainly in radio receivers. The benefit of this receiver architecture is obtained from the availability of low price narrowband RF and IF components with small power spending. Though, due to its narrowband future, it has the disadvantage that design of major components is made to an exact channel and is hard to increase the receiving band (i.e. digitalize the IF band processing give more flexibility to increase the frequency band and provide exact channel without distortion). So, for a

SDR advance, this architecture is not a good choice because of its narrow and fixed band design, the fact that the integration in a single Integrated Circuit (IC) chip is making it difficult due to the number of discrete components required. The different between Figure 2.1 and Figure 2.2 is the filtering process at IF band, digitalize or non-digitalize (Shi & Ismail, 2002)

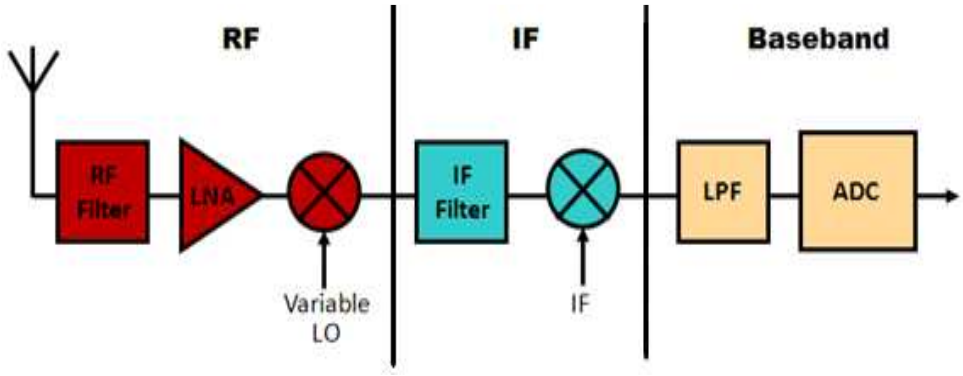

Figure 2-2. Simple super-heterodyne front-end architecture (Shi & Ismail, 2002)

The second architecture considers the ADC in the IF section, preceded by a RF filter, LNA and a mixing stage as shown in Figure 2.3. Compared with the previous architecture, this could be designed to operate over a wider bandwidth because of following the down conversion. The entire bandwidth can be filtered and digitized allowing digitally processing of same channel. Thus, one advantage is the possibility to receive more than one channel and then isolate each one using digital filtering. This architecture is an approximation of the ideal SDR receiver configuration. Furthermore, this architecture can be realizable with actual available components but without covering a high bandwidth of reception.

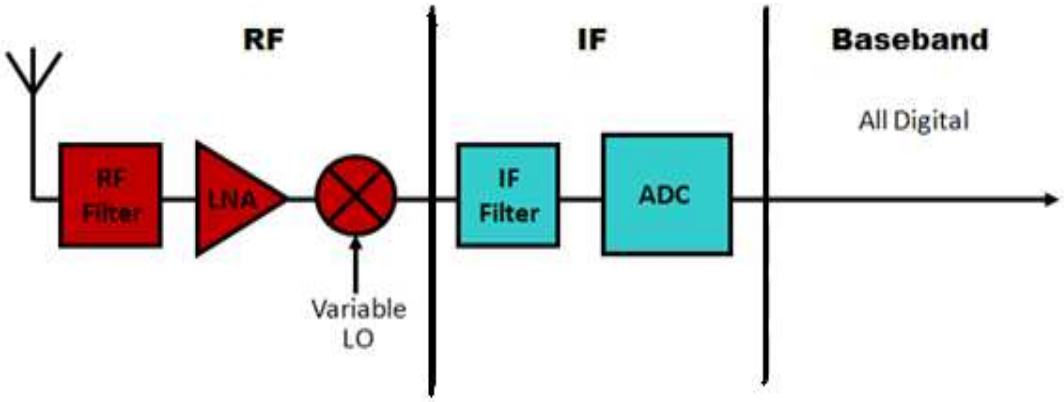

Figure 2-3. Single down conversion front-end architecture (Shi & Ismail, 2002)

Finally, the third architecture Figure 2.4., digitizes the signal at RF. This architecture corresponds to that envisioned by (Mitola, 1995) and is the most challenging for future approaches and the most appropriate for multi standard operation. Unfortunately, this architecture is not practical because ADC must fulfil unusual specifications, either a very high sampling rate to digitize a minimum frequency band in the order of GHz or the high dynamic range that will be required. Furthermore, other limits exist as the compulsory factor for ADC linearity over the entire frequency range and the power dissipation of such devices that would prevent their use in mobile applications (Shi and Ismail, 2002).

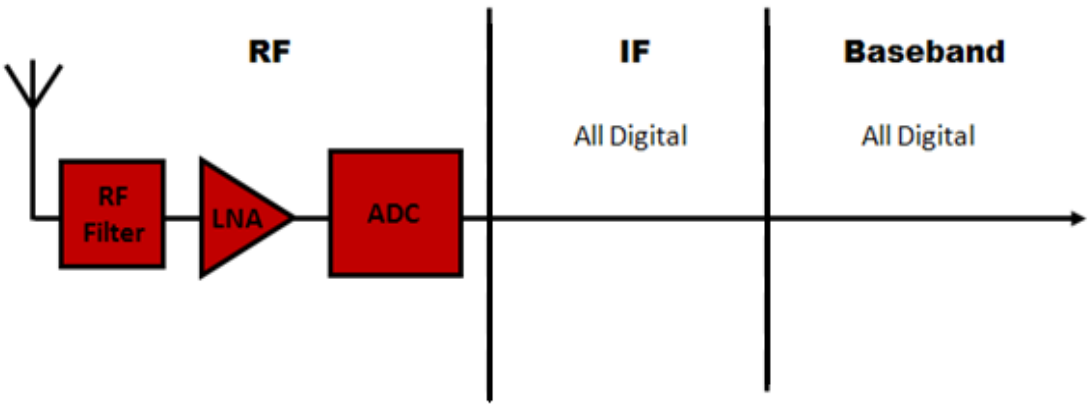

Figure 2-4. Direct digitization front-end architecture (Shi and Ismail, 2002)

2.4 SDR Receiver Architectures

SDR receiver architecture is mostly used the digital down converter to convert the intermediate frequency band to baseband. Figure 2.5.a shows the functional diagram of SDR receiver. After radio frequency mixing, the signal is changed to a digital signal via a high speed ADC, and then converted to baseband via DDC for more processing via DSP process. Figure 2.5.b illustrates the DDC filter stages. In order to get the baseband signals, the digital signal after ADC and Numerical Control Oscillator (NCO) is multiplied to generate the required signals. The distortion signal near the band of interest is moved by three stage DDC filters. The DDC filter contains Cascaded Integrated Com (CIC) filter to decimate the incoming signal, a Compensating Finite Impulse Response (CFIR) filter with decimation of 2 to compensate for the sharp attenuation caused by CIC filter and Programmable Finite Impulse Response (PFIR) filter with decimation by 2 to make further filtering and provide the mask frequency of the system. Since the high input information speed is 50-100 Msps, the Digital down converter implementation design need to be efficient to process this band of frequency in terms of power consumption and enhance the idea of SDR. Normally less multiplier filter implementation is desired for their rate and hardware competence. Digital down converter has to convert the received signals from high to low frequency by sufficient function and conditioning performance to reduce the error in the band of interest and power consumption (Douglas and Vinod, 2008).

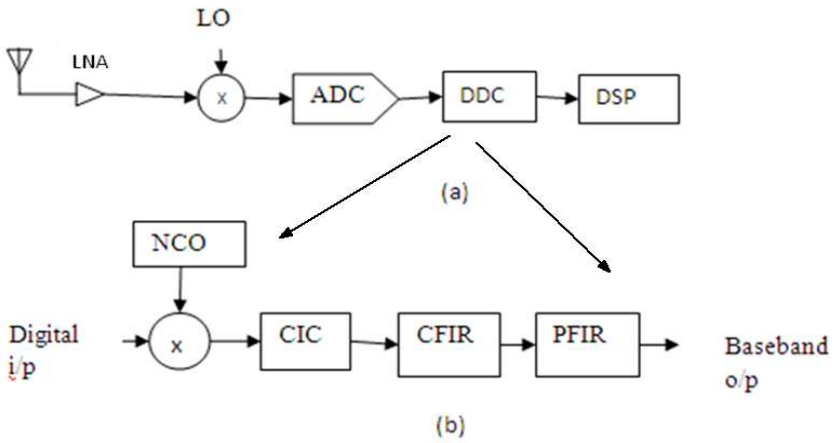

Figure 2-5. (a) SDR receiver, (b) DDC fundamental (Douglas &Vinod, 2008)

2.5 Related Work

Several designs and implementations of DDC filters for software defined radio shown in Figure 2.5 (b) are presented in recent research. The performance of SDR is greatly influenced by the DDC filter. Many researchers have attempted to improve the performance of DDC filter by addressing the following issues:

1. The power consumption of the filter to be minimum, while maintaining high efficiency.
2. Minimizing the pass band ripple to avoid the distortion within the received signal.
3. Compensating the adjacent band rejection and blocker requirement.

Most of the works to tackle the aforementioned problems were based on the Remez algorithm (Remez, 1975) and the “Weighted Chebyshev Approximation” or “Mini-max” algorithm (Chebysheve, 1934).

2.5.1 Multi Stage Sample Rate Converter

Multi stage Digital down converter structure for SDR receiver was designed by Tianqi and Cheng (2006) as illustrated in Figure 2.6.

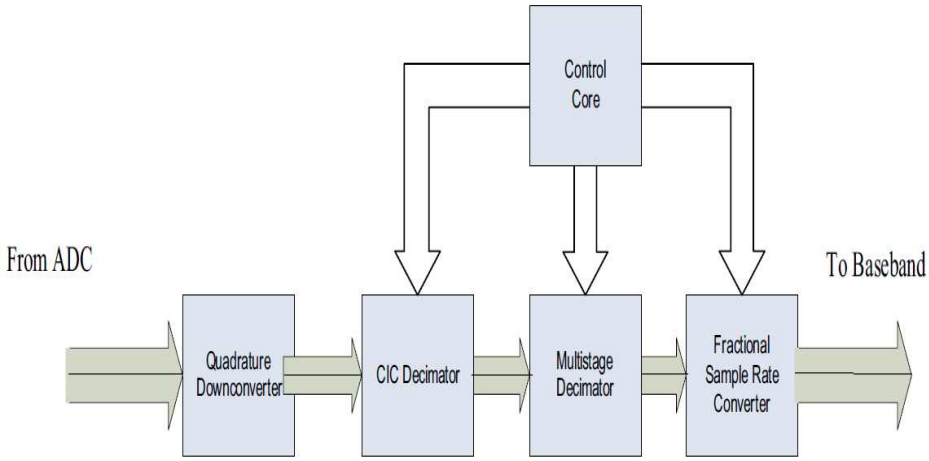

Figure 2-6 Sample rate converter architecture (Tianqi & Cheng, 2006)

In SDR technology, the most important process is the sampling change of the incoming signals after ADC filter. The designed DDC filter with high decimation and simple with specific arrangement of CIC filter as a first part, and three decimation stages from Nyquist half band filter and Equiripple half band filter are connected in last stage. The decimation section in the proposed filter is containing of three stages, serving as a factor-2 down sampler. The Nyquist filter has been used as anti aliasing filter in the first two stages and the linear phase Equiripple filter has been used in the last stage. By their design, they provide the SDR receiver sampling rate conversion Tianqi and Cheng (2006).

2.5.2 Fractional Decimation

Fractional decimation system was designed by Naina and Gordana (2007). The design of fractional decimation filter depending on the interpolated finite impulse response (IFIR) filter shows low complexity without multipliers which provide good quality applicant for SDR request. Additionally, the algorithms have been implemented in SPARTAN-3 of fixed point multiplication. The designer change a single step FIR filter by the lesser order multi-stage FIR filters as illustrated in Figure 2.7. The DDC filter has been implemented by generating the VHDL code in MATLAB programs by converting input signal and filter coefficients to the fixed point arithmetic (Naina & Gordana, 2007)

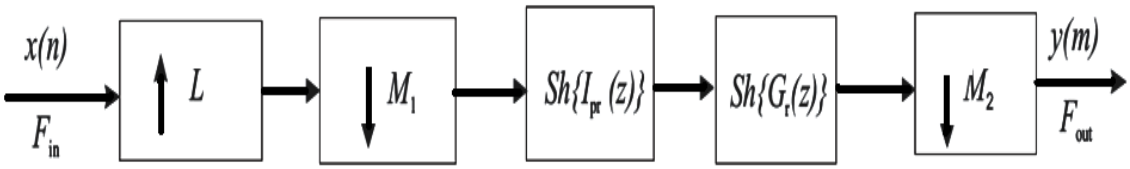

Figure 2-7 Fractional Decimation System (Naina & Gordana, 2007)

The algorithm implementation results show important FPGA equivalent gates utilization by about six times. Thus, the energy dissipated decreases, but the filter pass-band ripple is -0.05 dB, which will need more power in the implementation designs. The structure may be considered as the capable algorithm for the Software Radio applications due to its less complication in the given period of time. The ensuing output response of the this filter is illustrated in Figure 2.8 (Naina & Gordana, 2007).

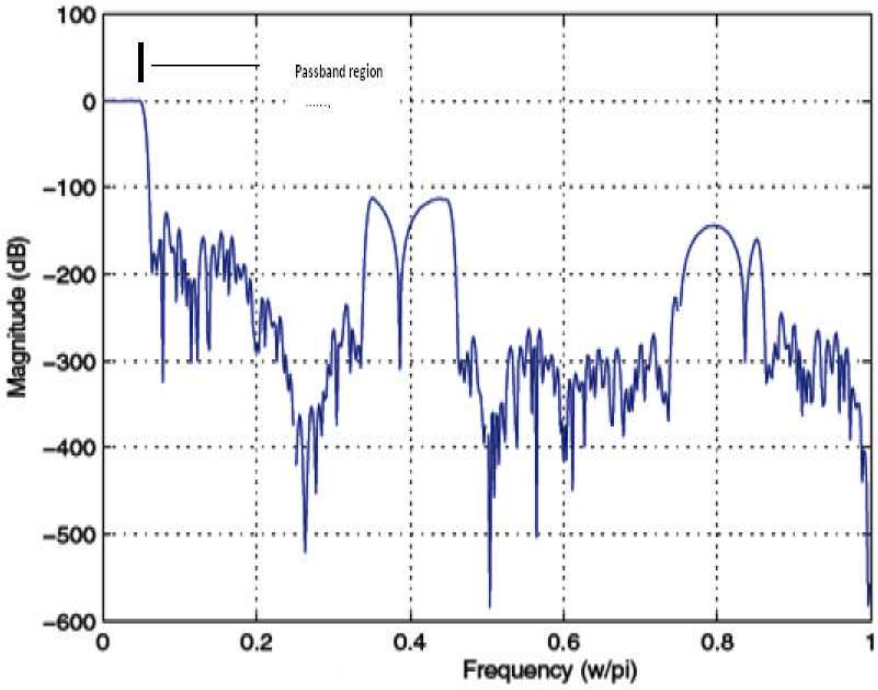

Figure 2-8 The resulting filter response (Naina & Gordana, 2007)

2.5.3 Optimal Architecture

An optimal architecture for a DDC was introduced by Tjerk et al. (2006). The filter consists of two CIC filter and FIR filter. The filter is implemented in five architectures which are two ASIC, GPP, FPGA, and Montium Tile Processor (TP).The power dissipated is evaluated in this design while performing the digital down converter algorithm and found that the ASIC is the most exceptional solution. In this design, they used two CIC filter as first stage and 125 –taps FIR filter in the last stage of DDC filter and this will increase the device utilization when implemented in FPGA. This will further increase the power consumption using the filter, which is calculated to be 115 mW for GSM channel. Hence this filter need to be more tuned in selecting the FIR filter design. The presented DDC algorithm is illustrated in Figure 2.9 (Tjerk et al., 2006)

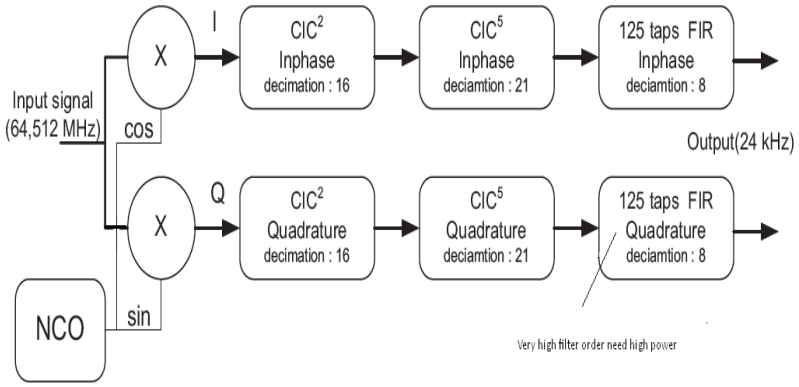

Figure 2-9 DDC algorithm by (Tjerk et al., 2006)

2.5.4 Multi Standard SDR Filter

Multiplier fewer channels filters for Multi-Standards SDR was designed by Douglas and Vinod, (2008). It is a method for decreasing the implementation complication of linear phase FIR digital filters by reducing the adder depth and the number of adders in the multiplier block. This was introduced to implement a multistage, multi-standards decimation filter. The results show that an important decrease in the hardware requirements occurred compared with other low delay multiplier implementations although the resultant response of DDC filter shows high pass-band ripple of about 0.1dB and critical adjacent band rejection as shown in Figures 2.10 and Figure 2.11 (Douglas & Vinod, 2008).

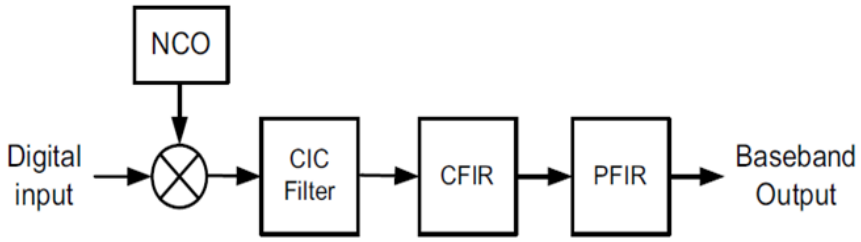

Figure 2-10 DDC design (Douglas & Vinod, 2008)

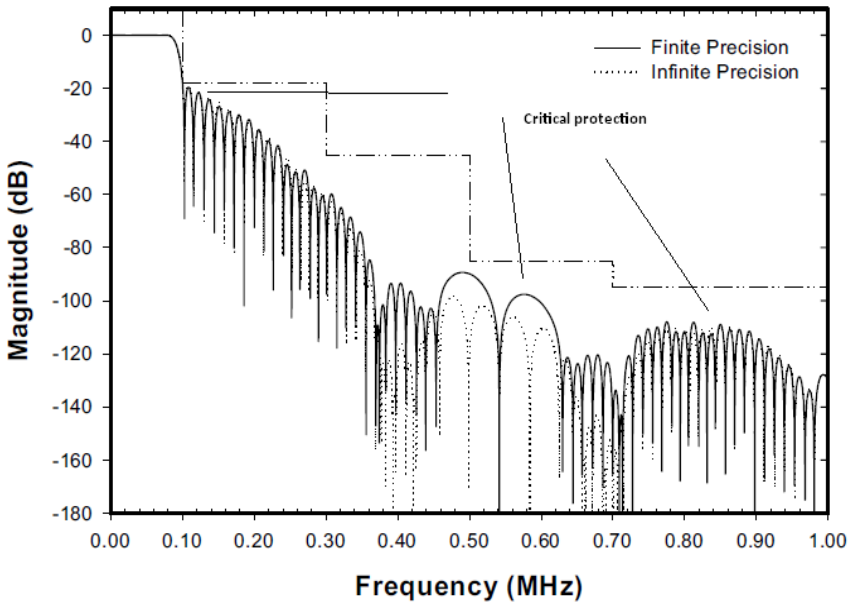

Figure 2-11 DDC Filter response (Douglas & Vinod, 2008)

2.5.5 Programmable Decimation Filter

Dual-Mode RNS based programmable Decimation Filter for WCDMA and WLAN was presented by Shahana et at., (2008). A dual-mode Residual Number System (RNS) based decimation filter may be able to programme for WCDMA and 802.11a standards. The Decimation process was done using multistage, multi rate finite impulse response (FIR) filters. The FIR implementation in RNS domain offers high speed since it takes open operation on smaller residues in parallel channels. The FIR filter also shows programmability to selected standard by reconfiguring the hardware architecture. The whole area is increased only by 33% to comprise WLAN compared with single mode WCDMA transceiver. In every mode, the unused parts of the overall architecture is powered down and bypassed to achieve power reduction. The filter structure of (Shahana, et at, 2008) is shown in the Figure 2.12

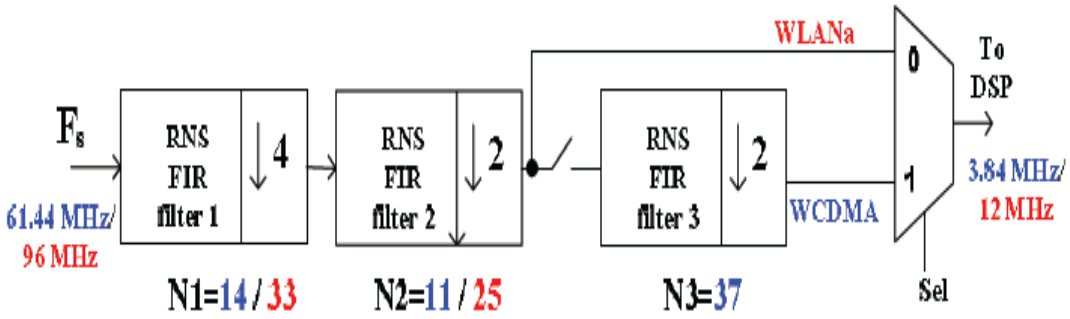

Figure 2-12 Programmable decimation filter (Shahana et al., 2008)

The received signal may be distorted by this filter because of the high pass-band ripple of proposed filter which is about -0.5dB and the stop-band attenuation which is about -44dB. In addition, the designed filter gives high input gain of about -44dB. The response of DDC filter is shown in Figures 2.13.

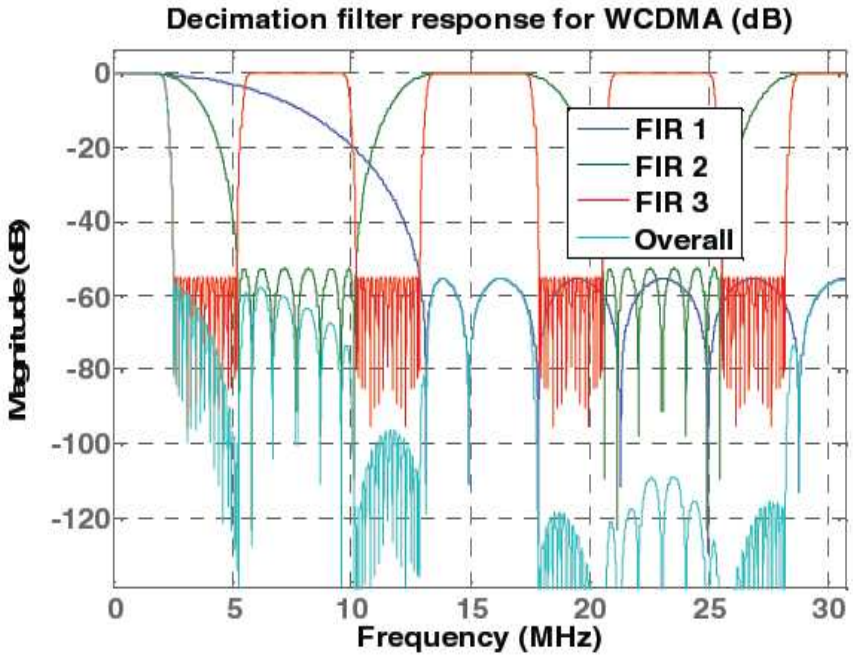

Figure 2-13 Decimation filter response (Shahana et al., 2008)

2.5.6 Low Pass band Error DDC Filter

A low pass-band error DDC filter to be work along with GSM mask frequency was reported by Ricardo (2008). A three stage DDC filter for GSM system is contains cascaded integrated comb, 21-taps as CFIR filter and 63-taps as PFIR filter. The filter is designed and simulated by using M-file program in MATLAB. Using this design the filter provide an adjacent band rejection of (-105dB) and pass-band ripple of about (-0.05dB) in filter response. The filter structure is shown in Figure 2.14.

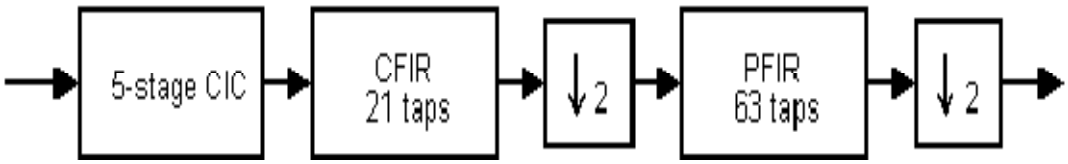

Figure 2-14 DDC filter structure (Ricardo, 2008)

The designer used to put two different weights in the PFIR filter in different band of frequency, but he selected an inappropriate place for this weight in the operating frequency at 120 KHz 130 KHz, such that the resulting response of combined filter did not satisfy the modern SDR receiver in term of pass-band ripple and band rejection, hence this design needs more tuning and rearranging of the weighted function to give better pass-band ripple and rejection requirements as well as the blocker conditions. The filter response with GSM mask frequency is illustrated in Figure 2.15.

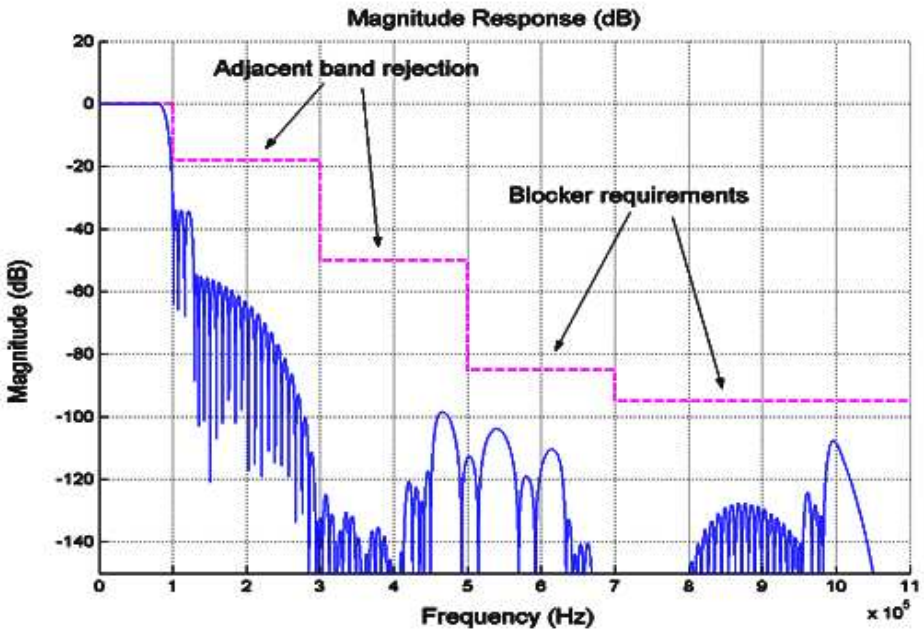

Figure 2-15 Filter response for GSM mode (Ricardo, 2008)

2.5.7 Decimation Filter Design Using MATLAB

New toolbox using Matlab programs for DDC filter design was presented by Shaha et al., (2009). The designed tools in Matlab window could be used to design the DDC filter for many standard communication systems. One may choose a necessary standard rate to provide the equivalent multi-stage conversion filter design by toolbox. This toolbox assists in providing a fast design and facilitates study of decimation filter for a lot of standard without doing large computation on the fundamental procedures. In this proposal, the Cascaded integrated comb may be used in the primary phases. By means of a half-band filter, with about half of the coefficients “zero” in the subsequent phase, gives additional decrease in filter complication. The preceding phase is a finite impulse response filter which provides the usual standard requirement but it work to decrease the frequency variety. Decreasing the quantity of coefficients in every filter part enhanced synthesis result

in situation of circuit density with energy consumption. The presented multistage decimation filter is shown in Figure 2.16 (Shaha et al., 2009).

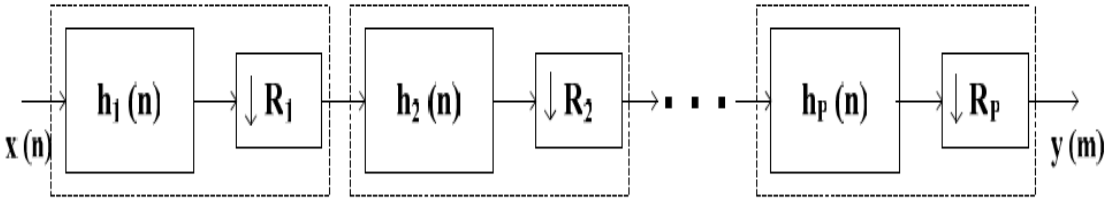

Figure 2-16 Multistage DDC filter (Shahana et al., 2009)

2.5.8 Multi Standards DDC Filter

A new design of multi standards DDC filter is available to work with GSM, IS-95 and WCDMA was produced by (Texas Instrument, 2009). This production contains three filter stages combined and this filter could convert the 69.33 MHz to 270 KHz. The input IF signal is multiplied by sine and cosine in the tow channel (I/Q) and the resulting signals is down converted from high to low baseband by three stage filtering to be processed in DSP processor. The filter chain provides the -0.03dB in the pass-band ripple and -25dB in adjacent band rejection with -105dB in the blocker region. These results are not enough to satisfy SDR requirements and need to be more efficient in terms of ripple and power consumption. The design of DDC filter is shown in Figure 2.17 and the pass-band filter response is shown in Figure 2.18. The adjacent band rejection and blocker requirements of this filter are illustrated in Figure 2.19 (Texas Instrument, 2009).

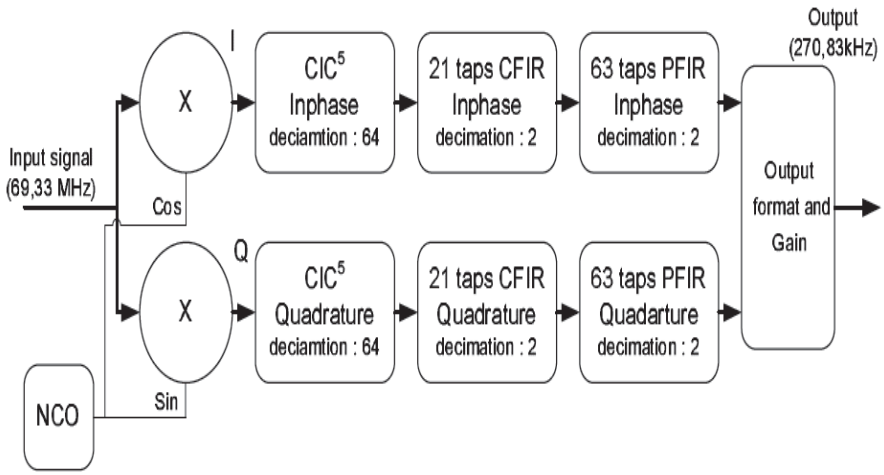

Figure 2-17 Channel of the TI GC4016 (Texas Instrument, 2009)

As obvious from the filter response in Figure 2.17, the high ripple in the band of interest (0-80KHz) will distort the received signals and the spectral replicates of succeeding stage will have effect on the system performance. In addition, the response of the proposal filter provides -25dB in the adjacent band rejection.

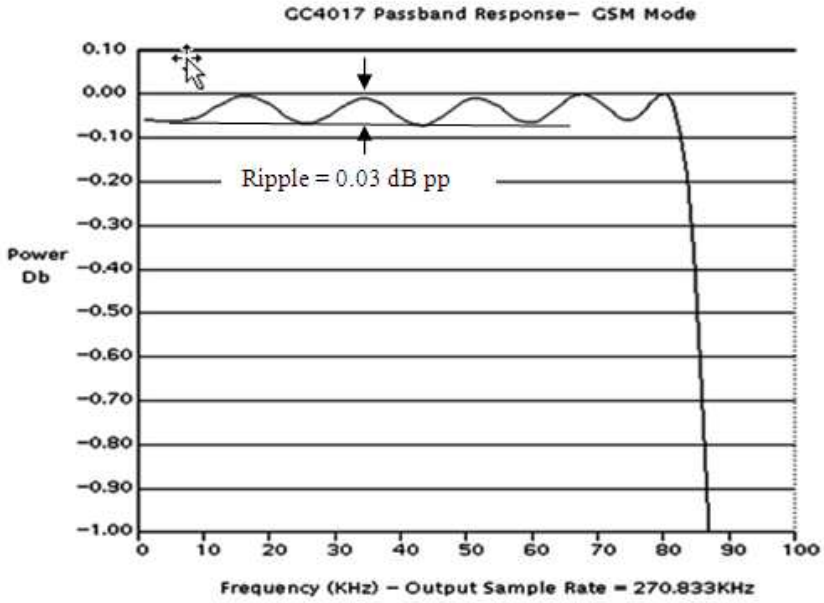

Figure 2-18 Overall passband response of GSM mode (Texas Instrument, 2009)

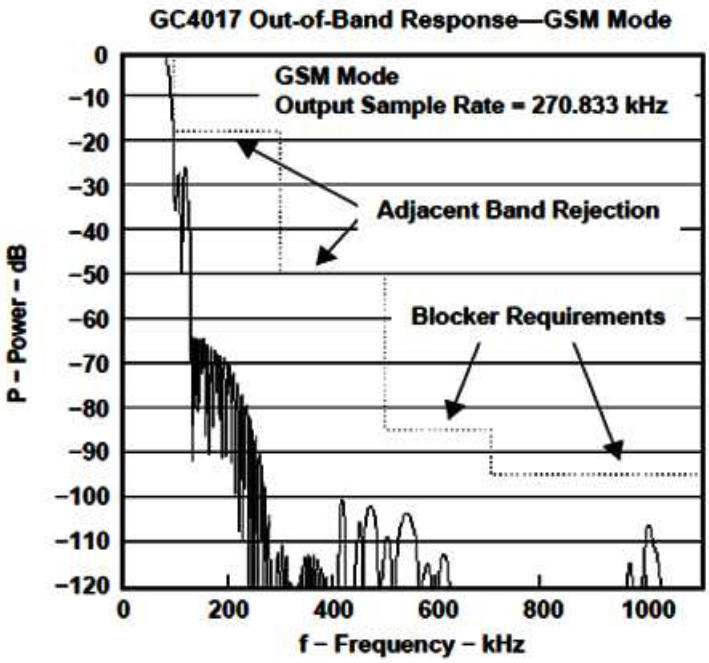

Figure 2-19 Adjacent rejection and blocker requirements (Texas Instrument, 2009)

2.5.9 Efficient DDC

Modelling of energy and area efficient digital down converters for wireless communications systems was designed by Perez et al., (2009). The filter design illustrate that when a digital receiver is considered, it exploits two clock areas. The major design parameters that contribute to build the design are the relationship between the transition band of the designed filter and its sampling frequency. In this design, the pass-band sampling is used instead of Nyquist sampling technique to provide low power consumption. The implementation of DDC structure shows the total slices elements of 1193. This result of slices is too large for the modern receiver that needs them to be very small. The receiver architecture is illustrated in Figure 2.20.