INVESTIGATION OF THE FLUID/STRUCTURE INTERACTION IN MOULDED UNDERFILL PROCESS

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INVESTIGATION OF THE FLUID/STRUCTURE INTERACTION IN MOULDED UNDERFILL PROCESS

by

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DECLARATION

I hereby declare that the work reported in this thesis is the result of my own investigation and that no part of the thesis has been plagiarized from external sources. Materials taken from other sources are duly acknowledged by giving explicit references.

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LIST OF SYMBOLS

SYMBOL	DESCRIPTION	UNITS
English Symbols		
A_1, A_2	Pre-exponential factors	1/s
B	Exponential-fitted constant	Pa.s
C_1, C_2	Fitting Constant	-
C_p	Specific heat	J/kg-K
E_t	Total energy	J/m^3
E_1, E_2	Activation energies	K
F	Front advancement parameter	-
g	Specific gravity	m/s^2
k	Thermal conductivity	W/m-K
k_1, k_2	Rate parameters described by an Arrhenius temperature dependency	1/s
m^*, n^*	Constants for the reaction order	-
n	Power law index	-
p	Pressure	Pa
r	Displacement of particle	Mm
T	Temperature	K
t	Time	s
T_b	Temperature fitted constant	K
u	Fluid velocity component in x-direction	mm/s
v	Fluid velocity component in y-direction	mm/s
w	Fluid velocity component in z-direction	mm/s
x, y, z	Cartesian coordinates	mm

Greek Symbols

α	Conversion of reaction	-
α_g	Degree of cure at gel	-
ΔH	Exothermic heat of polymerization	J/kg
η	Viscosity	Pa.s
η_0	Zero shear rate viscosity	Pa.s
ρ	Density	Kg/m^3
τ	Shear stress	Pa
$\dot{\gamma}$	Shear rate	1/s
υ	Kinematics viscosity	m^2/s
ν_{ad}	Artificial diffusity	-
Φ	Energy source term	J
τ^*	Parameter that describes the transition region between zero shear rates and the power law region of the viscosity curve	Pa
$\xi\eta\phi$	Uniform orthogonal computation space	-

LIST OF ABBREVIATIONS

2D	Two dimensional	33
3D	Three dimensional	6
ANN	Artificial neural networks	40
ADPI	Air Diffusion Performance Index	41
CAE	Computer Aided Engineering	17
BGA	Ball grid array	2
CAE	Computer aided engineering	8
CCD	Central composite design	80
CBS	Characteristic based split	33
CFD	Computational Fluid Dynamic	8
CTE	Coefficients of thermal expansion	25
CSP	Chip scale package	16

EMC	Epoxy moulding compound	7
FDM	Finite difference method	17
FE	Finite element	8
FEM	Finite element method	17
FSI	Fluid-structure interaction	7
FV	Finite volume	8
FVM	Finite volume method	12
GNF	Generalized Newtonian fluid	39
IC	Integrated circuit	1
I/O	Input / Output	9
MC	Moulding compound	24
MFCBGA	Moulded flip-chip BGA	22
MpCCI	Mesh-based parallel code coupling interface	9
MUF	Mouded underfill	2
PBGA	Plastic Ball Grid Array	31
PCB	Printed circuit board	1
PQFP	Plastic quad Flat Pack	19
RSM	Response surface methodology	11
S-CSP	Stacked-chip scale package	2
TQFP	Thin quad flat package	2
TSOP	Thin profile small outline package	2
UDFs	User defined functions	9
VOF	Volume of fluid	32

KAJIAN BAGI INTERAKSI BENDALIR/STRUKTUR DALAM PROSES UNDERFILL BERACUAN

ABSTRAK

Pembangunan pesat dalam alat electronic mudah alih seperti iPad, iPhone, iPod dan komputer riba telah mendorong teknologi pembungkusan IC ke arah pengecilan dengan pakej IC yang berciri-ciri kapasiti tinggi dan padat. Pengurangan pada saiz pakej IC telah menwujudkan cabaran kepada para jurutera dan pereka untuk mengekalkan kebolehpercayaan pakej dalam proses pembuatan yang berterusan. Dalam proses underfill beracuan, interaksi antara bendalir (EMC) dan struktur (cip silikon and bebola pateri) menghasilkan ubah bentuk yang tidak dikehendaki dan tekanan pada struktur, ini boleh menyebabkan kecacatan dan mengurangkan kebolehpercayaan pada pakej. Oleh itu, pemahaman fenomena FSI adalah penting untuk jurutera dan pereka IC untuk menangani masalah-masalah ini. Oleh itu, proses MUF dengan mempertimbangkan aspek FSI telah diberi tumpuan dalam kajian ini. Simulasi FSI telah dijalankan oleh perisian yang berdasarkan jumlah terhingga (FLUENT), dan unsur terhingga (ABAQUS), melalui teknik gandingan MpCCI untuk analisis yang serentak. Keupayaan perisian dalam menangani masalah pengkapsulan telah diperiksa dengan membandingkan keputusan yang diramal dengan keputusan terdahulu dan sekarang untuk proses pengkapsulan underfill beracuan yang berskala besar. Proses pengkapsulan underfill beracuan berskala besar difabrikasi dengan lut-sinar untuk visualisasi yang lebih baik untuk fenomena FSI, mekanisme aliran dan pembentukan udara yang terperangkap. Dalam simulasi, model kelikatan Castro-Macosko telah ditulis ke dalam UDFs untuk menerangkan kelakuan bendalir EMC. Ketepatan UDFs telah terbukti amat baik dalam memodelkan kelakuan bendalir reologi semasa proses pengkapsulan. Selain itu,

siasatan FSI dalam underfill beracuan telah dilanjutkan dengan kajian kes parametrik ke atas pelbagai faktor reka bentuk IC (iaitu, susunan bebola pateri, bentuk, bilangan kiraan I/O, ketebalan cip, ketinggian jurang) dan parameter pemprosesan (iaitu, tekanan masuk) dan kesan reologi. Kesan faktor-faktor ke atas kelakuan aliran bendalir, pembentukan udara yang terperangkap, ubah bentuk struktur dan tekanan telah dikaji. Hunbungan antara faktor dengan kesan-kesannya juga dibincangkan dan pakej dengan susunan bebola pateri jenis lingkaran mengalami tekanan dan peubahan bentuk yang paling serius. Tambahan pula, pengoptimuman menggunakan kaedah gerak-balas permukaan (RSM) telah dijalankan untuk mengkaji hubungan interaktif setiap faktor dan mengoptimumkan proses pengkapsulan underfill beracuan. Reka bentuk IC yang optimum, kawalan yang sepatutnya dalam parameter pemprosesan dan pemilihan bahan didapati mempunyai kesan penting terhadap pergerakan bendalir, pembentukan gelembung, ubah bentuk dan tekanan semasa proses pengkapsulan underfill beracuan. Reka bentuk IC yang optima untuk pakej (20 mm × 20 mm) dengan susunan bebola pateri bagi kedua-dua parameter fizikal dan proses mempunyai ciri-ciri 150 μm untuk ketinggian pateri, 250 μm untuk ketebalan cip, dan 50.43 μm untuk ketinggian jurang pada tekanan masuk sebanyak 3.43 MPa. Kajian ini dijangka memberi garis panduan dan rujukan yang bernilai untuk para jurutera dan pereka pakej semasa proses pengkapsulan MUF dalam industri mikroelektronik.

INVESTIGATION OF THE FLUID/STRUCTURE INTERACTION IN MOULDED UNDERFILL PROCESS

ABSTRACT

The rapid development of portable electronic devices, such as iPad, iPhone, iPod, and laptop, propels the integrated circuit (IC) packaging technology toward miniaturization characterized by high capacity and compactness of IC package. The scaling down of IC package size has given challenges to the engineers and IC designers in maintaining package reliability. In moulded underfill (MUF) process, the interaction between fluid (EMC) and structure (silicon chip and solder bump) yields unintended deformation and stress that may cause defects and reduce package reliability. Thus, the understanding of the FSI phenomenon is essential for the engineers and IC designers to tackle these problems. Therefore, the MUF process considering FSI aspect was the focus of this research. The FSI simulation was performed by finite volume based (FLUENT) and finite element based (ABAQUS) software through the MpCCI coupling technique for the simultaneous analysis. The capability of the software in handling encapsulation problems was examined by comparing the predicted results with previous scholars' works and the current scaled-up MUF encapsulation processes. The scaled-up MUF encapsulation processes were fabricated in transparent for better visualization of FSI phenomenon, flow and void formation mechanisms. In the simulation, the Castro-Macosko viscosity model was written into UDFs to describe the EMC fluid behaviour. The accurateness of the UDFs has been proven excellent in modelling the rheological fluid behaviour during the encapsulation process. Moreover, the FSI investigations on the MUF process were extended to the parametric case studies on various IC design factors (i.e., solder bump arrangement, shapes, number of I/O count, chip thickness, gap height),

processing parameter (i.e., inlet pressure) and rheological effect. The effects of these factors on the fluid flow behaviour, void formation, structure deformation and stress have been studied. The correlation between the design factors and those effects has been discussed and it was found that package with perimeter solder bump arrangement endured highest stress and deformation. Furthermore, the optimization using response surface methodology (RSM) was carried out to investigate the interactive relationship of each factor and optimize the MUF encapsulation process. The optimal package design, proper control of the processing parameter and material selection were found crucially influenced the fluid flow mechanism, void formation, deformation and stress during the MUF encapsulation process. The optimum design of the IC package (20 mm × 20 mm) with perimeter solder bump arrangement for both physical and process parameters was characterized by 150 μm of solder bump standoff height, 250 μm of chip thickness, and 50.43 μm of gap-wise at the inlet condition of 3.43 MPa. The current study is expected to provide valuable guidelines and references for the engineers and IC designers during the MUF encapsulation process in microelectronics industry.

CHAPTER 1

INTRODUCTION

1.1 Introduction

The rapid development of the portable electronic devices such as smart phone, laptop and tablet PC facilitates the communications, managing and sharing the information and entertainment. Slim and ergonomic designs of these devices create the challenging task to the designer and engineer. Compact characteristics, high performance and high reliability of IC package are needed to suit into a limited space of those devices. To accomplish these goals, the design of the IC package is now towards miniaturization and diversification for various IC applications. In the microelectronic industry, IC package designers and engineers are always concern with the reliability and quality of the IC package. To overcome these problems, the IC encapsulation process is utilized to encapsulate and protect the IC structures such as silicon chip, solder bump, wires, IC paddle and lead-frame from the hazardous environments. During IC encapsulation, the interaction between EMC and IC structures may yield undesirable defects on the IC package. Improper process control, material selection and the IC design may reduce the package reliability. As a result, it may cause reliability failure. Therefore, the understanding of the phenomenon occurs during the IC encapsulation is imperative to handle the IC design, process control, and material selection for optimal IC encapsulation process.

1.2 IC Packaging and Encapsulation Process

IC packaging provides reliable housing and protection for IC chip (silicon die), and protects the interconnection of the IC chip to other components such as PCBs, transformers, and connectors. It also mechanically supports the IC package.

Hence, the IC package is protected from vibration and mechanical stress. The exposure of IC chip and interconnectors (solder bumps and wire bonding) to moisture, ionic contamination, radiation, heat, and thermo-mechanical stress leads to defects and failures of the IC package. Therefore, IC encapsulation is a crucial process in IC packaging because it protects the IC chip and interconnectors from hazardous environment.

During IC encapsulation, the encapsulant is transferred into the mould cavity to encapsulate the IC structures (silicon chip, solder bump, wire bonding, lead frame, and paddle) by using transfer moulding technology. Figure 1.1 illustrates the transfer moulding technique during encapsulation. This technique has been widely applied to various IC packaging such as thin quad flat package (TQFP), thin profile small outline package (TSOP II 54 L LOC), stacked-chip scale package (S-CSP), mould array package, moulded underfill (MUF), flip chip underfill encapsulation, and ball grid array package (BGA). Several issues, including structural deformation, overstress and void formation, reduce package reliability during encapsulation.

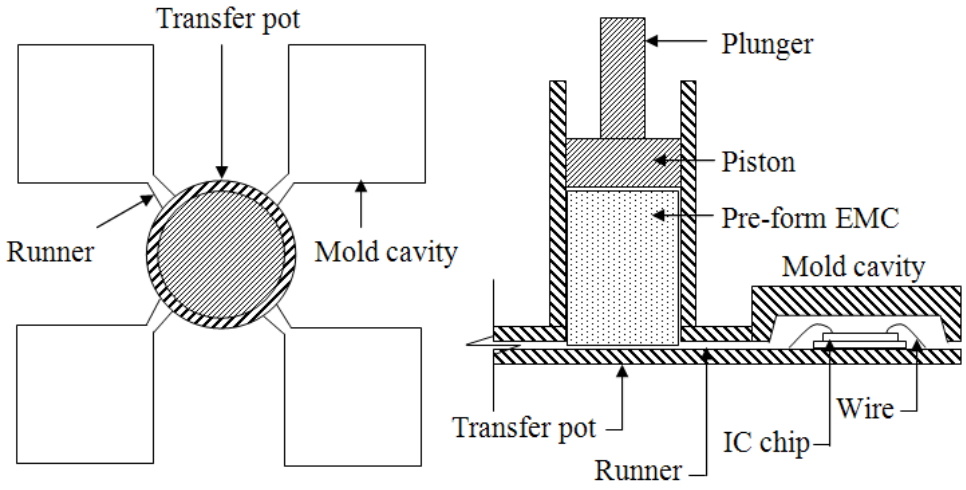


Figure 1.1: Illustration of moulding encapsulation setup.

1.2.1 Flip chip underfill process

The flip chip package was developed by IBM in the early of 1960s to enrich microelectronic technology. The development of flip chips enables the IC package to be designed with a high number of interconnectors. Thus, the reliability of the interconnectors is significant for the flip chip package. In flip chip packaging, the underfill encapsulant is applied to protect the interconnectors from harmful environment. The underfill encapsulant fills the intermediate space between flip chip and substrate, which consists of interconnectors (solder bump). The capillary effect of the intermediate space let the encapsulant flow through the space in the conventional underfilling method. Figure 1.2 illustrates the underfill process.

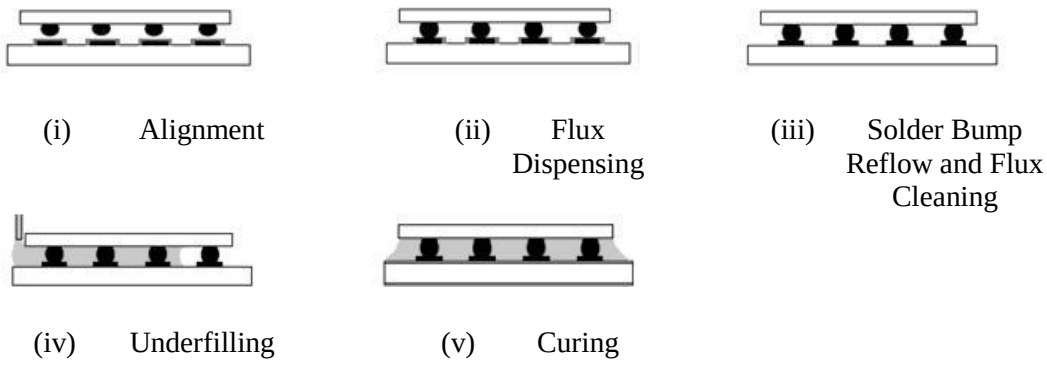


Figure 1.2: Conventional underfill process (Wan et al, 2007).

The longer filling time of the conventional flip chip underfill has become the bottleneck in the microelectronic industry. Lower productivity may cause an increase of manufacturing cost. The productivity of the underfill process is lower compared with other types of IC encapsulation process. This is because the underfilling process is dependent on the speed of encapsulant flow that fills the space between the flip chip and substrate as illustrated in Figure 1.2. Alternatively, the pressurized underfill process had been proposed to overcome the problem.

The pressurized underfill process was thus developed by Han and Wang (1997) to address this problem. Pressurized underfill is performed by using a specially designed mould as shown in Figure 1.3. Vacuum conditioning at the air vent assists the smooth flow of the encapsulant. The application of pressurized underfill significantly reduces filling time and allows the use of highly viscous encapsulants in enhancing package reliability. However, the specific pressurized underfill mould design may only apply for a certain chip size or specific flip chip design and may also costly for the hardware modification. Thus, this technique is not widely applied in the industry.

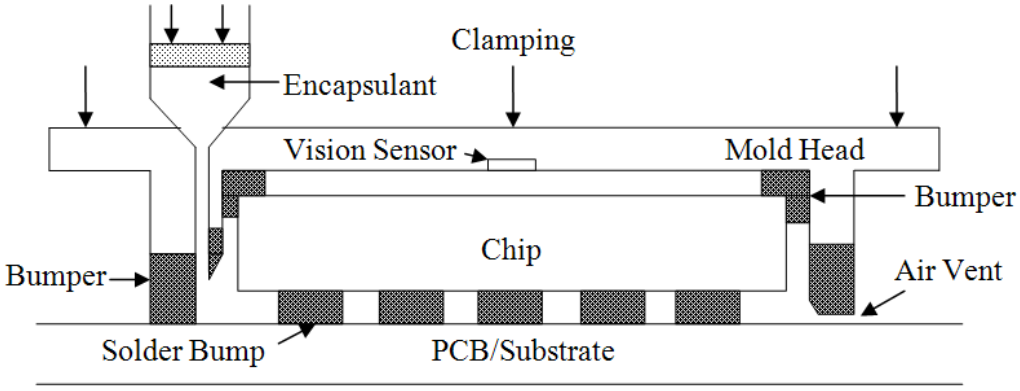


Figure 1.3: The pressurized process of underfill (Han and Wang, 1997).

Low cost and high throughput of the process are always the concerns in manufacturing process. The reduction in processing step can directly reduce the cost. In order to reduce processing steps, no-flow underfill process had been introduced to assemble and underfill the space between flip chip and substrate as depicted in Figure 1.4. The advantages (Painaik and Hurley, 2004) of the no-flow underfill process include simplification of process, no-additional flux agent needed, and curability of the no-flow underfill material in the reflow process. Development of the no-flow underfill was implemented on lead-free flip chip packaging. These underfill

techniques have also been applied on the high-density bump and fine pitch of flip chip package, board-level assembly, and assembly of flip chip flex BGA and micro-BGA. Although this underfill method yields higher throughput and low cost, but the void formation during the process causes the reduction in package reliability. Improper process control of soak temperature and time may cause voids at the solder joints and the intermediate space; hence, diminish the package reliability. Voids in the package may induce stress concentration, delamination and solder extrusion; hence caused early failure of the package (Wan et al., 2007). Therefore, the moulded underfill technique had been introduced to address the package reliability problem.

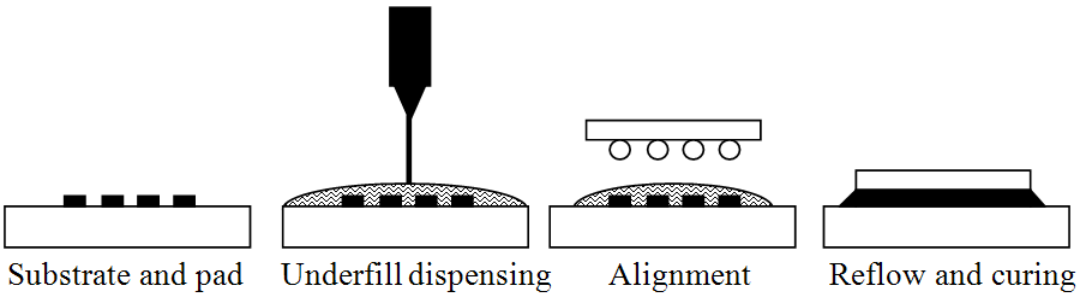


Figure 1.4: No-flow underfill processes (Wan et al, 2007).

1.2.2 Moulded underfill (MUF) encapsulation process

The microelectronic industry is focused on achieving high productivity, low cost and high reliability of the IC package in the manufacturing process. In conventional flip chip packaging, longer filling time affects the production speed of IC packages. Enhanced productivity can be accomplished through the implementation of transfer moulding technique (Becker et al, 2001) with single moulding step. The MUF process minimizes production time, improves package reliability and package co-planarity, and reduces stress concentration on the interconnectors (Chen, 2008). Thus, its excellent characteristics have led to the widely use of the MUF package in mobile applications (Joshi et al, 2010). However,

the application of this method on the 3D small-scale and thinned stacking chip still needs further research before it can be applied into mass production. Figure 1.5 shows the schematic of MUF process.

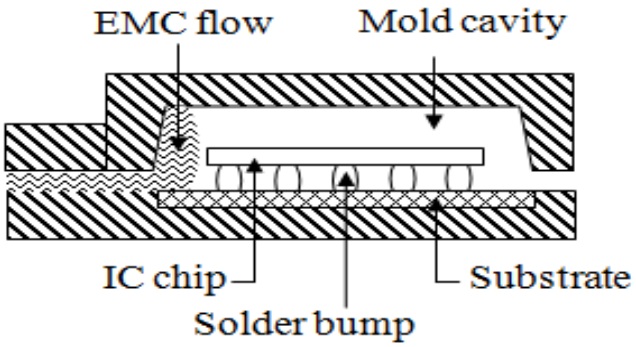


Figure 1.5: Moulded underfill process.

1.3 MUF encapsulation background and problem statement

Encapsulation process is a popular technique to encapsulate and protect the IC chip. This technique provides reliable housing to IC chip and also enhances the IC package interconnections. The development of the flip chip underfill process from the conventional method to the moulded underfill method has been discussed in Sections 1.2.1 and 1.2.2. The conventional flip chip underfill technique has been practiced for nearly 25 years (Wan et al., 2007), however, the low productivity and long filling time have become the constraint in the microelectronic industry. Therefore, the improved underfill technique is important to yield better productivity and reliability of the IC package.

There is a wide research gap in the field of MUF technique. Many research and development activities are still carried out by the researchers to better understand the MUF technique. Although this technique has been introduced for nearly 12 years and patented by Weber (2000), it is still difficult to observe the fluid-structure interaction phenomenon during the MUF process especially for small scale and thinned chips of

IC packages. Besides, there are still limited literatures available in this topic. The design of the IC package, the process control parameters and the material selection for MUF process affect the fluid flow behaviour, structural deformation, stress concentration, especially on the chip and solder bump. Improper control of these factors may cause void formation, critical structural deformation, and also induce initial failure of the package. To minimize the impact of these problems, the understanding of MUF encapsulation process is significant. Thus, computational simulation is advantageous for the visualization, and for a better understanding of the physicochemistry of FSI phenomenon. To attempt the solution, several commercial software solutions had been developed for the encapsulation process, such as Moldflow, Cadmould, C-mould, MAGMAsoft, Flow-3D etc. However, these software solutions are mainly for the fluid flow analysis but limited for the FSI analysis.

The IC package design is toward miniaturization, compact and high performance. The encapsulation of miniaturized IC package yields the challenging task to IC designers and engineers in maintaining the package reliability. In addition, the reduction of silicon chip and solder bump sizes might bring more challenges to MUF process. The interaction between EMC fluid and structures could cause unintended deformation and stress that impose on the structure. The extreme structural deformation and stress on structures reduce package reliability in the subsequent manufacturing process. As a result, it could increase the rejection rate of IC products due to the malfunction of package. Therefore, the understanding of FSI phenomenon is crucial to tackle this problem through optimal IC package design and proper process control.

In the MUF process, small IC package and non-transparent packaging mould cause difficulties in visualising FSI phenomenon. FSI also occurs in the encapsulation of wire-bonding package, as it was extensively reported in the available literature. The deformation of wire bond is normally observed from the top view of IC package. However, the visualisation of FSI in the moulded flip chip package by using MUF technique is more complicated than the wire-bonding package. The horizontal position of the chip complicates FSI visualisation. The chip is thin and tiny in package size. The best method for visualising FSI is through cross-sectional and side views of the scaled-up transparent mould, and also by using the simulation tools.

1.4 Objectives of the study

The general objective of this research work is to investigate the fluid/structure interaction during moulded underfill process. The understandings of moulded underfill process are significant for IC designers and engineers to obtain the optimal IC package design and process control. In order to achieve these aims, six main objectives were set out as mentioned below:

1. To validate the predictions of modelling tools, CFD and CAE in the fluid flow and structural analyses of MUF process.
2. To validate the predictions of encapsulation process in S-CSP, TQFP underfill and MUF encapsulation processes using various viscosity model and user defined functions (UDFs) of Castro-Macosko model.
3. To carry out and establish the experiment on a scaled-up MUF process.
4. To visualize and study the FSI phenomenon on the scaled-up MUF process in the experiment and simulation.

5. To study the effect of different parameters such as inlet pressure, solder bump arrangement, shapes, number of I/O counts, and chip thickness to the IC structures of the MUF IC package.
6. To perform the computational optimization of MUF process by using response surface method and to study the interactive relationship of each factor to the responses.

1.5 Scope of the research work

In this research work, the investigation of FSI phenomenon is focused on the MUF encapsulation process through the simulation and scaled-up experiment. The FSI simulation of fluid flow and structural analyses concentrates on the actual size of MUF packages by considering the Castro-Macosko viscosity model to describe the realistic moulding flow behaviour. This research also focused on the parametric case studies to enrich the understanding of each factor. Moreover, the optimization of the IC package using response surface methodology was carried out to investigate the interactive relationship of the factors to minimize the deformation, stress, void formation and filling time in the encapsulation process. The validation of the FSI simulation on solving fluid flow and structural predictions were performed with scaled-up experiment and the polymer behaviour of Castro-Macosko model was compared with TQFP and S-CSP encapsulation obtained by the previous researchers.

1.6 Thesis outline

This thesis is organized in five chapters. Brief presentation about IC packaging, flip chip underfill, background, objectives and scope of research have been introduced in chapter one. In chapter 2, literature study of moulded IC

encapsulation process is presented. The methodology in mathematical modelling and numerical method is highlighted in chapter 3. In chapter 4, the validation of experimental and simulation results, parametric case studies and optimization of IC package are presented. The interactive relationship of each factor and the minimization of the responses are also discussed in this chapter. Lastly, concluding remarks on the studies and recommendation for future works are described in chapter 5.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The current trend of microelectronics packaging is toward smaller, thinner, higher performance, compact and higher reliability, such as high I/O chip, thin package, multi chip module etc. These IC characteristics boost the challenges to IC designers and engineers in maintaining the package reliability through the subsequent manufacturing process. In the aspect of manufacturing, longer production time consumes higher cost, for example, flip chip underfill process would take a longer time compared with transfer moulding IC encapsulation. Thus, moulded underfill encapsulation process was proposed and developed by Weber (2000), in which the underfill and encapsulation are preformed in a single step. In this chapter, a substantial amount of previous works on the underfill, IC encapsulation and moulded underfill processes is discussed. Moreover, the fluid behaviour modelling, fluid-structure analysis, RSM optimization are also discussed in this chapter.

2.2 Flip chip underfill process

In early 1960s, IBM developed the C4 (Controlled Collapse Chip Connection) flip chip package, through the connection of solder bumps from silicon chip to substrate for electricity supply. The reliability of the solder bump is important for the flip chip IC package. To maintain the package reliability, the underfill encapsulant is applied during the packaging process to protect the interconnector. In the conventional underfill process, the encapsulant is dispensed to fill the intermediate space between IC chip and substrate, which consists of solder bumps. During the filling process, the encapsulant is driven by the capillary effect of the intermediate

space as presented in Section 1.2.1. Improper control of the underfill process can cause cracking problems and high-stress concentration on the solder bump (Su et al., 1999). Moreover, the material significantly affects flip chip reliability (Lau et al., 2000) because imperfections of the underfill lead to delamination of the silicon chip and the substrate as well as induced cracks. Delamination is caused by the separated interface between the encapsulant and structure. Fluid flow characteristics (Yamada and Togasaki, 2003) during the underfill process are influenced by the design of interconnectors, such as solder bump standoff height, solder bump pitch, and bump gap. A large chip size with a small bump gap and high I/O counts allows a uniform flow and a void-free condition. Defects such as fractures (Zhang et al., 2008), crack on die and underfill (Shim et al., 2000), and voids in the package (Lee et al., 2010) reduce the reliability of the flip chip package.

Substantial modelling studies (Wheeler and Bailey, 2000; Pantuso et al., 2003; Lai and Young, 2004; Wan et al., 2005; Wan et al., 2009; Young, 2010; Khor et al., 2010) had been conducted to describe the encapsulant flow during the underfill process, including analytical models for flow front advancement and filling time. On the other hand, CFD applications in the conventional underfill process provide apparent visualization of the underfill process and predictions of underfill behaviour. Several solving methods have been utilized in predicting underfill flow, including FEM (Han and Wang, 1997; Tay et al., 1997), FVM (Yang et al., 1998), and characteristic split-based method with FEM (Kulkarni et al., 2006), which discretized the governing equations of the fluid flow during the simulation. In the underfill encapsulation process, Han and Wang (1997) noted that the surface tension of the encapsulant slightly decreased with the increase of temperature, and that the dynamic contact angle was an important consideration in the underfill process. Besides, Tay et

al. (1997) found that the underfill time was proportional to surface tension and inversely proportional to viscosity. Besides, the filling of fluid in conventional underfill encapsulation is driven by capillary effect that is dependent on the surface tension (Pantuso et al., 2003) of the chip and substrate.

Zheng et al. (2008) also carried out two-dimensional underfill flow modelling. The improvement of underfill on various dispensing patterns was performed by Xie et al. (2008) by using a 3D flow model, which was well validated by experimental results. Furthermore, Wan et al. (2009) enhanced the numerical modelling of flip chip underfill by developing analytical equations and using power law equation to describe non-Newtonian fluid behaviour. They performed underfill predictions by using ANSYS software, as depicted in Figure 2.1, and their predictions were in good agreement with the experimental work of Nguyen et al. (1999).

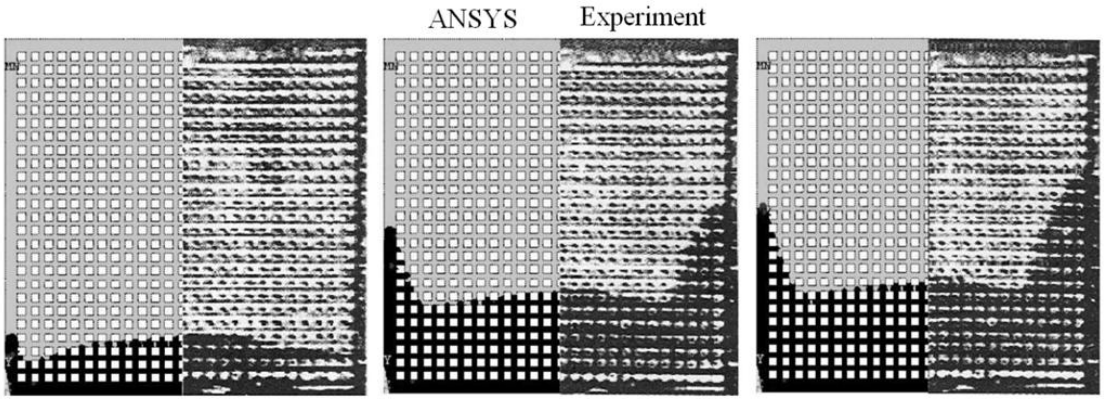


Figure 2.1: Predicted underfill flow profile by Wan et al. (2009) and experimental results (Nguyen et al., 1999).

In recent years, the application of FV-based software FLUENT was reported by Khor et al. (2010), who investigated the 3D conventional underfill process by taking into account the solder bump pattern of the flip chip package. The design of the solder bump pattern in the flip chip underfill had a crucial effect on filling time and flow front velocity, which caused the full array package to consume a longer

filling time for the underfill process. The presence of the solder bump restricted the fluid flow to a narrow space. The predictions of FLUENT results are shown in Figure 2.2.

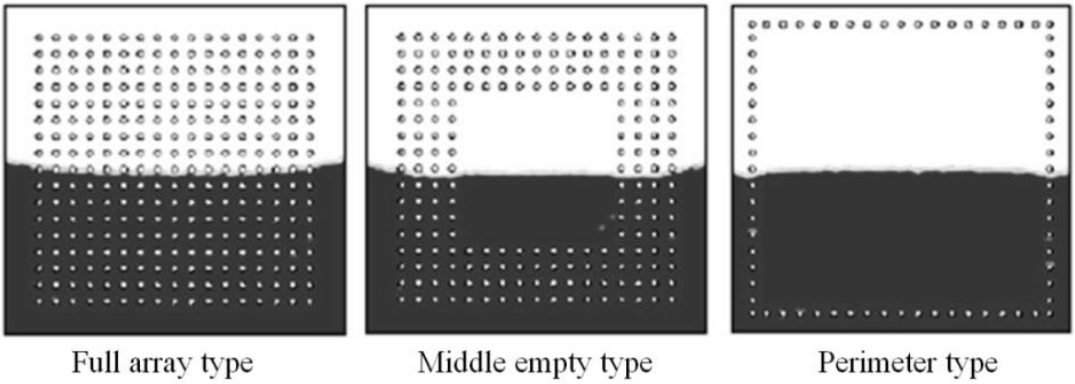


Figure 2.2: Capillary driven underfill process at 50% filling stage for different solder bump pattern (Khor et al., 2010).

Recently, an improvement on the flow front tracking method was carried out by Wang et al. (2011) by using the PLIC–FAN (Piecewise linear interface calculation – flow analysis network) method in a capillary driven underfill process. This method handled the interface reconstruction and tracked the melt front at every time step. They used Petrov–Galerkin methods to solve the fluid flow governing equations. Their simulation results showed realistic predictions on the melt front of the underfill. A comparison of the experimental and simulation results by Wang et al. (2011) is presented in Figure 2.3. Their studies and application of algorithm have contributed to the improvement of virtual modelling. In addition, Moon et al. (2011) addressed the importance of edge effect in underfill modelling and showed that neglecting the edge effect will affect the accuracy of predictions. The 3D modelling and experimental results obtained by Moon et al. are illustrated in Figure 2.4.

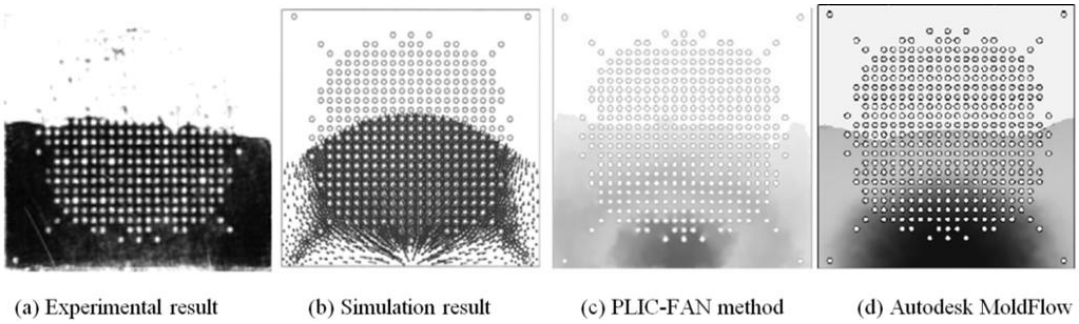


Figure 2.3: Flow front profile (a) Experimental and (b) simulation results by Han and Wang (1997); (c) PLIC-FAN method and (d) Autodesk MoldFlow by Wang et al. (2011).

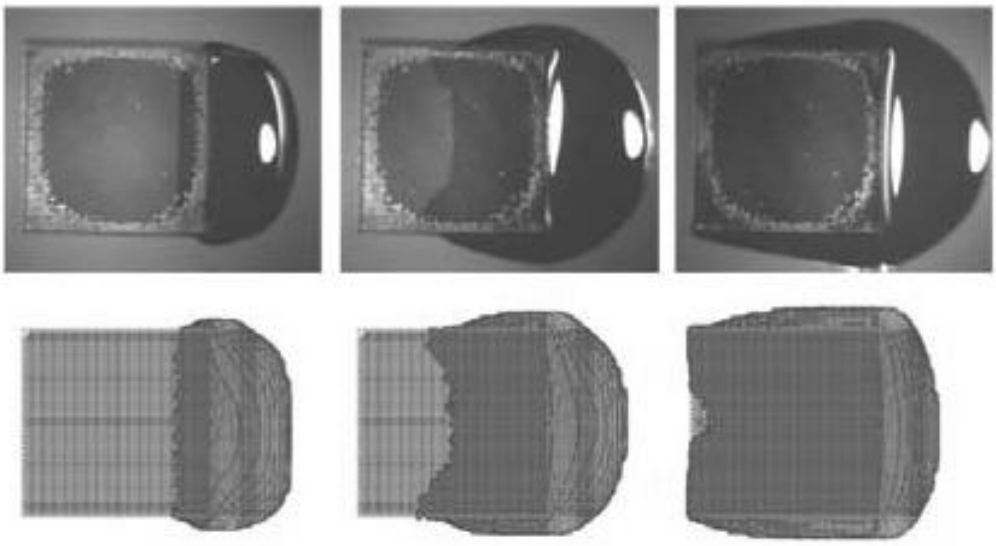


Figure 2.4: Edge effect of underfill modelling (Moon et al., 2011) at 10, 60 and 95 % of filling.

2.3 IC Encapsulation process

IC package reliability is a main issue in IC packaging. Reliability parameters in the IC encapsulation process are usually referred to the deformation, stress imposed on IC structures (e.g. silicon chip, solder bump, wire bond and IC paddle) and void formation. High deformation, stress imposed on IC structures and void in the IC package may cause the malfunction of package. Improper processing, material selection, and package design yield unintended defects or features to the IC package in the subsequent processes. These defects and features cause failures to the IC

package, such as interconnector cracks or fractures, structural deformation, interface delamination, and overstress. These defects consequently cause the IC package to break down. In the encapsulation process, the feeding of viscous polymer fluid (e.g., EMC and liquid encapsulant) causes the interaction between fluid and structure during encapsulation. This interaction induces the deformation of IC structures, including wire sweep and lead-frame deformation. Unstable filling during encapsulation also contributes to void formation or incomplete filling of mould cavity. To eliminate and minimize the defects in the encapsulation process, the understanding of the process is important. In this section, a substantial amount of works on the IC encapsulation is considered in TQFP, S-CSP and MUF packages. Reliability issues during encapsulation process are also discussed in the subsequent sections.

2.3.1 Encapsulation process for TQFP and S-CSP packages

Various IC packages are designed for the variety applications of electronic devices. TQFP is popularly used in portable electronic devices such as cell phone, portable personal computer, and digital camera because it is lightweight and has good thermal performance. Figures 2.5 and 2.6 depict a typical TQFP IC package and its internal structures within the package. During encapsulation, the interaction phenomenon induces the structural deformation such as wire bonding and paddle shift. Therefore, encapsulation process must be properly controlled to eliminate these problems. The study on the predictions of 144-lead TQFP encapsulation was carried out by Nguyen et al., (2000) through computational modelling by using the CFD-ACE (U) solver of the PLICE-CAD software package. The experiment was conducted by using transfer-moulding technique on the commercially available

TQFP package with the dimensions of 20 mm × 20 mm × 14 mm. Their results were found in good conformity with the short-shot experimental results. Minor discrepancies were observed for flow front shape and locations compared with the experiment because a simple geometric model was used.

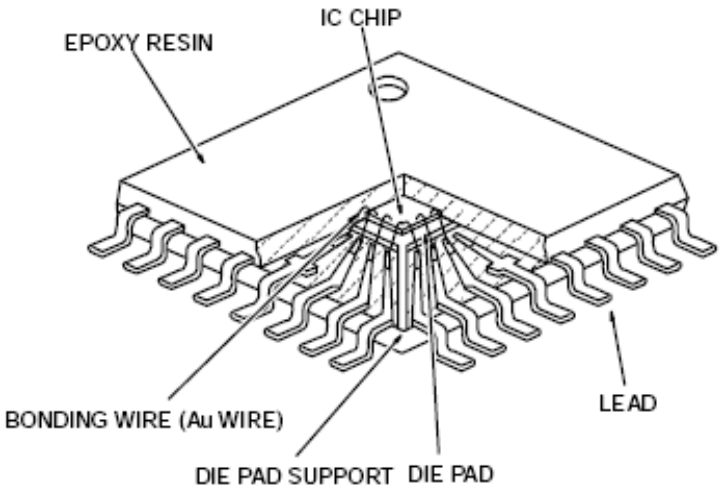


Figure 2.5: Schematic of a TQFP [http://cpu.linuxmania.net].

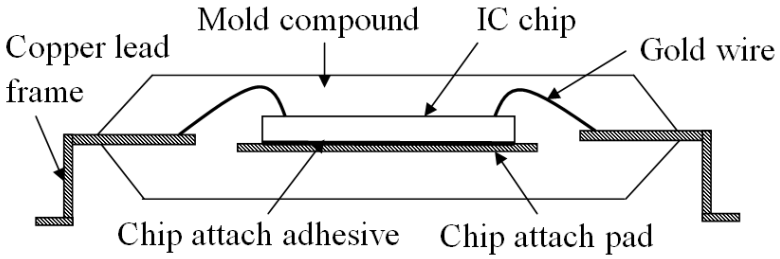


Figure 2.6: Illustration of typical TQFP (Ref. http://www.practicalcomponents.com).

During the encapsulation, the interaction between fluid and structure causes other issues in package reliability. The integration of CFD and CAE software allows the researcher to perform structural analysis. Teng and Hwang (2008) utilized the Moldex3D-RIM software to simulate encapsulation of the TQFP process and the commercial finite element (FE)-based ANSYS to conduct structural calculation. The generated fluid flow data were extracted by using InPack software, and then transferred to ANSYS. In their analysis, the paddle shift was attributed to unstable

filling because the lead frame was subjected to unstable forces. The corner regions of the chip also had an air trap. Figure 2.7 illustrates the experimental and simulation results using Moldex3D-RIM software. A similar paddle shift phenomenon was also observed in other studies (Shen et al., 2007; Chou et al., 2009; Chen et al., 2007; Pei and Hwang, 2005). Finite element method (FEM) and finite difference method (FDM) (Kuah et al., 1996) were also utilized to simulate the flow modelling of plastic quad flat package (PQFP) using transfer moulding while considering the lead frame and wire structures during encapsulation.

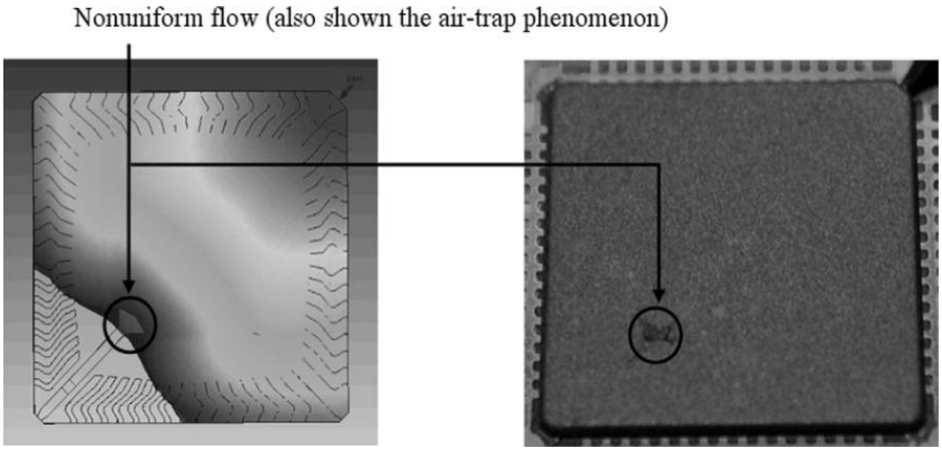
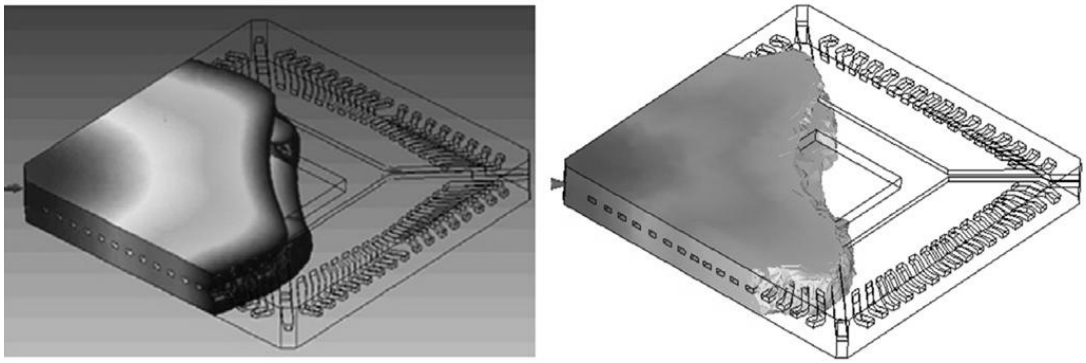


Figure 2.7: Simulation and experimental results by Teng and Hwang (2008).

In recent years, Wang et al. (2010) introduced the Galerkin/least-squares stabilized FEM during microchip encapsulation. The similar technique was also used for underfill process as mentioned in Section 2.2. Piecewise linear interface calculation–flow analysis network (PLIC–FAN) method was applied for melt front tracking by reconstructing the interface of fluid and air phases. The simulation system was developed and carried out by using VC++ 6.0. Their algorithm predicts the details of the melt front by considering the presence of the lead frame and IC chip (Figure 2.8). The smooth melt front is shown in the predictions of Moldex-3D (Figure 2.8a). However, they predicted the detailed disturbance on the melt front.

The occurrence of non-uniform melt front that was due to the lead frame and IC chip, which is clearly visualized in Figure 2.8 (b). Hence, the continuous improvement in virtual modelling yields realistic predictions of flow front advancement in the IC encapsulation process.



(a) Moldex-3D (b) Stabilized filling method

Figure 2.8: Melt front prediction (a) Modex-3D (Teng and Hwang, 2008) and (b) stabilized filling method (Wang et al., 2010).

Stacking chip technology allows the IC packages to be compact and with high capacity by stacking the package vertically. The technology is a result of the high demand and high performance of electronic devices. The current and future trends of stacking chip technology are presented in Figure 2.9. The increased IC chip and wire bonding in IC package need reliable protection. Thus, encapsulation process is also applied to the stacking chip package. Multifarious research effort has been performed in encapsulation simulation for S-CSP package. Moon et al. (2007) investigated stacking chip packages using MoldFlow through the injection moulding technique. The design of stacked-die configuration, mould cap clearance, and properties of the moulding compound significantly affected the flow front profiles during filling. The overhang of stacking chip may increase the tendency of void formation and cause mechanical failures. Moreover, increasing mould gap clearance and decreasing fluid viscosity could achieve uniform flow front profiles.

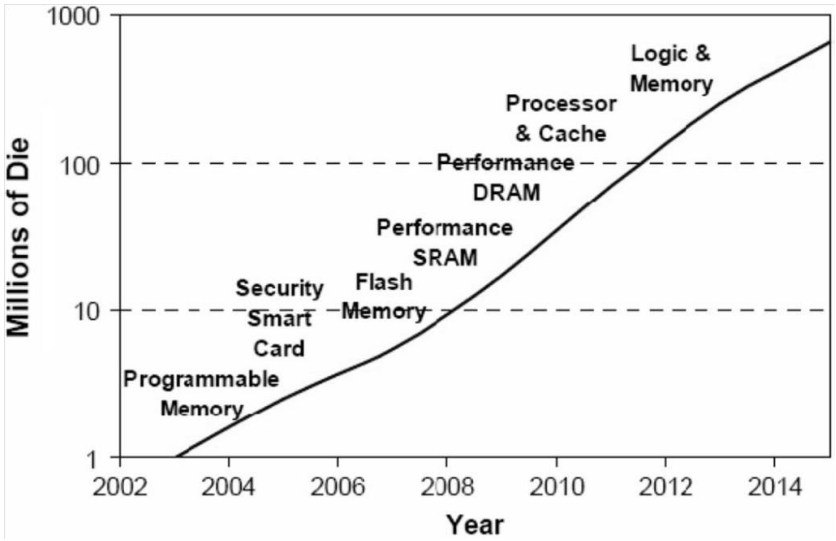


Figure 2.9: Chip staking trends (Agonafer et al., 2006).

Abdullah et al. (2007, 2008, and 2010) studied the encapsulation process of S-CSP package by using the FORTRAN program. FDM was applied to discretize the governing equations. Figure 2.10 depicts the melt front predictions by using FORTRAN 77 program. Retardation of EMC material advanced the slower flow front and increased the resistance of fluid flow during the process. The selection of the viscosity model for EMC is also essential to the simulation results while the Castro–Macosko model describes the optimized EMC predictions during IC encapsulation. Thus, the design of stacking chips and the characteristics of moulding compound are important in the modelling of IC encapsulation. Similarly, Ramdan et al. (2012b) had studied the S-CSP encapsulation (Figure 2.11) by using FLUENT focused on the venting effect. They found the flow front distribution of S-CSP encapsulation process and pressure profiles within the cavity significantly influenced by the number of vents, position and size.

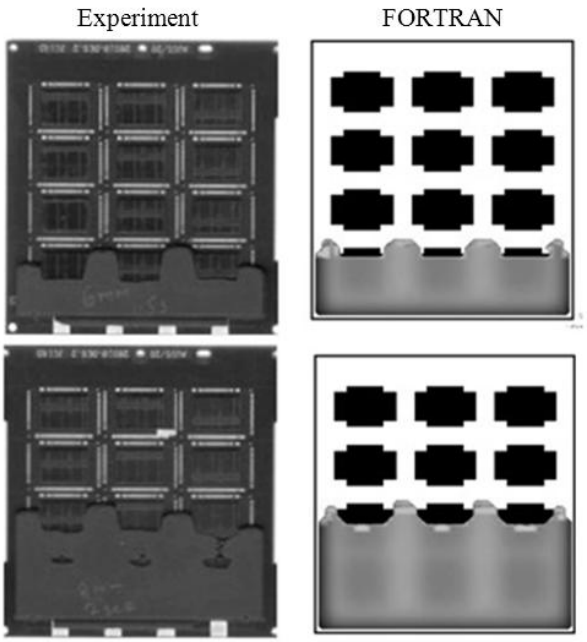


Figure 2.10: Predicted melt front using FORTRAN and experimental results (Abdullah et al., 2007).

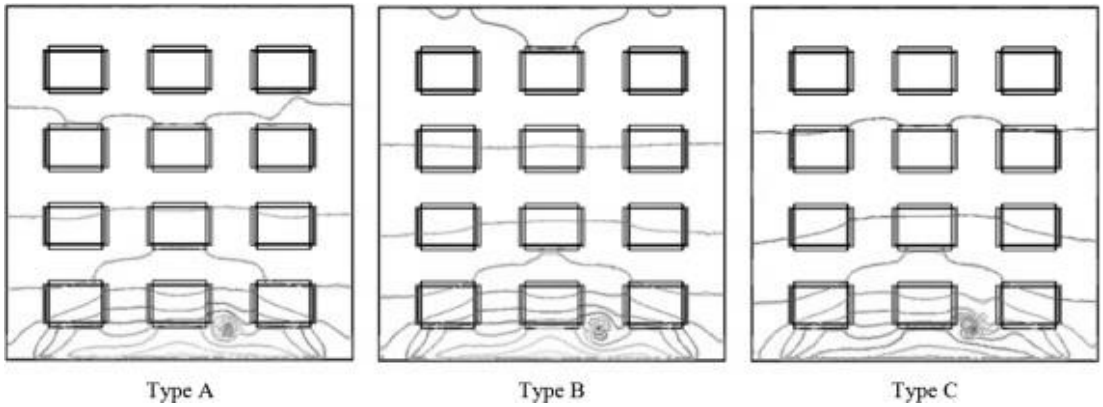


Figure 2.11: Predicted pressure profile using FLUENT by different venting designs (Ramdan et al., 2012b).

2.3.2 Moulded underfill (MUF)

High productivity and low cost in the manufacturing process are the desired goals of engineers in the microelectronic industry. Conventional flip chip packaging requires more filling time, which affects the subsequent production speed of IC packages (Rector and Fisher, 2011) and creates a bottleneck. Alternatively, the implementation of transfer moulding technique (Becker et al., 2001) can reduce the

number of processing steps, where the underfill and encapsulation are performed at a single moulding step. Thus, this process enhances the overall productivity by reducing the production time, improving package reliability, enhancing package co-planarity, and reducing stress concentration on the solder bumps (Chen, 2008). Moreover, this moulding technique also helps in reducing thermal mismatch (Braun et al., 2002), enhancing stress performance (Kao et al., 2004), providing better electrical (Braun et al., 2006) and thermal performance (Tsai et al., 2007). Besides, vacuum conditioning during the MUF process and its material performance also make it void-free during encapsulation process. Therefore, its excellent characteristics have made MUF package widely used in mobile applications (Joshi et al., 2010). Further reviews on the MUF developments will be discussed in the following paragraphs.

Lee et al. (2008) investigated the MUF process on a flip chip multi-chip module by using transfer moulding. Modex3D software was utilized to handle flow front modelling in the MUF process. A characterization of the MUF rheological compound was also considered. Void formation was observed at the top-left and bottom-right gate locations in their experimental and simulation results. The void formation was still observed when seven different types of gate and locations were employed by using the finite element model. They found that the optimized design with the top-left pin gate solved the void formation problem in the packaging, and they concluded that an optimal design is a significant and effective way to solve the void formation in the MUF process. The numerical and experimental results were found to be in good conformity, as clearly shown in Figure 2.12.

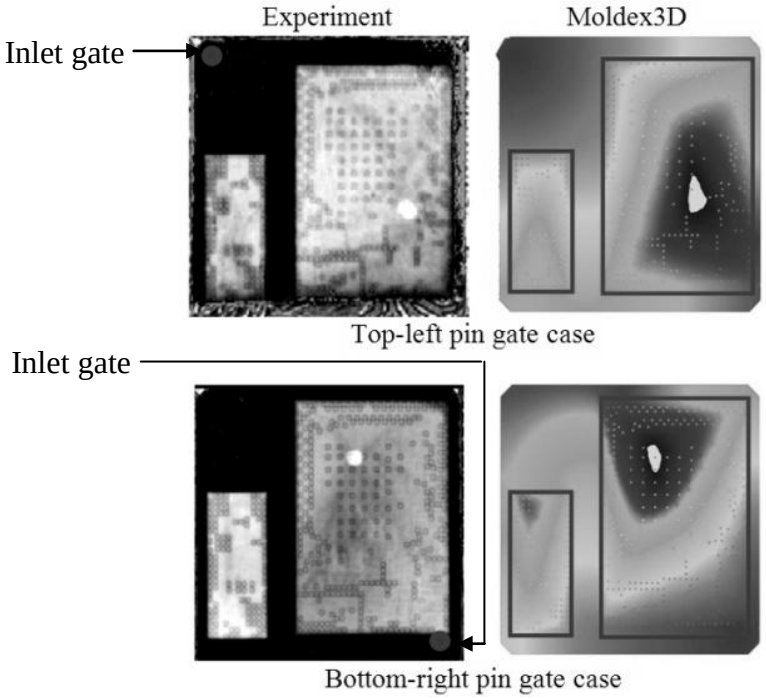


Figure 2.12: Experimental and Moldex3D results on predicted void formation (Lee et al., 2008).

The underfill techniques offer significant productivity improvement through capillary underfill process. The effect of no-flux type of flip-chip packaging on the interfacial adhesion in the moulded underfill package was examined by Rector and Fischer (2001) by using scanning acoustic microscopy. The moulded flip-chip packages fulfilled the JEDEC (Joint Electron Devices Engineering Council) level 3 requirement and showed the greatest reliability in thermal shock tests. Kooi et al. (2004) investigated the flip-chip package by using transfer moulding technique. They focused on the exposed die moulded package and non-exposed die MUF for the matrix array packaging (Figure 2.13). Both packages were tested and the non-exposed die moulded package showed a better reliability performance than the exposed die moulded package because cracking was observed at the mould corner.

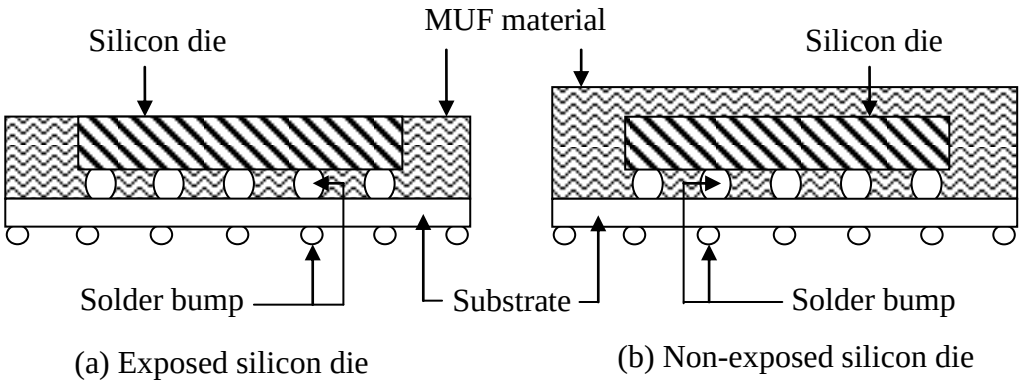


Figure 2.13: Schematic drawings of exposed-die and non-exposed-die MUF (Kooi et al, 2004).

Kao et al. (2004) studied the moulded flip-chip BGA (MFCBGA) characterization by using finite element method. The thermal and stress characteristics were taken into account in the analysis for MFCBGA and the more common FCBGA. A comparison of both packages characteristics was made. The major concerns in moulded flip-chip BGA were the high stress concentration at the silicon die from the injection pressure and the thermal stress generated as well as the mismatch between them. The thermal performance of MFCBGA was obtained in their study. The material properties with lower coefficients of thermal expansion (CTE) and higher temperature of gelation (a process of forming a gel), T_g, had resulted in lower bump and chip bending stresses for the package. In addition, the application of moulded underfill (MUF) technique in the IC packaging process yields shorter processing time and enhanced the package reliability by using MUF material. The MFCBGA process with underfill and MUF is illustrated in Figure 2.14.