EFFECT OF TETRAMETHYLAMMONIUM HYDROXIDE (TMAH) ETCHANT ON THE FORMATION OF SILICON NANOWIRES TRANSISTOR PATTERNED BY ATOMIC FORCE MICROSCOPY (AFM) LITHOGRAPHY

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UNIVERSITI SAINS MALAYSIA

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by

LEW KAM CHUNG

Thesis submitted in fulfillment of the requirement

for the degree of

Master of Science

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DECLARATION

I hereby declare that I have conducted, completed the research work and written the dissertation entitled," Effects of tetramethylammonium hydroxide (TMAH) etchant on the formation of silicon nanowires transistor patterned by atomic force microscopy (AFM) lithography". I also declare that it has not been previously submitted for the award of any degree or diploma or other similar title of this for any other examining body or university.

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Date: 5th October 2011

Witness by

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Date: 5th October 2011

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LIST OF ABBREVIATIONS

CH_3COOH	Acetic acid
AlAs	Aluminium arsenide
a-Si	Amorphous silicon
NH_4OH	Ammonium hydroxide
ASPEG	Ammonium salt of poly(ethylene glycol)
AFM	Atomic force microscope
CVD	Chemical-vapour-deposition
CMOS	Complementary metal-oxide semiconductor
c-Si	Crystalline silicon
An	Degree of etch anisotropy
DI	De-ionized
EBL	Electron beam lithography
EDX	Energy dispersive x-ray
EDP	Ethylene diamine pyrochatechol
FET	Field effect transistor
GaAs	Gallium arsenide
HDPE	High density polyethylene
HCI	Hydrochloric acid
HF	Hydrofluoric acid
H^+	Hydrogen ion
H_2O_2	Hydrogen peroxide
a-Si:H	Hydrogenated amorphous silicon
OH^-	Hydroxide ion
IPA	Isopropyl alcohol
JFET	Junction field effect transistor
LB	Langmuir-Blodgett
LED	Light emitting diode
LAO	Local anodic oxidation
MOSFET	Metal oxide semiconductor field effect transistor
MBE	Molecular beam epitaxy
HNO_3	Nitric acid
PVD	Physical vapor deposition
PEG	poly(ethylene glycol)
PTFE	Polytetrafluoroethylene
PVDF	Polyvinylidene fluoride
KOH	Potassium hydroxide
K^+	Potassium ion
RIE	Reactive ion etching
SPL	Scanning probe lithography
SPM	Scanning probe microscope
STM	Scanning tunnelling microscope
SAMs	Self-assembled monolayers

SPA	Semiconductor parameter analyzer
Si	Silicon
SiO_2	Silicon dioxide
SOI	Silicon on insulator
SiNWT	Silicon nanowire transistor
SDSS	Sodium dihexyl sulfosuccinate
TMAH,$(CH_3)_4NOH$	Tetramethyl ammonium hydroxide
TFT	Thin film transistor
3-D	Three dimensional
TiO_2	Titanium dioxide
Ti^{2+}	Titanium ion
TSNFETs	Twin silicon nanowire field effect transistor
2-D	Two dimensional
VPFESEM	Variable pressure field emission scanning electron microscope

LIST OF SYMBOLS

V_s	Applied voltage
at %	Atomic percent
V_{bi}	Built in potential
C	Celsius
I	Current
°	Degree
N_d	Dopant concentration
D	Drain
I_d	Drain current
V_d	Drain voltage
E	Electric field
eV	Electron volt
G	Gate
V_g	Gate voltage
Hz	Hertz
k	Kilo
μm	Micrometer
nm	Nanometer
nm/s	Nanometer/second
N/m	Newton/meter
Ωcm	Ohm centimeter
%	Percent
V_p	'Pinch off' voltage
R_+	Rate of ion-assisted
R_n	Rate of removal of solid material
RH	Relative humidity
s	Second
S	Source
V_{DS}	Source-drain voltage
T	Temperature
H	Thickness of the dopant
V_T	Threshold voltage
t	Time
V	Tip-sample voltage
V	Volt
V/m	Volt/meter
wt%	Weight percent

KESAN LARUTAN PUNARAN TETRAMETILAMMONIUM HIDROKSIDA (TMAH) KE ATAS PENGHASILAN TRANSISTOR SILIKON NANOWAYAR DICORAKKAN OLEH LITOGRAFI MIKROSKOP DAYA ATOMIK (AFM)

ABSTRAK

Dalam kajian ini, litografi AFM telah digunakan untuk mencorakkan struktur peranti transistor silikon nanowayar (SiNWT) daripada oksida berskala nano pada permukaan silikon atas insulator (SOI) melalui proses pengoksidaan anodik setempat (LAO). Corak oksida tersebut akan berfungsi sebagai topeng untuk melindungi lapisan silikon semasa proses pemunaran. Struktur SiNWT yang dihasilkan terdiri daripada sehelai nanowayar yang bertindak sebagai saluran dan pad-pad sentuh "source" (S), "drain" (D) dan "lateral gate" (G). Struktur peranti yang terhasil kemudian dipunar secara punaran kimia basah menggunakan tetrametilammonium hidroksida (TMAH) dan asid hidrofluorik (HF) yang bertujuan untuk menyingkirkan lapisan silikon dan lapisan oksida yang tidak diingini. Bagi litografi AFM, diperolehi bahawa voltan tip yang dikenakan 9 volt dan laju pergerakan tip semasa pencorakan 6 μm/s merupakan parameter yang terbaik untuk menghasilkan nanostruktur corak topeng peranti tersebut. Selain itu, punaran dengan TMAH pada 65°C selama 35s adalah sesuai untuk menyingkirkan lapisan silikon yang tidak diingini daripada permukaan SOI. Selepas punaran dengan HF pada suhu bilik selama 5s, peranti SiNWT dengan ketebalan saluran 99.05 nm, panjang saluran 6.92 μm dan jarak saluran ke "gate" 318.64 nm telah dihasilkan. Daripada pencirian elektrik I_d-V_d dan I_d-V_g, dapat dibuktikan bahawa peranti yang dihasilkan adalah SiNWT yang bersaluran-p.

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ABSTRACT

In this research, AFM lithography was performed to create nanoscale oxide pattern of silicon nanowires transistor (SiNWT) structure via local anodic oxidation (LAO) process on silicon on insulator (SOI) surface. These nanoscale oxide patterns will act as a mask to protect silicon layer during etching. The SiNWT structures consist of a nanowire as a channel with contact pads of source (S), drain (D) and lateral gate (G). The fabricated device structure was then wet chemically etched with tetramethylammonium hydroxide (TMAH) and hydrofluoric acid (HF) to remove the uncover silicon layer and oxide layer, respectively. Using AFM lithography, it was found that the 9 volt tip voltage and 6 μm/s tip writing speed were the most suitable parameters to fabricate nanostructure mask pattern of device. The TMAH etching at 65°C for 35s was found as the best condition to remove silicon layer completely from uncovered SOI surface. After HF etching at room temperature for 5s, the SiNWT with 99.05 nm channel thickness, 6.92 μm channel length, and 318.64 nm channel to gate gaps was fabricated. From the I_d-V_d and I_d-V_g electrical characteristic confirmed that the fabricated SiNWT is p-channel SiNWT.

CHAPTER 1

INTRODUCTION

1.1 Introduction

Nanotechnology has become one of the most promising research areas which it can bring significant progress in the development of materials and devices. Nanotechnology involves the definition, design and function of a structure in which the dimensions are measured in nanometers (Rosoft, 2002). To produce nanomaterials and nanostructures such as nanowires, nanorods, quantum dots and nanoparticles, research works have been done on the formation of these materials. To get specific nanoobjects and their properties, a particular technique should be selected.

Nanowire is a one dimensional nanostructure that has thickness, diameter or length in the range of 0.1 nanometers to 100 nanometers. Silicon nanowire is one of the nanowires that exists in the development of nanostructure or semiconductor especially for nanoelectronic device industry. Due to silicon nanowire compatible with complementary metal-oxide semiconductor (CMOS) technology, it is a very attractive material to be used as interconnection materials and basic components for nanoelectronic and optoelectronic with lower power consumption such as light emitting diode (LED) and high speed field effect transistor (FET). Nanoelectronics are applied in the nanotechnology of the electronic components especially the often

referred to transistor devices that are so small that inter-atomic interaction exist in the quantum mechanical properties (Rosoft, 2002).

At present, SiNWT has become a very interactive material in its potential to be used in the building of nanoelectronics for device industry. Silicon nanowire transistor is a FET that is operated by either electrons or holes as carriers. Transistor is the fundamental block for all the electronic devices because the number of transistors in a silicon chip had grown from a few hundred to over ten million on a single chip. SiNWT can be fabricated by top-down and bottoms-up approach which depends on its application (Salem *et al.*, 2009). Salem *et al.*, (2009) had discussed that for the improvements of the potential of its application in the integrated circuits, the bottoms-up approach provides cost-effective nanowire compared to the top-down approach. In this research, the SiNWT with nanowire used as a channel with contact pads of source (S), drain (D) and gate (G) has been fabricated by AFM nanolithography and followed by the wet chemical etching process.

1.2 Problem Statement

Since the early seventies, the number of the transistors in a silicon chip had increased from a hundred to over ten million on a single chip by today. The size of the transistor has obviously become smaller and smaller. Due to the shrinking size of the transistors, there are more and more transistors can be squeeze into a chip. Although increasing the amount of transistors into a chip will increase the

performance of the electronic device, it will also create some problems. When more transistors are put in a chip, a more complex structure will be created on the chip. The complexity of this structure is complicated and must be followed by many steps in the fabrication processes which are quite costly. Then, the amount of the transistors will also make the heat transferred into a smaller space and heat dissipation problem will happen. The SiNWT with simple structures and simple process with less complex structures and step of the fabrication processes can solve this problem. With simple structures, the electron mobility become faster and the performance of the electronic device will not be affected. Meanwhile, with the simple process, the cost of the electronic device fabrication is lower compared to the complicated fabrication processes.

There are many techniques that have been developed for SiNWT fabrication such as chemical-vapour-deposition (CVD) (Lee *et al.*, 2009; Yoon *et al.*, 2008; Salem *et al.*, 2009; Suk *et al.*, 2008), electron beam lithography (Salem *et al.*, 2009), laser induced decomposition (Salem *et al.*, 2009) and field-emission growth inducer on a scanning tunnelling microscopy tip (Salem *et al.*, 2009). These techniques are very complex and require expensive masking system. To solve these problems, the SiNWT can be fabricated by an AFM lithography followed by a wet chemical etching process. The advantages of AFM lithography for fabrication of the SiNWT are, it is a simple and it does not need an expensive masking system.

In a semiconductor industry, dry and wet chemical etching processes are used to produce nanostructured devices. Wet chemical etching process is widely used to etch silicon and silicon dioxide as the process is simple and easy to handle compared to dry etching process. Wet chemical etching of silicon dioxide is commonly done by hydrofluoric acid (HF) solutions (Williams and Muller, 1996). Potassium hydroxide (KOH) (Gwo, 2001; Biswas and Kal, 2006; Fu *et al.*, 1999) and tetramethyl ammonium hydroxide (TMAH) (Tabata *et al.*, 1992; Sonphao and Chaisirikul, 2001; Chien *et al.*, 2002; Tokoro *et al.*, 1998; Biswas and Kal, 2006) alkaline solution are commonly used for the silicon wet chemical etching process. KOH is a less-toxic, economical, with high silicon etch rate, high degree of anisotropy, low etched surface roughness and moderate Si/SiO_2 etch rate ratio. But, KOH is not CMOS compatible due to the presence of K^+ metal alkaline ions in it (Biswas and Kal, 2006; Chien *et al.*, 2002). To solve that problem, TMAH is used for SiNWT fabrication. TMAH has the advantages of being CMOS compatible, non-flammable, smooth, less harmful, have high silicon etch rate and have high selectivity in masking layers and is also less-toxic.

1.3 Research Objectives

1. To fabricate a SiNWT using AFM lithography followed by wet chemical etching process.
2. To investigate the effect of the TMAH etchant on the formation of SiNWT structures.
3. To characterize the electrical properties of the fabricated SiNWT.

1.4 Scope of the research

In this research, SiNWT was created with the nanowire as a channel that is in contact with the source (S), drain (D) and gate (G) pads. The SiNWT was fabricated by AFM lithography and followed by wet chemical etching process. AFM lithography was performed by local anodic oxidation (LAO) process. The oxide patterns grew on the chemically reactive substrate which acts as a mask by the application of a voltage between a conductive AFM tip and its substrate. There are several parameters that influence the patterning process such as tip writing speed, relative air humidity, sample voltage tip, radius tip, sample distance tip, anodization time and crystalline orientation. The tip writing speed and sample- tip voltage which most influence the process were studied in this research (Cervenka *et al.*, 2006; Mo *et al.*, 2008; Fang, 2004; Kuramochi *et al.*, 2003; Vijaykumar and Kulkarni, 2007; Umezu *et al.*, 2002; Hsu and Lee, 2008; Fang *et al.*, 2008; Held *et al.*, 1998; Hutagalung *et al.*, 2007; Fu *et al.*, 1999).

The AFM lithography can only produce the oxide pattern mask and wet chemical etching was then performed in order to produce the SiNWT. TMAH and HF acid were chosen for silicon and silicon oxide etching. TMAH is an anisotropic chemical etchant and CMOS compatible, it was used to remove the uncovered silicon layer and leave behind the oxide pattern. Meanwhile, HF acid was used to remove oxide layer. In this research, the effect of the TMAH etchant due to etching time on the constant etching temperature and concentration during the formation of the SiNWT structures was studied.

The fabricated SiNWT was observed under AFM for surface topography and dimension. The SiNWT had characterized by variable pressure field emission scanning electron microscope (VPFESEM) and EDX for the surface morphology, dimension and element measurement. For electrical characterization, the I-V electrical characteristic of the fabricated SiNWT was characterized under the semiconductor parameter analyzer (SPA) by using cryogenic probe station to investigate the electrical properties of the SiNWT structures.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Nanotechnology is a technology that involves the design, definition and function of a structure in which the dimensions are measured in nanometers. Thus, it is not limited to the dimension of the materials or devices in the nanometer size. For materials or nano-sized devices, it is in the range of 0.1 nanometers to 100 nanometers in size or dimensions. Nanotechnology is an extension of the conventional physical device to completely new approaches with self-assembly molecule rather than to develop new materials with nanoscale dimension and directly control the materials on the atomic scale. 'Nano' is derived from the Greek word meaning 'Dwarf' (Rosoft, 2002).

According to the National Science Foundation and National Nanotechnology Initiative (NNI) of the United Kingdom, nanotechnology is the ability to understand, control and manipulate matter at the level of individual atoms and molecules (in the range of about 0.1 to 100nm) in order to create materials, devices and system with fundamentally new properties and functions because of their small structure. The definition also proposed the usage the same principles and tools to establish a unifying platform for science and engineering at nanoscale, and employing the atomic and molecular interaction to develop the efficient manufacturing methods (Goddard III *et al.*, 2007).

There are two main approaches used in nanotechnology fabrication which is called as the top-down approach and bottoms-up approach. These two approaches are really used for the development of materials or devices in the nanometer size. Top-down approach is a method for materials or devices fabrication from bulk materials. This approach takes a bulk material, mechanize it or modify it to the desired shape or smaller components. So, this approach is conducted from large items to become smaller ones. Bottoms-up approach is a method to build materials or devices from the molecular component or smaller building blocks which chemically self-assemble itself. This approach is conducted from the small items to become bigger ones.

In the semiconductor industry, top-down approach and bottom-up approach are applied in the nanoelectronic device fabrication. The most common methods for top-down approach in the nanoelectronic device fabrication are electron beam lithography (EBL) (Wang *et al.*, 2006; Feste *et al.*, 2009; Koo *et al.*, 2005; Lee *et al.*, 2009b; Weber *et al.*, 2006; Salem *et al.*, 2009) and scanning probe lithography (SPL)(Martinez *et al.*, 2008).This approach involves molding or etching materials into smaller components. For bottoms-up approach, the common methods are molecular beam epitaxy (MBE), physical vapor deposition (PVD) and chemical vapor deposition (CVD).

2.2 Scanning probe microscopes (SPM)

A decade ago, scanning probe microscopes (SPMs), a molecular microscope was invented in the area of nanoscience and nanotechnology researches. The basic method of these SPMs was essentially to be able to move a tip over the substrate surface with a probe (sensor) with molecular sensitivity in the nanometer scale of the horizontal and vertical direction. The sensor movement was controlled under a highly sensitive feedback system which will then be coupled to a variety of signals to provide atomic surface details.

There are two types of the SPMs that were invented which are called as scanning tunnelling microscope (STM) and atomic force microscope (AFM). The STM was invented to characterize the surface structures for conducting materials. Due to the data from the STM images that provides information on the relative importance of molecule-molecule and molecule-substrate interaction, it is useful in such applications as microelectronic fabrication, epitaxial growth of thin films, lubrication and chromatography. Meanwhile, the AFM was developed to characterize the surface structures for non-conducting and conducting materials. The AFM is mostly used to characterize the surface of the thin film, polymer coating and single-crystal substrates. In advance, the AFM is used for nanoelectronic fabrication which happened in this research.

2.3 Atomic force microscope (AFM) lithography

Atomic force microscope (AFM) lithography has shown itself to be unique for patterning and materials structuring in the nanometer precision. As usual, the AFM is used as a microscope to directly illustrate the image on the surface topography with atomic and molecular resolution. The image of the surface is obtained by recording and regulating the force felt by a probe as it scans the surface. AFM can be used to study both insulating and conducting material, and can be operated in the liquid, vacuum or air (Xie *et al.*, 2006).

The AFM lithography works based on the principle of interaction between the probe and substrate separation in close contact condition < 1 nm. So, the AFM lithography can operate in contact mode (Fu *et al.*, 1999; Giesbers *et al.*, 2008; Kuramochi *et al.*, 2003; Hu and Hu, 2005; Kuramochi *et al.*, 2004; Park *et al.*, 2007) or noncontact mode (Hsu and Lee, 2008; Kuramochi *et al.*, 2004; Fang *et al.*, 2008; Fang, 2004; Hutagalung *et al.*, 2007). When suitable external field applied and/or forces are exerted, the probe can induce various physical and chemical processes on the substrate surface. Due to the physical and chemical processes on the substrate surface, the localized nanostructures are generated. AFM lithography possesses the versatility to pattern a wide range of materials including metals, semiconductors, polymers and biological molecules in different media. The surface topography and physical properties of the fabricated localized nanostructures can be immediately characterized with AFM (Xie *et al.*, 2006).

AFM lithography can be classified into two groups in term of their operational principles which are bias-assisted AFM lithography and force-assisted AFM lithography as shown in Figure 2.1. Bias-assisted AFM lithography is used in this project where the AFM tip is biased to create a localized electric field and the AFM tip acts as a nanoscale electrode for current injection or collection. Depending on the magnitude of the tip's biasness (positive bias or negative bias) and substrate materials, the application of the tip voltage can lead to anodic oxidation for nanostructures, nano-lines or nano-dots fabrication (Xie *et al.*, 2006).

In force-assisted AFM lithography, a large force is applied to the tip for pattern fabrication and the tip-surface interaction is mainly mechanical. During force-assisted AFM lithography, forces larger than those used for AFM imaging are loaded onto the tip. The initially featureless surface is then patterned by mechanically scratching, pushing or pulling the surface atoms and molecules with the probe (Xie *et al.*, 2006). Park *et al.*, (2007) had used force-assisted AFM lithography for the formation of the damage layer on silicon substrate by a simple scratching process using special designed diamond tip cantilever for industrial application as a micro-to-nano machining tool.

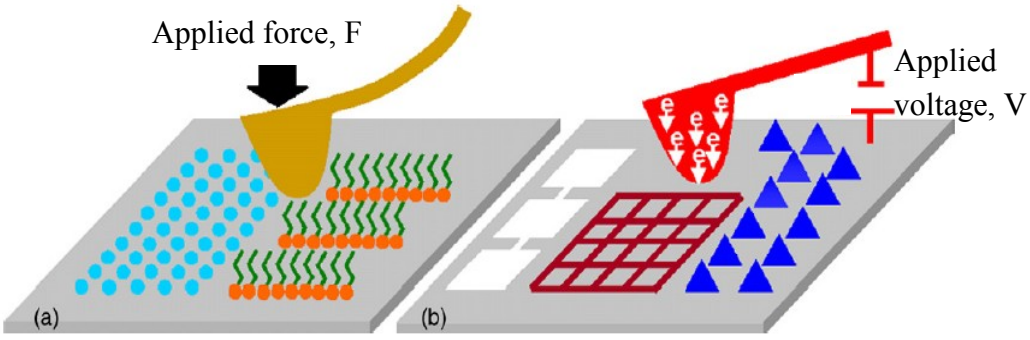

Figure 2.1: (a) Force-assisted and (b) bias-assisted AFM lithography (Xie *et al.*, 2006).

2.3.1 Bias-assisted AFM lithography

In bias-assisted AFM lithography, a bias is applied to the AFM probe to create a localized electric field in the nanometer-sized close contact tip-sample distance. The distance is usually less than a few nanometers, with applying a tip bias of several volts, an electric field of 10^8 V/m to 10^{10} V/m would be generated. Due to the high electric field, this will initiate several physical and chemical processes which make the patterning formation happen through field emission, joule heating, charge injection, explosive discharge, electrostatic attraction and electrochemical reaction. During the patterning formation, the process involved is ion solvation and mobility on the substrate surface. Ionic motion in liquid range from a few seconds to fractions of a millisecond and ions at the surface of materials are natural nucleation sites in absorbing water. Solvation increases the ionic mobility, and this is reflected in their response to the electric field around the tip (Rosoft, 2002). There are various technique of the bias-assisted AFM lithography such as anodic oxidation, electrochemical modification and functionalization of molecules, electrochemical deposition, charge deposition and manipulation, and nanoexplosion and shock wave generation (Xie *et al.*, 2006). The bias-assisted AFM lithography with anodic oxidation technique is then reviewed.

2.3.2 Principle of AFM lithography by local anodic oxidation (LAO)

In the local anodic oxidation (LAO) technique as shown in Figure 2.2, oxide will grow on a chemically reactive substrate by the application of a voltage or bias

between a conductive AFM tip and a substrate surface which act as an anode. There was a threshold voltage at which the anodic oxidation started. The water molecules are adsorbed onto a substrate that is dissociated due to high electric field ($E > 10^7$ V/m) which is generated by applying several volts at a few nanometer tip-substrate surface distance into fragments (e.g. H^+, OH^- and O^{2-}) and acted as an electrolyte. Oxygen containing radicals will then contribute to the formation of surface oxides due to an electric field enhanced diffusion through the oxide layer (Cervenka *et al.*, 2006).

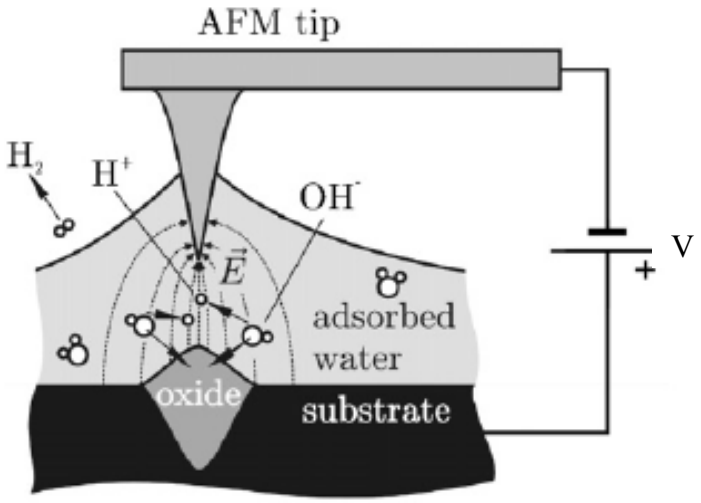

Figure 2.2: Schematic view of local anodic oxidation process induced by AFM tip (Cervenka *et al.*, 2006).

Xie *et al.*, (2006) proposed that in the LAO technique, the water meniscus formed in the tip-sample gap which is dissociated by the negative tip bias, and the O^- and OH^- oxidative ions that reacts with the substrate to form localized oxide nanostructures. Because the molecular volume of the oxide is usually larger than that of the substrate material, raised nanopatterns are formed after the oxidation reaction.

Held *et al.*, (1998) reported that LAO is usually carried out by placing the sample in an electrolytic cell and the water is used as the electrolyte. The conductive AFM tip is used as applied bias either as a constant voltage or current source. The AFM tip acts as a cathodically biased electrode to the sample surface, while the contamination layer between the tip and sample acts as an electrolyte producing this chemical reaction. So, the oxide patterns can be inspected immediately after the writing process. The water film is very important because it plays the primary role in forming the oxides.

Gwo, (2001) has discussed that the LAO process happened where a positive sample bias is applied between the sample and the grounded tip of the probe. The electrolysis of the water meniscus is formed by the capillary force between the tip (cathode) and the humidity absorbed sample surface (anode) that supplies the necessary oxidant anions (mainly OH^- ions). The applied sample bias also provides the strong electric field for ion migration into the sample.

Fang, (2004) reported that the LAO process on the specimen's surface will occur directly below the AFM probe tip when a negative bias voltage is applied to the probe. There is an adsorbed water layer on the surface, which provides the required electrolyte under the ambient conditions. Under the AFM tip as a cathode, the specimen's surface will be oxidized and the ions (including OH^- and O^{2-}) that contributes to the formation of the surface oxide and finally the nanooxidized structure will be made.

2.3.3 Oxide nanostructures fabricated by AFM-based local anodic oxidation (LAO) technique

AFM-based local anodic oxidation has been applied to produce oxide structures on semiconductors, metals and other materials. Although LAO process happened by applying the voltage between the AFM tip and the substrate surface, the fabricated oxide structure depends on the substrate materials because different substrate materials will provide different properties of the oxide structures (Xie *et al.*, 2006).

The AFM-based LAO process is mostly applied to produce oxide structure on semiconductors especially onto silicon surface (Cervenka *et al.*, 2006; Calleja *et al.*, 1999; Blasco *et al.*, 2001; Vijaykumar and Kulkarni, 2007; Hu and Hu, 2005; Fang, 2004; Kuramochi *et al.*, 2003; Fu *et al.*, 1999; Palasantzas *et al.*, 1999; Luo *et al.*, 2006) or H-passivated silicon surface (Mo *et al.*, 2008; Kuramochi *et al.*, 2004) for micro/nano-devices (Palasantzas *et al.*, 1999; Mo *et al.*, 2008) or nanoimprinting mould fabrication (Luo *et al.*, 2006). Umezu *et al.*, (2002) has reported that the height and width of the oxides on the amorphous silicon surface are larger compared to crystalline silicon when LAO technique is applied to the crystalline silicon and amorphous silicon. So, the microstructure of the silicon surface affects the oxide nanostructures fabrication. Equation (2.1) shows the chemical reaction between the silicon surface and water. Hu and Hu, (2005) proposed the chemical reaction by LAO on silicon surface as shown in Equation (2.2), where the OH^- is ionization on a few nanometers of water film on the silicon surface.

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ \quad (2.1)$$

$$Si + 2OH^- \rightarrow SiO_2 + 2H^+ \quad (2.2)$$

Then, the AFM-based LAO process is also applied to produce oxide nanostructure on silicon nitride thin film on silicon substrate. The reaction of the LAO process on the silicon nitride thin film is the same with the reaction to produce oxide nanostructure on the silicon surface but the oxidation rate is extremely fast compare to the silicon surface. So, the silicon nitride thin film functions as a tool to increase the oxidation rate of the LAO process (Hsu and Lee, 2008; Gwo, 2001). Cervenka *et al.*, (2006) have discussed that during the LAO process to produce oxide line on GaAs and silicon surface, the oxide line fabricated on the GaAs surface are generally less developed.

Besides that, the oxidized nanostructures are grown onto the titanium thin film which have been deposited on the silicon substrate (Fang *et al.*, 2008; Kim *et al.*, 2008) or GaAs (Held *et al.*, 1998) substrate by the LAO process. Fang *et al.*, (2008) have studied the fabrication of the titanium dots and wires using amplitude modulation AFM-based LAO process. Held *et al.*, (1998) reported that the oxide lines are able to be fabricated on the titanium films with excellent electronic properties. Kim *et al.*, (2008) had investigated the influence of voltage waveform in AFM-based LAO process on titanium by analysing the current behaviour and the morphology of fabricated oxide nanodots features. The chemical reactions leading to anodic oxidation of titanium happened when ions OH^- and ions Ti^{2+} migrated through the oxide, driven by the potential drop and are combined to form a rather

unstable $Ti(OH)_2$ and finally form TiO_2 as shown in Equation (2.3) (Held *et al.*, 1998).

$$Ti(OH)_2 \rightarrow TiO_2 + H_2 \quad (2.3)$$

Lazzarino *et al.*, (2006) have studied the chemical properties of LAO oxide nanostructures that's fabricated on layered GaAs/AlAs/GaAs heterostructures and the result showed that the aluminium compound present in the oxide nanostructure. Giesbers *et al.*, (2008) reported that the AFM-based LAO process was also applied to fabricate the oxide nanostructure on the graphene surface. It showed that isolating trenches oxide nanostructure is able to be fabricated on the single layer and few layer graphene flakes, which enables the possibility for the fabrication of table top graphene based device. Lee *et al.*, (2003) has fabricated predesigned antidot arrays with feature sizes of 70 nm (width) x 10 nm (height) on various materials including aluminium, titanium and silicon using AFM-based LAO process and selective wet etching technique.

Lee *et al.*, (2004) proposed that the AFM-based LAO process are applied to produce oxide nanostructures on various organized molecular films as a resist like self-assembled monolayers (SAMs), Langmuir-Blodgett (LB) films and spin-coated polymer films which is deposited onto the silicon substrate. The functional groups of self-assembled molecules for SAMs can affect the AFM lithography speed, so choosing the right functional groups is very important. For LB films, the result showed that oxide nanostructures started to grow at the point of degradation that

resist in AFM-based LAO process. Due to thermal stable and more resistant to etching solution of the polymer films compare to organic self-assembled layers, so polymer resist is suitable for oxide nanostructures fabrication.

2.3.4 Parameters that influenced the AFM-based on LAO technique

AFM-based LAO process is actually influenced by several parameters such as tip writing speed, relative air humidity, tip sample voltage, tip radius, tip sample distance, anodization time and crystalline orientation (Cervenka *et al.*, 2006; Mo *et al.*, 2008; Fang, 2004; Kuramochi *et al.*, 2003; Vijaykumar and Kulkarni, 2007; Umezu *et al.*, 2002; Hsu and Lee, 2008; Fang *et al.*, 2008; Held *et al.*, 1998).

2.3.4.1 Tip writing speed

In Figure 2.6, Cervenka *et al.*, (2006) has studied the silicon nanolines prepared at different tip sample voltages and writing speeds on Si (100) substrate. The nanolines are fabricated under a relative humidity of 46% and a temperature of 23°C. Going from left to right, the lines are prepared at progressively increasing writing speeds. On the other hand, the lines are grown at a progressively increasing tip sample voltages when going from bottom to top. From Figure 2.3, at constant tip sample voltage, the oxide lines will be less developed with increasing writing speeds. It is obvious that the lines prepared at the highest tip sample voltage and the lowest writing speed (top-left) is the best developed one in height and width. Then, it is less

developed when the lines prepared are at the lowest tip sample voltage and the highest writing speed (bottom-right). In Figure 2.4, the height of silicon oxide lines was inversely proportional to the logarithm of the tip writing speed for the 6 volt and 8 volt tip sample voltage.

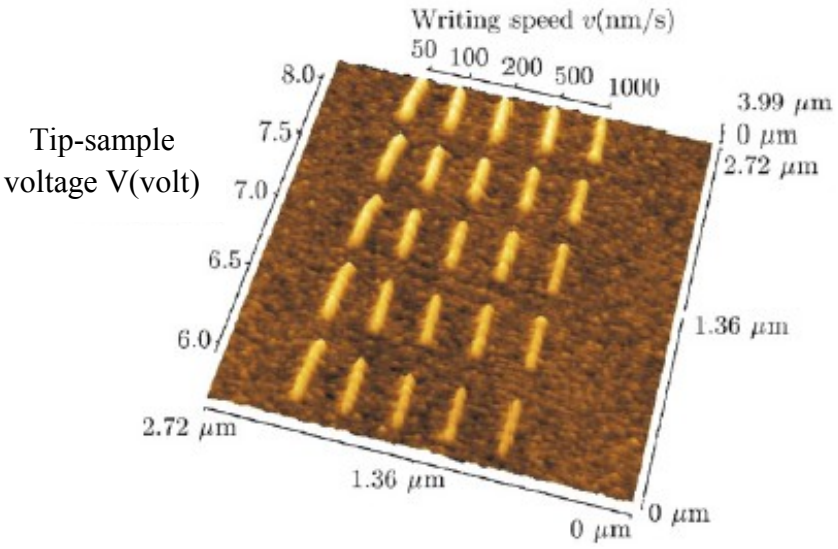

Figure 2.3: Si nanolines prepared at different tip sample voltages and writing speeds on a Si (100) substrate (relative humidity = 46%; T= 23°C) (Cervenka *et al.*, 2006).

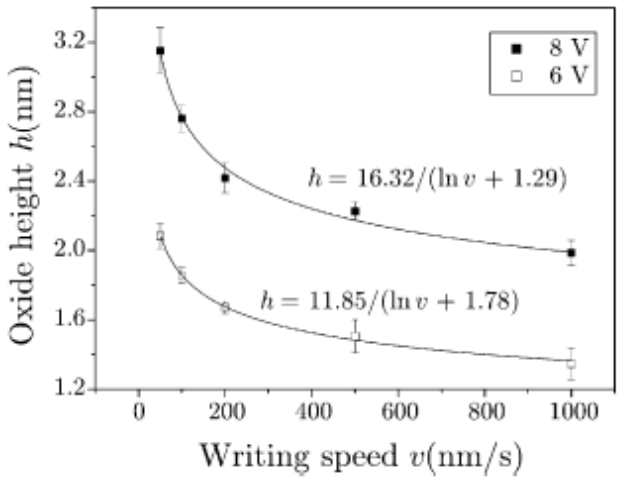

Figure 2.4: The height of Si oxide lines as a function of tip writing speed for two tip sample voltages (relative humidity = 46%; T= 23°C) (Cervenka *et al.*, 2006).

Kuramochi *et al.*, (2003) have studied the effect of the tip writing speed at a variation of relative humidity in the range of 40% to 80%. The size of the silicon oxide lines were reduced from 3 nm to 0.1 nm when the tip writing speed increased from 400 nm/s to 1200 nm/s at a variation of relative humidity (Kuramochi *et al.*, 2003).

Fang *et al.*, (2008) have reported the effect of the tip writing speed during the titanium oxide nanowire fabrication by LAO process. The oxide nanowires generated applied voltages of 7, 8, 9, and 10 volt at tip writing speed of 2 μm/s, 5 μm/s and 7 μm/s. It is obvious that the heights and widths of oxide nanowires are affected by the tip writing speed due to the applied voltage. When the tip speed is lowered, 2 μm/s was used to induce the oxide and the nanowires with a higher height and width are achived. On the other hand, nanowires with a lower height and width are fabricated when a higher tip speed, 7 μm/s with same voltage is used to induce the oxide (Fang *et al.*, 2008).

2.3.4.2 Relative air humidity

Held *et al.*, (1998) have studied the effect of the relative air humidity during the oxide nanostructures fabrication at titanium film. Figure 2.5 showed the relationship between the FWHM oxide line width and relative humidity due to the applied voltage of -5.5 volt. It was observed that the line width scales is linear with the humidity. The FWHM oxide with 50 nm width had been produced when the

oxidation happened at 30% relative humidity and the oxidation was impossible below a relative humidity of 25% (Held *et al.*, 1998).

The air humidity was influenced by the height and width of the oxide nanowires which was reported by Fang, (2004). It was obvious that as the humidity increased, the height and width of the oxide nanowires also increased. The lateral and vertical dimension of the oxide nanowires have a direct relationship to the amount of induced humidity. This is due to the electric field effect that initiates the oxide mechanism, as the humidity increased, the electrochemical interaction between the tip and the surface becomes stronger (Fang, 2004).

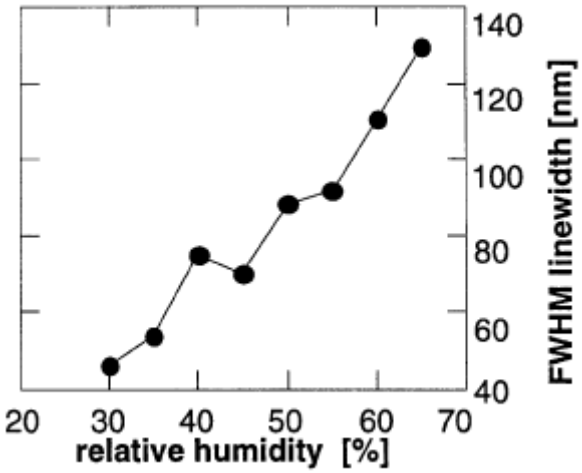

Figure 2.5: FWHM oxide line width as a function of relative humidity at applied voltage of -5.5 volt (Held *et al.*, 1998).

Kuramochi *et al.*, (2003) have studied the effect of the humidity on the fabricated oxide dots shaped according to the applied voltage, V_s, exposure time, t, and relative humidity, RH. Figure 2.6 shows the topographic images and line profile

of the fabricated oxide dots at the same applied voltage and exposure time with different relative humidity of 50% and 80%. It is observed that the height of the oxide dots was increased from 3.55 nm to 5.38 nm when the relative humidity is increased from 50% to 80%. From the topographic images, when the relative humidity was increased, the fabricated dot became "two-storied shape" with a broad base and a narrow upper half. This is due to the space charge effect and ionic diffusion through the surface water layer (Kuramochi *et al.*, 2003).

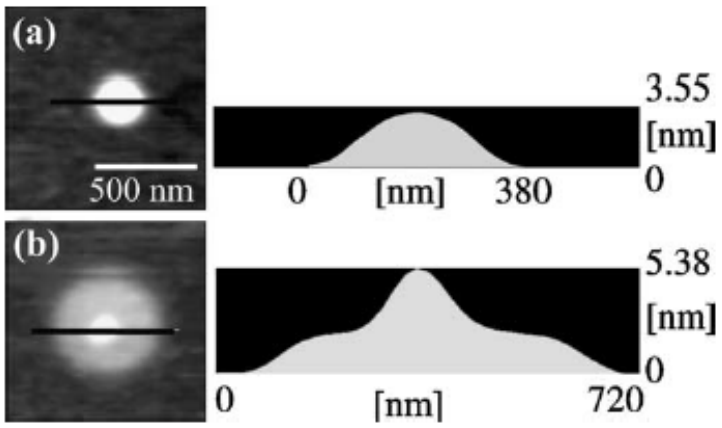

Figure 2.6: Topographic images and line profile of fabricated oxide dots. (a) V_s= 8 volt, t= 100 s , RH =50% and (b) V_s=8 volt, t= 100s , RH =80% (Kuramochi *et al.*, 2003).

Figure 2.7 shows the variation in height of the oxide protrusions fabricated by applying various voltages at low relative humidity (30-50%) and high relative humidity (60-70%). For low and high relative humidity, it is obvious that the height of the oxide protrusions increased as relative humidity increased for the applied low voltages. Hsu and Lee, (2008) have discussed that when high voltages applied, the saturation height oxide protrusions were generated for the low and high relative

humidity which was about 4.05 nm and 3.75 nm. This behaviour suggested that a space charge is build up to hinder the oxyanions diffusing in the oxide.

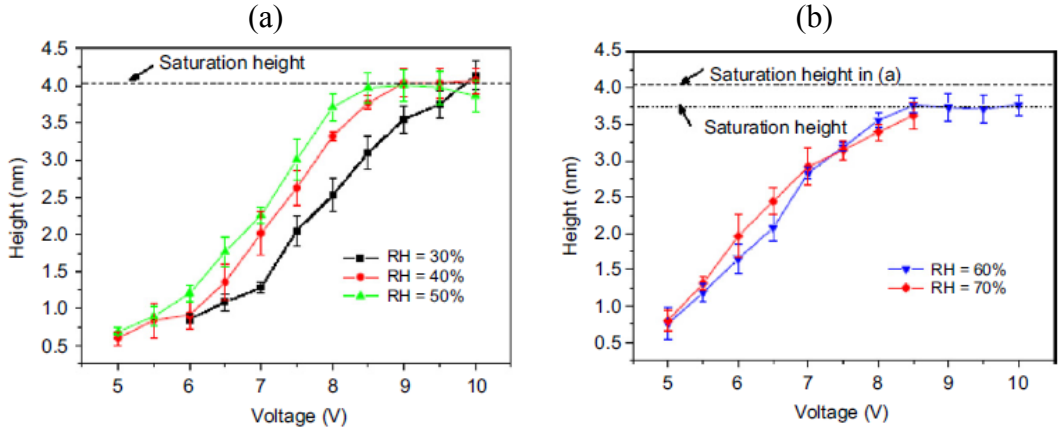

Figure 2.7: Relation between sample voltage and height at (a) low relative humidity (30-50%) and (b) high relative humidity (60-70%) (Hsu and Lee, 2008).

2.3.4.3 Tip sample voltage

Cervenka *et al.*, (2006) discussed on the effect of the tip sample voltages to produce the silicon oxide line for two different writing speeds (50 nm/s and 500 nm/s) at a relative humidity of 46% and a temperature of 23°C. It is obvious that the height of the silicon oxide lines showed a linear relationship due to the applied tip sample voltages and the smallest height of 1.5 nm was achieved at a tip sample voltage of 6 volt and a tip writing speed of 500 nm/s.

Fang *et al.*, (2008) proposed that the applied voltages are one of the important factors that affect the growth of dots and lines during LAO process. Figure 2.8 shows the relationships between the growth rate and the oxide height of the oxide nanodots

at the static voltages of 7, 8, 9, and 10 volt. It can be observed that the larger the oxide height, the slower the growth rate. The applied voltages were proportional to the growth rate of the oxide height.

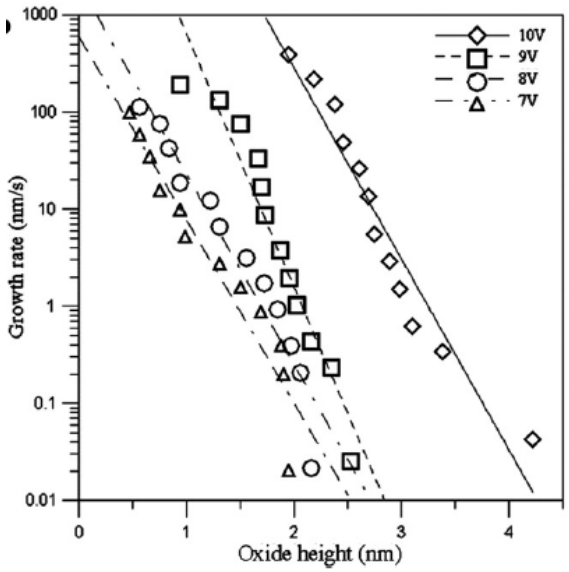

Figure 2.8: The growth rate of the oxide nanodots under different oxide heights by applied voltages of 7, 8, 9 and 10 volt (Fang *et al.*, 2008).

Hsu and Lee, (2008) reported the effect of the various sample voltages ranging from 5 volt to 10 volt on oxide protrusions shaped at a relative humidity of 70%. From the topographic image and cross-section profiles in Figure 2.9, the height and width of the oxide protrusions are also increased as the applied voltages increased from 5 volt to 10 volt. The topographic image showed that the oxide protrusions are in simple dome shaped at low sample voltages (≤ 8.5 volt). At high sample voltages (≥ 9 volt), the oxide protrusions shapes are "two-storied shape" because the fabricated oxide protrusions had a narrow peak at the center and a broad base. The formation of the "two-storied shape" oxide protrusions is due to the high