SIMULTANEOUS SWITCHING NOISE IMPACT TO SIGNAL SENSITIVITY ON USB 2.0

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SIMULTANEOUS SWITCHING NOISE IMPACT TO SIGNAL SENSITIVITY ON USB 2.0

by

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DECLARATION

I hereby declare that this work has been done by myself and no portion of the work contained in this report has been submitted in support of any application for any other degree or qualification of this or any other university or institute of learning.

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TABLE OF CONTENTS

CHAPTER 2 – BACKGROUND REVIEW

CHAPTER 3 – PROJECT METHODOLOGY

CHAPTER 4 – RESULTS AND DISCUSSIONS

LIST OF TABLES

Page

LIST OF FIGURES

Page

LIST OF PLATES

Page

LIST OF ABBREVIATIONS

AC	Alternating Current
BC	On-board Capacitor
BER	Bit Error Rate
BGA	Ball Grid Array
BSC	Back-Side Capacitor
Cdie	On-die Capacitor
DC	Direct Current
DJ	Deterministic Jitter
DSC	Die-Side Capacitor (On-package Capacitor)
DUT	Device under Test
EC	Edge Capacitor
ESL	Equivalent Series Inductance
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
FIB	Focused Ion Beam
FIR	Finite Impulse Response
ISI	Inter-symbol Interference
ITP II	Intel In-target Probe
LSC	Land-Side Capacitor
PCB	Printed Circuit board
PDN	Power Distribution Network
PLL	Phase-Locked Loops
PTH	Plated Through-Hole
PWL	Piecewise Linear Source
PWM	Pulse-width Modulation
RC	Resistance and Capacitance
RJ	Random jitter

RLGC	Resistance, Inductance, Conductance, Capacitance
SIPI	Signal Integrity & Power Integrity
SSN	Simultaneous Switching Noise
STV	Silicon Through-via
USB	Universal Serial Bus
VRM	Voltage Regulator Module

LIST OF SYMBOLS

A	Area of overlapping plates
C	Capacitance
d	Separation between plates
D_+	Positive signal from differential signal pair
D_-	Negative signal from differential signal pair
ε_o	Electric constant
ε_γ	Relative static permittivity
I	Current
I_{cc}	Current profile
$\mathrm{I}_{cc}(f)$	Current profile in frequency domain
L	Inductance
R	Resistance
t_d	Propagation delay of transmission line
V	Voltage
V_{ACN}	AC supply voltage
V_{out}	Output voltage
V_p	Wave velocity of transmission line
V_{VRM}	Input voltage from voltage regulator
ω_o	Resonance Frequency
$Z(f)$	Impedance profile in frequency domain
Z_{in}	Input impedance
Z_L	Load impedance
Z_o	Characteristic impedance of transmission line
Γ	Reflection coefficient

KESAN HINGAR PENSUISAN SERENTAK
KEPADA KEPEKAAN ISYARAT BAGI USB 2.0

ABSTRAK

Hingar pensuisan serentak (SSN) meningkat dengan kadar data I/O yang lebih tinggi menyebabkan kawal selia voltan bekalan dalam litar transistor menjadi satu cabaran. Voltan bekalan berubah sewajarnya mengikut rekabentuk rangkaian agihan kuasa (PDN). Usaha-usaha kejuruteraan lazimnya tertumpu kepada bentangan PDN bagi mengurangkan laluan galangan. Walau bagaimanapun, hasrat untuk mengecilkan saiz komponen suatu sistem telah memberi cabaran dalam menghasilkan rekabentuk PDN yang lebih komprehensif terutamanya dalam mengawal kejatuhan voltan. Oleh itu, kajian berhubung kesan hingar bekalan terhadap prestasi isyarat adalah diperlukan dalam rekabentuk PDN pada masa hadapan. Selain daripada mengoptimumkan PDN, cara yang lain dalam mengukur kesan frekuensi voltan bekalan yang berbeza terhadap isyarat keluaran diperkenalkan dalam kajian ini. Prestasi isyarat pemancar litar bas sesiri semesta (USB) diteroka dalam usaha untuk mengkaji hubungan ini. Isyarat gambarajah mata diperiksa selepas menggantikan voltan bekalan DC dengan pelbagai frekuensi voltan bekalan AC. Berdasarkan pemerhatian kepada hasil simulasi, pemancar USB mempunyai ketahanan yang lebih baik terhadap hingar bekalan pada frekuensi operasi 480 MHz dan juga frekuensi-frekuensi harmonik 960 MHz dan 1.44 GHz. Hingar bekalan berlebihan pada frekuensi-frekuensi ini tidak menyebabkan kegagalan kepada gambarajah mata. Penemuan ini dibuktikan lagi melalui pengukuran makmal. Gambarajah mata diukur bagi kes-kes tekanan pensuisan serentak yang berbeza. Voltan bekalan diukur dan dianalisis dengan menggunakan

kaedah jelmaan Fourier pantas (FFT) bagi mengenalpasti penyumbang frekuensi yang utama dalam profil hingar. Isyarat I/O daripada hasil pengukuran menunjukkan prestasi yang lebih baik terutamanya apabila hingar bekalan yang diukur berada dalam kawasan frekuensi 480 MHz dan 960 MHz. Hingar bekalan berbanding gambarajah mata diperhatikan dengan menggabungkan kedua-dua model integriti kuasa dan integriti isyarat dalam simulasi transistor USB. Satu cara yang berbeza untuk merekabentuk PDN diperkenalkan dengan membuang pemuat nyahgandingan atas acuan (Cdie). Daripada analisis, walaupun hingar AC yang berlebihan diaruh di dalam rel bekalan (selepas dibuang Cdie), isyarat tersimulasi masih lulus dalam ujian gambarajah mata. Berdasarkan kajian ini, kawasan silikon boleh dikurangkan lagi sebanyak 10% - 20% dengan mengeluarkan Cdie, yang mana ianya akan menyediakan lebih fleksibiliti dalam rekabentuk silikon. Kajian ini menyimpulkan bahawa USB menpunyai sensitiviti yang berbeza bagi frekuensi hingar bekalan yang berbeza. Di samping itu, penyingkiran Cdie boleh dilaksanakan selepas disahkan melalui simulasi transistor USB, bersama-sama dengan model integriti isyarat dan integriti kuasa.

SIMULTANEOUS SWITCHING NOISE

IMPACT TO SIGNAL SENSITIVITY ON USB 2.0

ABSTRACT

Simultaneous Switching Noise (SSN) is increasing with higher I/O data rate, resulting into challenges for regulating supply voltage in typical transistor circuit. Supply voltage changes accordingly with Power Distribution Network (PDN) design. Engineering efforts are focused on PDN layout to minimize the impedance path. However, the desire to miniaturize components on a system increases design challenges to control voltage drop via comprehensive PDN design. Hence, it is a need to study the impact of supply noise to signal performance in future PDN design. Instead of optimizing PDN, a different way of quantifying different frequency supply voltage impact to output signal is introduced in this research. In order to observe this relationship, Universal Serial Bus (USB) transmitter circuit signal performance is explored. Signal eye diagram is observed by replacing DC input voltage with various frequencies of AC input voltage. From the simulation, USB transmitter has better immunity to the supply noise at its operating frequency of 480 MHz, and also its harmonic frequencies of 960 MHz and 1.44 GHz. Excessive amount of supply noises at these frequencies are not causing signal eye diagram to fail. This finding is further verified by lab measurement. Eye diagram is measured by different simultaneous switching stress test cases. The supply voltage is captured and analyzed using Fast Fourier Transform (FFT) to identify the major frequency contributors in the noise profile. From the measurement result, signal has better performance especially when the measured supply noise falls in the frequency regions of 480 MHz and 960 MHz. Consequently, supply noise versus eye diagram

is observed by including both power integrity and signal integrity model in USB transistor simulation. A different way of designing PDN is proposed by removing on-die decoupling capacitor (Cdie). From analysis, although excessive AC noise is induced in the supply rail after removing Cdie, the simulated signal passes the eye diagram compliance requirement. Based on this finding, silicon area can be reduced by 10% to 20% after removing Cdie, which provides better flexibility in silicon design. This research concludes that USB has different sensitivity to different frequency of supply noise. In addition, Cdie removal can be implemented, which is verified by USB transistor level simulation, together with signal integrity and power integrity models.

CHAPTER 1

INTRODUCTION

1.1 Overview

Transistor size shrinks every generation to obtain higher data rate and clock speed. Operating voltage is scaled down, trending toward low power consumption in line with transistor's size reduction. Supply voltage's design target is tightening because of lower supply noise margin, after scaling down the operating voltage.

In contrary with supply noise margin, most chipmakers desire to increase the number of I/O in every new generation chip to accommodate higher user needs. Design engineers constantly need to keep pace with higher design complexity with I/O current drawn increase, which in turn will induce higher Simultaneous Switching Noise (SSN) on a given interconnect. Interconnect parasitic such as resistance and inductance contribute to non-ideal supply voltage characteristic. Resistance increase DC IR drop and lowering nominal voltage; while inductance induces AC voltage fluctuation when interacting with transient current of the operating I/O (Kumar *et al.*, 2010). The amount of DC voltage drop and AC voltage fluctuation increases when multiple circuits draw current from the same power supply rail. This voltage noise is interpreted as SSN which directly impact circuit performance in timing and signal quality.

In order to reduce SSN resulted from supply voltage drop, Power Distribution Network (PDN) has to be designed optimally. PDN consists of supply voltage routing from voltage regulator on board into transistor circuit on die. It is optimized by reducing effective resistance and inductance of the routing. Ideally,

PDN routing is implemented with larger width and area to reduce the overall resistance and inductance path. Moving ground plane next to a power plane also provides good return path referencing.

At the same time, signal performance is analyzed apart with power delivery. Analysis for signal performance considers only DC voltage change in typical cases. However, supply voltage changes with time due to non-ideal characteristic of PDN. Supply voltage varies in time domain with the function of inductance, current amplitude and its slew rate. The variation of supply voltage is amplified especially when multiple current travel through high inductance path of power supply rail (Mikhail, 2007). Thus, running signal analysis without consider PDN is insufficient to model the impact of input voltage to output signal. Design mismatch might occur due to lack of correlation between PDN model and signal model.

Moreover, silicon and package size shrink is reducing resources available to both signal integrity and power integrity design (Mikhail, 2007). Continuously suppressing the supply noise by optimizing PDN is not an effective design. Extra resources are required to design PDN, which in turn lead to larger silicon and package size. Furthermore, extra decoupling capacitors are placed on silicon, package and board to meet the AC voltage droop design target. It defeats the purpose of shrinking transistor size to acquire better circuit performance.

Hence, PDN design should be correlated with signal performance. Forcing PDN design to meet the target impedance criteria at all frequencies is not applicable in chipset I/O design. Signal sensitivity to supply noise is the parameter to investigate because it is the key to determine the performance of I/O. In this research, Universal Serial Bus 2.0 (USB 2.0) is used as high speed I/O to be studied.

1.2 Problem Statement

Supply noise budget is scaled inversely proportional to the I/O data rate. Voltage noise margin allowed for integrated circuit becomes tighter as data rate increases with generation. Design challenge for PDN increases in this competitive electronic product market. User is looking for cheaper and multifunction product instead of higher performance CPU. Electronic manufacturer reduces the cost to design and manufacture to enable product affordable by end user.

Therefore, resources available in designing PDN reduced significantly. Silicon size, package size, and number of decoupling capacitors are the resources to design a PDN. Silicon size and package size reduction directly increase the resistance and inductance path of voltage routing. Decoupling capacitors are removed due to process or area limitation. Supply voltage droop varies proportional to resistance, inductance and current drawn from integrated circuit. The design goal for PDN is to maintain impedance as low as possible. Excessive supply noise will be induced whenever PDN impedance is not controlled (Priest *et al.*, 2009).

By foreseeing the limitation in PDN design, power integrity design by optimizing through PDN without looking into output signal resulted by the supply noise is insufficient. Correlation between power integrity and signal integrity is needed as both designs are impacting each other in the circuit operation. Instead of suppressing noise with limited resources in PDN, supply noise impact to signal performance should be further explored.

1.3 Research Objectives

The main objectives of this research are:

(i) To investigate the impact of SSN at possible frequency range to signal performance by using USB.

(ii) To measure and correlate the supply noise with signal performance using existing USB chipset.

(iii) To develop the way of integrating power integrity model and signal integrity model together with transistor level circuit by using USB.

(iv) To exploit the possible PDN design method for USB by conducting signal sensitivity analysis.

1.4 Research Scopes

This research will focus on the following scopes:

(i) Obtain signal integrity channel model and connect with the USB transmitter in transistor level simulation.

(ii) Inject supply voltage in sinusoidal waveform, from low frequency to high frequency and observe the changes in signal eye diagram.

(iii) Compare the difference between input DC voltage and input AC voltage to signal eye diagram.

(iv) Measure SSN with existing USB chipset by enabling all the USB through different methods and inspect the eye diagram resulted from the SSN.

(v) Connect PDN with previous USB transmitter circuit to form a complete circuit model.

(vi) Maximize SSN in simulation by enabling 14 USB transmitters while examine the supply noise and eye diagram changes.

(vii) Explore the possible way of designing PDN based on summarized signal sensitivity analysis through early simulation and measurement.

1.5 Research Target Contribution

In this research, a method of combining power integrity and signal integrity model together into transistor level circuit simulation is going to be introduced. Typical power integrity and signal integrity analyses are carried out separately. By combining both models together with transistor level circuit, it has the highest accuracy by compensating the simulation time. Direct impact of supply noise to signal performance can be observed in the simulation.

Besides, this research aims to verify signal has distinct sensitivity level to different frequencies of noise. Signal sensitivity will be studied in both simulation and measurement. Once signal sensitivity to supply noise is known, PDN design can be changed and manipulated by focusing only to specific frequency regions. A better way of designing PDN is targeted; which reduce the size of silicon or packaging. It may save manufacturing cost and provide more spaces to accommodate extra circuitry for better functionality.

1.6 Overall Research Flow

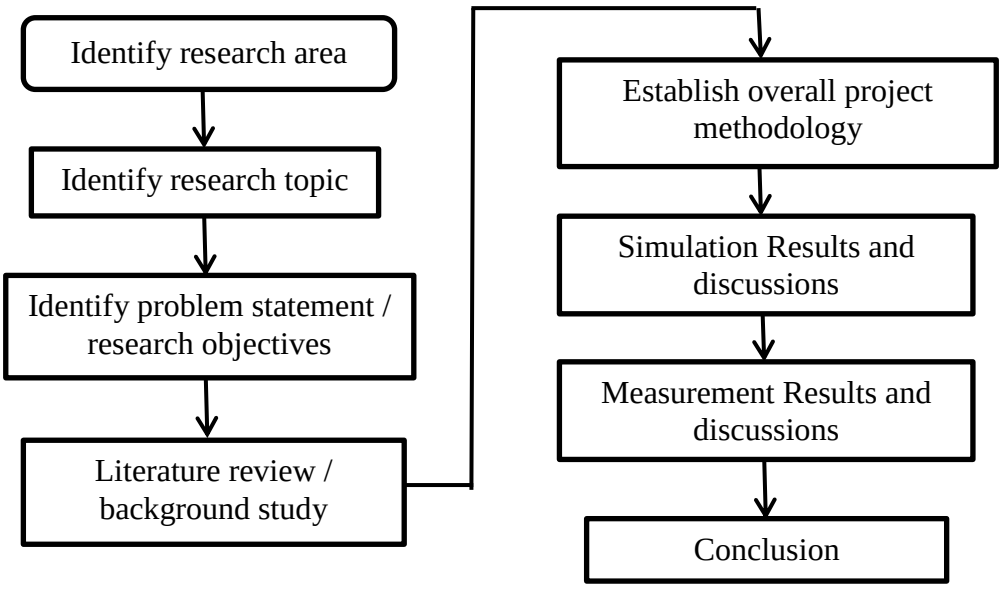

Figure 1.1: Overall research flowchart

As shown in Figure 1.1, the overall research starts with identifying research area, which is decided to focus in power integrity. Next, topic is chosen as Simultaneous Switching Noise Impact to Signal Sensitivity on High Speed I/O. Problem statements and research objective are scoped based on project title and area of interest.

Next, project continues with literature review according to previous researches. Background review and comparison study is done in power integrity and signal integrity related researches. After literature review, project methodology flow is established. Simulation and measurement test cases are determined accordingly.

After project methodology flow is setup, results are collected from simulation and measurement. Discussion is elaborated based on the results extracted. Finally, research ends by concluding the overall project results and outcomes.

1.7 Thesis Outline

The overall thesis consists of five chapters. Chapter one introduces the background and the problem statement. Other than that, the objectives, scopes and contributions of this research are stated.

Chapter two elaborates the background review on power integrity and signal integrity. PDN induces supply noise is introduced in this section and ways to improve power integrity are discussed. Besides, signal transmission line results channel losses and ways to enhance signal integrity are illustrated.

Chapter three demonstrates the methodology to carry out this research. It includes the simulation setup and measurement setup to obtain supply noise together with signal eye diagram. Furthermore, research limitations in simulation and measurement are discussed in this section.

Chapter four presents the results and discussions. Simulation results using SPICE together with measurement data are displayed in this section. Signal sensitivity to supply noise is disclosed. By referring to signal sensitivity study, a new way of designing PDN is introduced.

Finally, chapter five concludes this research and future recommendations are suggested.

CHAPTER 2

BACKGROUND REVIEW

2.1 Introduction

Current product is trending toward higher data rate but lower power consumption for battery efficiency. Low supply voltage and low current drawn are designed to meet low power consumption requirement. Input supply voltage is scaled down together with transistor sizing to increase speed and efficiency. In high speed device, digital signal slowly lose its advantage over analog signal. Transistor drive strength reduces significantly due to voltage decrement; results into weak signal transmission. Signal distortion happens in transmission line because the signal strength is not strong enough to transfer through transmission line. Moreover, supply voltage droop and channel losses are interrupting the operation of typical I/O signal transmission (Choi *et al.*, 2008). In order to control supply voltage noise and signal losses, power integrity (Wang *et al.*, 2010; Nabeshima *et al.*, 2011) and signal integrity (Shen *et al.*, 2008; Huang *et al.*, 2010) are playing important roles.

2.2 Power Integrity

Power integrity (PI) (Thierauf, 2011) is the parameter to determine the quality of supply voltage going into integrated circuit. In high speed digital circuit, supplying a clean voltage is important to drive and operate the transistor circuit. Excessive noise in supply voltage will induce extra jitter in sensitive circuit such as Phase-Locked Loops (PLL) (Chan *et al.*, 2007). I/O is unable to transmit and receive

signal at the desired signal rate whenever timing disturbance happens in clock circuitry. Moreover, supply noise will further reduce the transmitted signal strength and decrease the eye margin of signal (Choi *et al.*, 2008).

Supply noise increases significantly especially when the data rate and number of devices continue to increase throughout generation to accommodate user needs. It results into challenge in power integrity due to SSN appears in wide bandwidth for high speed digital circuit. Reducing impedance in PDN becomes a major task in power integrity design to reduce the overall noise; specifically at resonance of PDN. Decoupling capacitors are widely used on package and silicon to lower down the effective impedance of PDN and reduce the SSN in typical I/O circuit (Okumura *et al.*, 2010).

2.2.1 Power Distribution Network (PDN)

Figure 2.1 shows one of the examples to model PDN for typical chipset (Mahajan *et al.*, 2004). In chipset family, PDN is analyzed starting from Voltage Regulator Module (VRM). VRM is the component on motherboard to provide a chipset the appropriate supply voltage. It regulates voltage from main power supply (+5V or +12V) and converts it into a much lower voltage required by chipset.

Voltage coming out from the VRM will be the starting point of power integrity path. Supply voltage penetrates into intermediate layer of routing within motherboard through vias before it is delivered into package. A typical PDN supply voltage is routed within the printed circuit board (PCB). Top layer of PCB is usually reserved for signal microstrip traces.

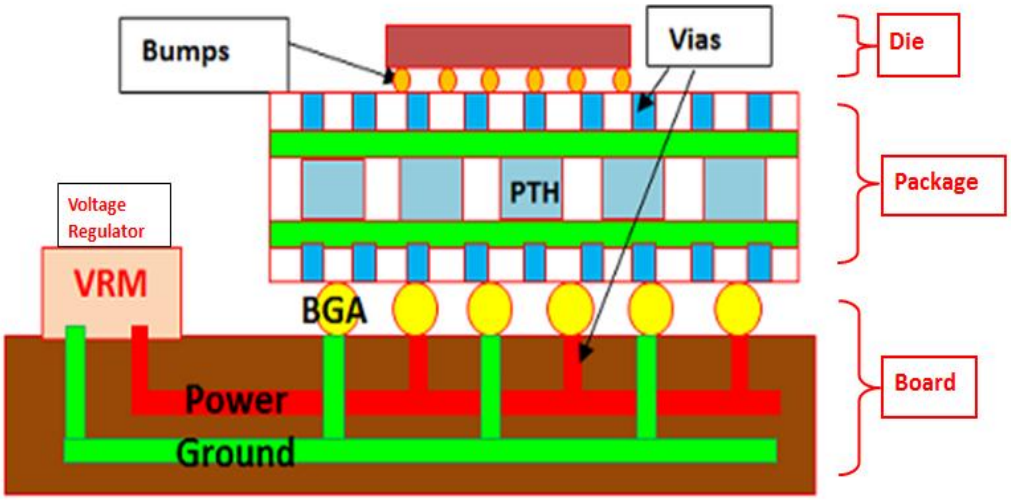

Figure 2.1: Example of PDN model (Mahajan *et al.*, 2004)

From motherboard, supply voltage goes into package through Ball Grid Array (BGA) (Chen *et al.*, 2012). BGA is one of the surface-mount packaging used for integrated circuit such as microprocessors and chipsets. Within package, voltage is routed through multiple high-density vias and Plated Through-Hole (PTH) before it reach top layer of packaging. These vias and PTHs contain high inductance and resistance path, which contribute to supply voltage droop as current flow through.

Finally, supply voltage is delivered into silicon through C4 bump or flip chip (Chen *et al.*, 2012). Flip chip is used for interconnecting semiconductor devices, such as integrated circuit chips to external package with solder bumps. In past analysis, power integrity covered up to C4 bumps without considering on-die interconnects. However, on-die interconnect contributes significant resistance path due to its high density layout. Hence, on-die power grid is taking into consideration in PDN analysis due to its impact in DC voltage drop.

2.2.1(a) Current Flow in PDN

In a PDN, all the voltage routing, vias, BGAs, PTHs contain inductance and resistance. Transistor draws current from supply voltage when there is switching activities happen. Current travels through the PDN impedance path will induce IR drop together with AC voltage fluctuation in supply voltage. Supply voltage drop increases especially when large current is needed by transistor; while voltage regulator cannot supply sufficient amount of current to the circuit.

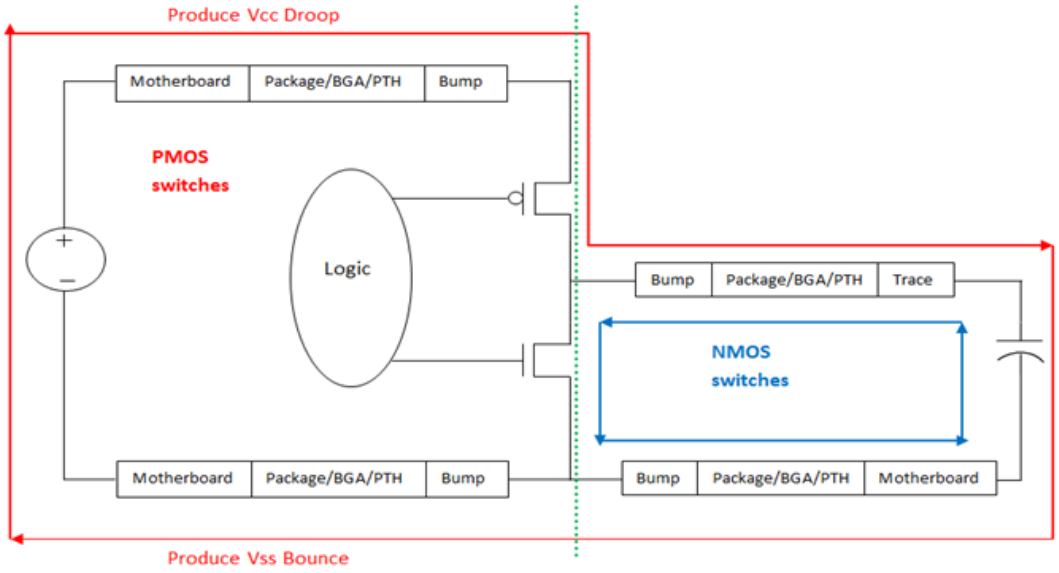

Figure 2.2: Current flow in CMOS transistor (Soman, 2006)

Figure 2.2 shows a typical current loop as transistor switches in a circuit. Model on the left represents the PDN; whereas model on the right illustrates the signal traces. When PMOS is turned on, current flows through red color line which induces supply voltage droop and ground bounce. When NMOS is turned on, current is discharged through the blue color line. Ideally digital circuit as in Figure 2.2 does not induce voltage droop since no current flow through PDN. However, there is still leakage current flow through transistor due to its non-ideality.

2.2.1(b) PDN Lumped Model

Current flow through PDN can be simplified in a lumped model. Voltage routing, BGAs, vias, PTHs are replaced by resistance and inductance in the lumped model as shown in Figure 2.3.

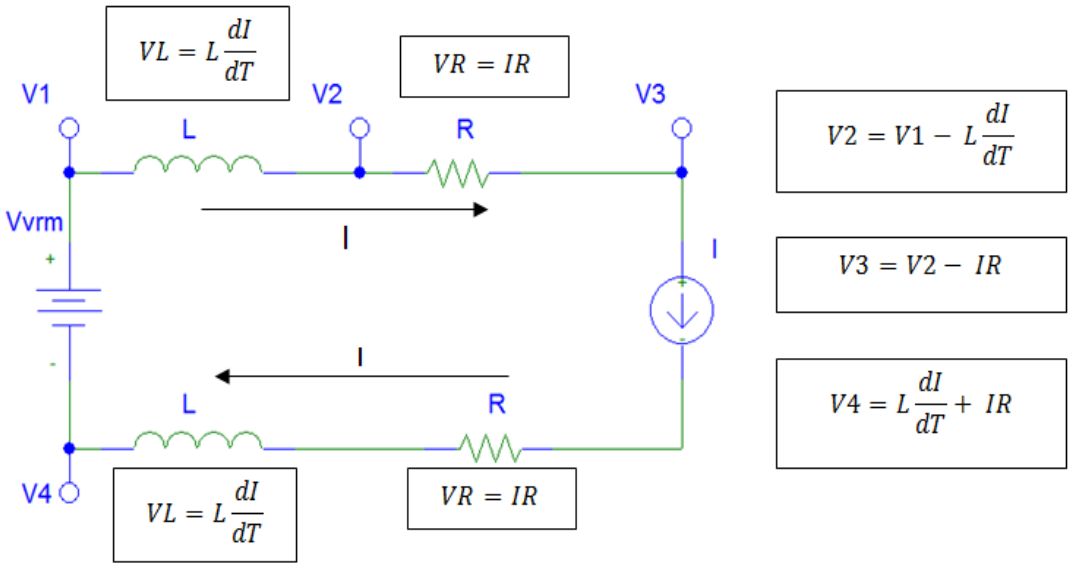

Figure 2.3: Current flow in simplified PDN model

V1 – Input voltage from voltage regulator.

V3 – Output voltage going into transistor.

In ideal case, there is no inductance and resistance exists in path:

$$L = 0, \qquad R = 0, \qquad V3 = V2 = V1 \tag{2.1}$$

In reality, inductance and resistance exist in PDN:

$$V3 = V1 - L\frac{dI}{dT} - IR \tag{2.2}$$

In order to reduce voltage droop in PDN, decoupling capacitor is added to PDN as shown in Figure 2.4. Decoupling capacitor typically comes with Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL). It is resulted from manufacturing which reduces the efficiency of the decoupling capacitor.

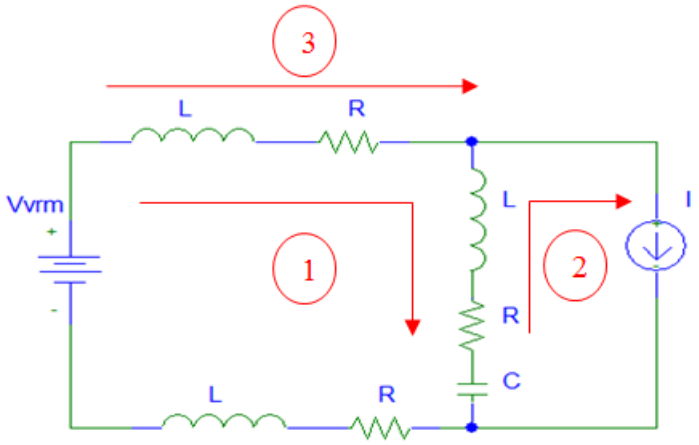

Figure 2.4: Simplified lumped model of PDN with decoupling capacitor

As power supply turned on, decoupling capacitor will be charged up. Capacitor is the first to supply AC current required by transistor as it turns on. It reduces slew rate of current across the PDN. Hence, the capacitor must be placed as near as possible to the load to increase the decoupling efficiency.

The full lumped model of PDN is displayed in Figure 2.5. It is split into 4 regions: voltage regulator, motherboard, package and die (silicon). Each region consists of inductance and resistance in series that contribute to voltage droop. Different decoupling capacitors are connected at these regions. Each capacitor in PDN serves its own function in filtering supply noise from low to high frequency.

The reason of SSN increases with later generation of chipset can be explained from the lumped model. Voltage droop relies mainly on current amplitude,

current slew rate and impedance of PDN. Current amplitude increases together with the number of I/O in integrated circuit, which contributes to both DC and AC voltage droop. Next, current slew rate increases proportionally with higher data rate; results into excessive AC voltage fluctuation. Besides, challenges in reducing PDN inductance and resistance increase after silicon and package size shrink. These factors contribute to the supply noise significantly, causing excessive SSN in supply voltage in typical integrated circuit.

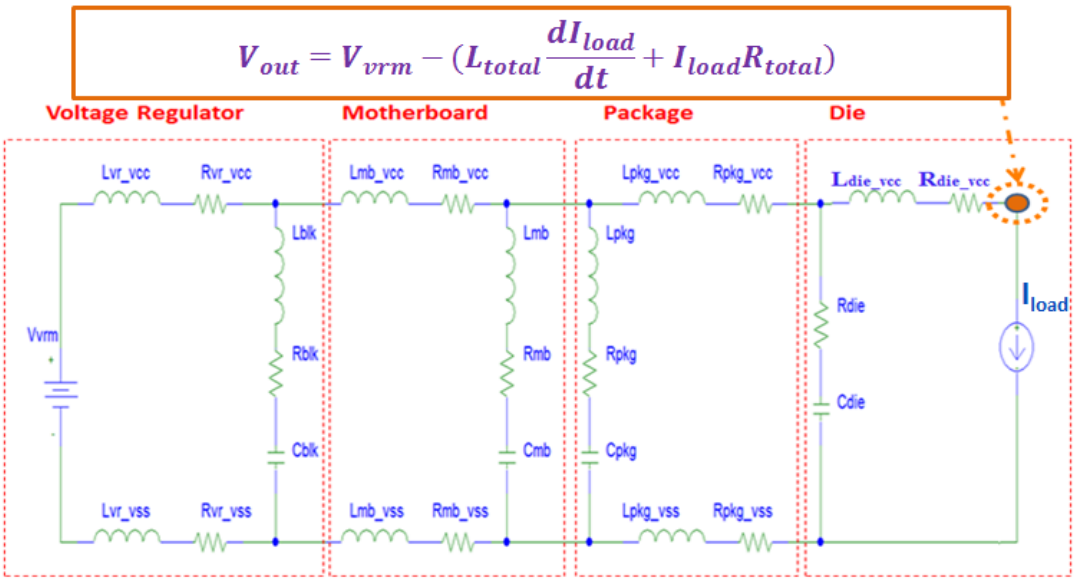

Figure 2.5: PDN full lumped modeling

2.2.2 Impedance Profile

PDN can be analyzed in time domain and frequency domain (Watkins *et al.*, 2012). Simulation in time domain by using transistor circuit model, together with package model extraction has the highest accuracy, but may require a huge computing resource. Hence, estimation of SSN by using frequency domain of impedance is introduced in PDN design (Kim, 2011). It saves the long simulation

time with frequency domain analysis. Effective impedance of PDN can be simulated in frequency domain, containing the PDN resonance peak frequency information. Although it cannot predict the exact amplitude of supply noise as in transient simulation, but it can identify the maximum supply noise frequency by observing through PDN resonance frequency.

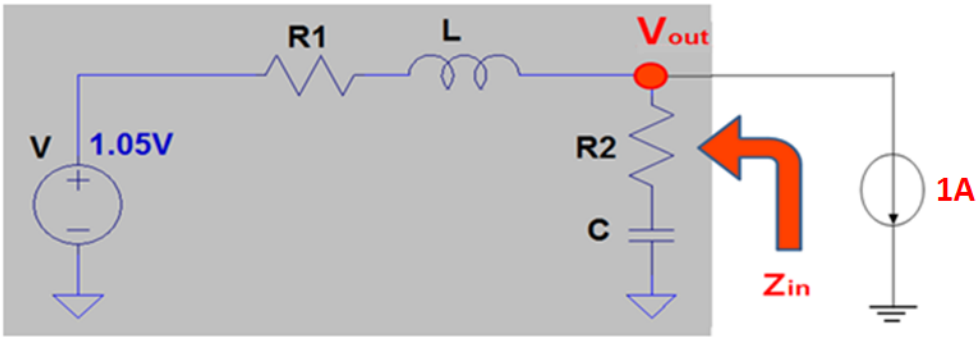

Figure 2.6: Impedance profile connection in frequency domain analysis

Way of obtaining impedance profile of a PDN in frequency domain is shown in Figure 2.6. By replacing the load current with AC current of 1.0 A, impedance of PDN is simulated by probing on V_{out} as illustrated. From the ohm's law equation, $V = ZI$, impedance, Z of PDN is equal to the output voltage, V by setting output current, I to 1.0 A. An example of impedance profile is shown in Figure 2.7.

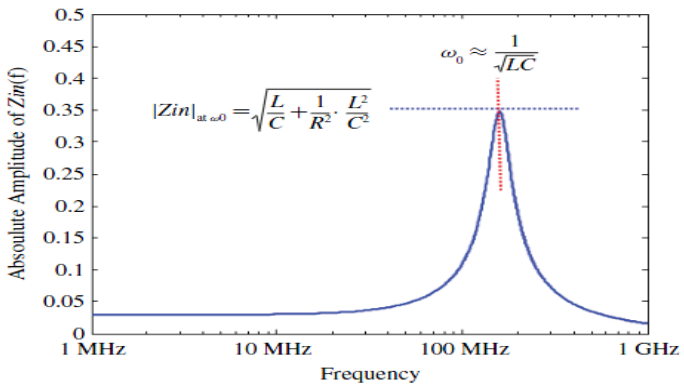

Figure 2.7: Example of PDN impedance in frequency domain (Kim, 2011)

2.2.2(a) Target Impedance

From the impedance profile in frequency domain, PDN can be designed to meet the voltage droop across whole frequency range. Once the target voltage droop is known, PDN design target impedance can be obtained by using maximum current drawn by the integrated circuit. The AC noise, V_{ACN} is a function of PDN impedance PDN and current, I_{CC} flowing through (Soman, 2006).

$$V_{ACN}(f) = I_{cc}(f) * Z(f) \tag{2.3}$$

As long as AC noise target, $V_{ACN}(f)$ and maximum current drawn, $I_{cc}(f)$ are known, PDN can be designed to meet maximum target impedance, $Z(f)$. Target impedance profile is the maximum PDN impedance to meet at every frequency. With such approach, worst case voltage droop can be controlled within the design specification throughout every frequency.

2.2.3 Supply Noise

It is very pessimistic to use the method in frequency domain to meet target impedance at the whole frequency range (Soman, 2006). It may lead to design bottleneck or overdesign in PDN to fulfill the design requirement. Other than analyzing the PDN in frequency domain, methodology used in current chipset PDN design is time domain simulation. Ideally, supply noise is simulated by connecting PDN together with integrated circuit. It has the highest accuracy in getting supply noise by using transistor circuit; with compensation of long simulation time. An alternative way of simulating supply noise is by using current profile generated from integrated circuit to represent to the I/O activities.

2.2.3(a) Current Profile

Current profile is used to replace complicated transistor model circuit in SPICE simulation. Worst case current profile is generated from simulation by setting the temperature and process corner to produce highest current slew rate. High slew rate current profile usually includes the highest frequency data transition pattern. Supply noise simulated by worse case current profile in time domain is then used as supply noise design target (Tan, 2009). This current profile is placed right after the PDN in simulation to obtain supply voltage in time domain.

Current profile can be generated separately from different buffer to be connected in distributed model; or integrated all current profile together in a single lumped model. Separated current profile is preferred for better accuracy and flexibility in PDN analysis. On-die power grid is needed to distinguish current profile's connection from each buffer. The way of obtaining current profile by simulation is demonstrated as example in Figure 2.8.

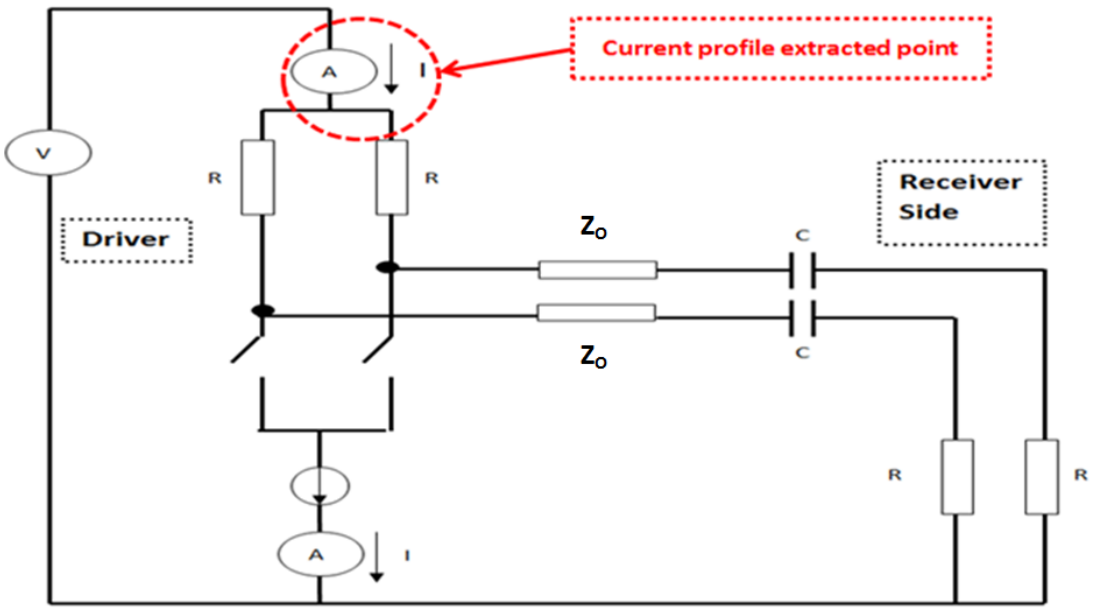

Figure 2.8: Current profile probing point in typical differential I/O (Soman, 2006)

2.2.4 Simultaneous Switching Noise

As discussed in Section 2.2.1(b), supply voltage droop is a function of current, resistance, inductance, and slew rate of current (Smith, 1999). When there is only one lane of I/O active as shown in Figure 2.9, the current drawn is insignificant and the resulted supply noise can be controlled easily. However, current amplitude increases when there are multiple I/O switching events happen at the same time (refer to Figure 2.10). The slew rate of current is amplified especially if these I/O operate in phase with each other as displayed in Figure 2.11. The current of these I/O overlap and result into excessive voltage droop in PDN (refer to Figure 2.12). This phenomenon is interpreted as SSN.

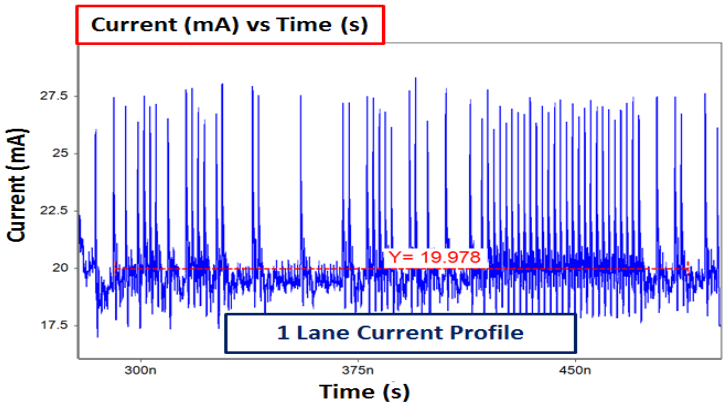

Figure 2.9: Example – One I/O switching (current profile)

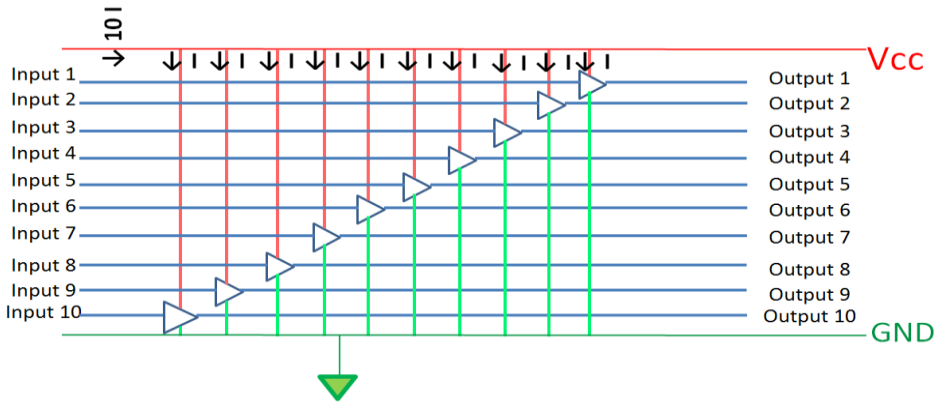

Figure 2.10: Example of 10 buffers simultaneous switching

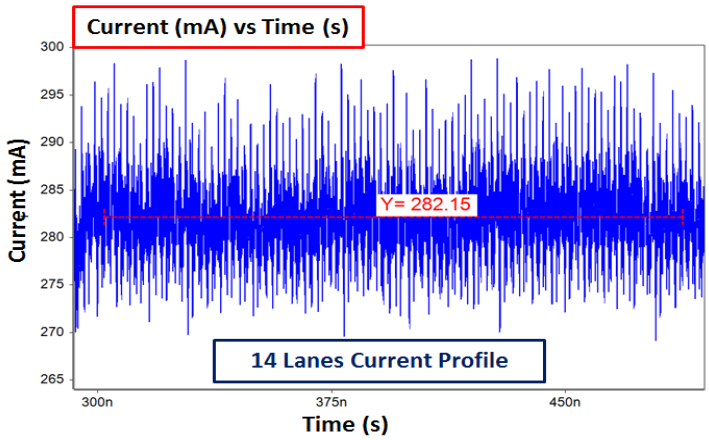

Figure 2.11: Example – 14 I/O switching (current profile)

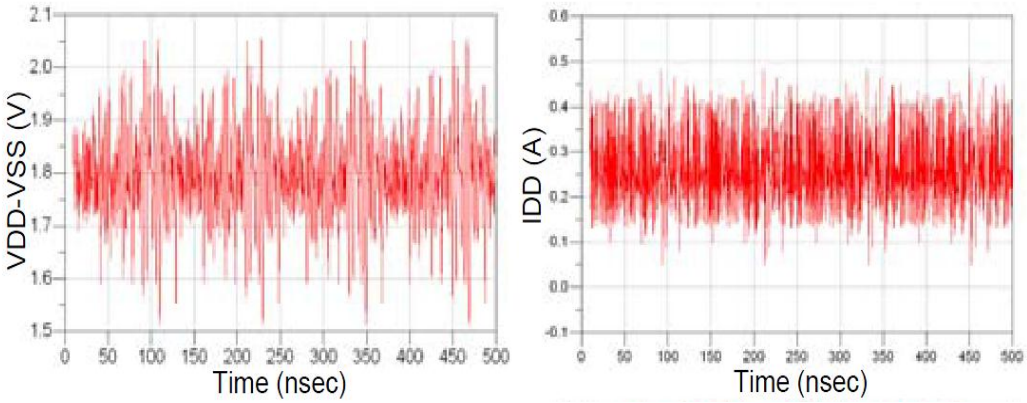

Figure 2.12: Supply noise and current profile due to simultaneous switching (Oikawa *et al.*, 2010)

Signal degradation happens when SSN exists in supply rail, in which reduces the timing margin and voltage margin of signal. The impact of SSN to signal is further emphasized when signal channel model is included in the simulation (Oikawa *et al.*, 2010). The continuously increase in data rates lead to higher SSN and further degrades the signal performance. Impact of higher data rate to supply noise and signal performance can be observed in the previous research by using graphic memory systems (Kim *et al.*, 2007), as shown in Figure 2.14.

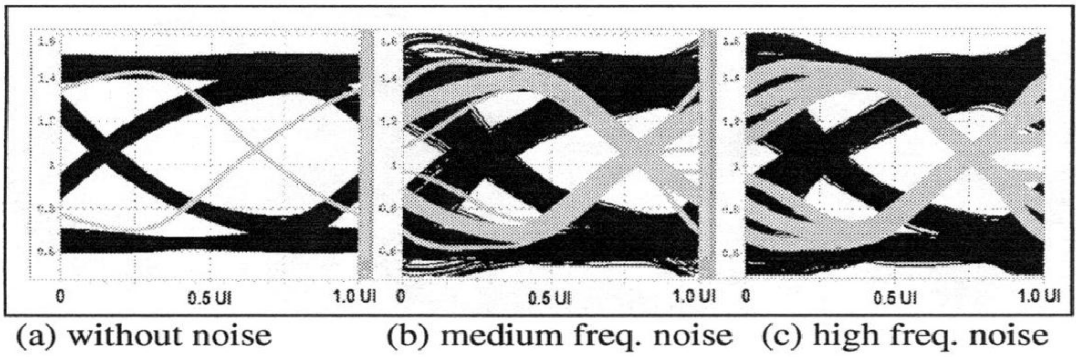

Figure 2.13: Eye diagram resulted by different frequency of SSN (Kim *et al.*, 2007)

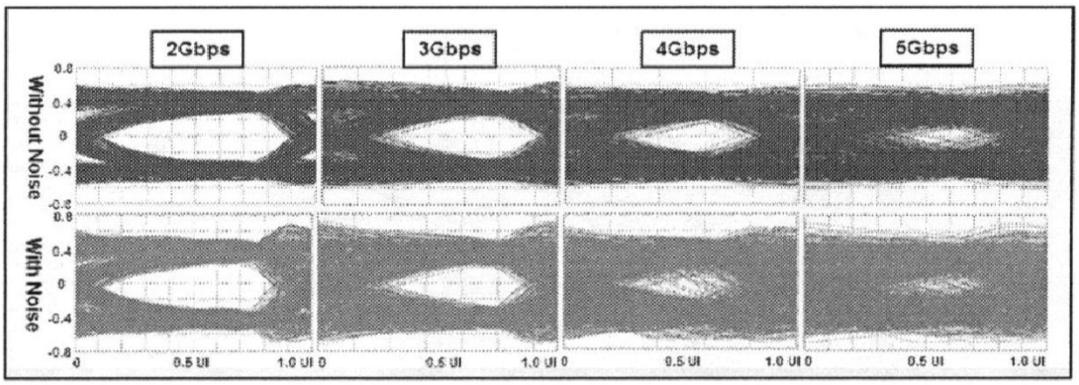

Figure 2.14: SSN impact to eye diagram at different data rate (Kim *et al.*, 2007)

2.2.5 Power Integrity Improvement Methods

Power integrity is affected by both current and impedance of PDN. Throughout generation, engineering efforts are focusing in optimizing PDN either in packaging or board routing. The main objective of PDN design is trying to control the impedance as low as possible and keep the voltage droop to minimum level. Furthermore, a better power integrity model is always desired to improve the accuracy and efficiency in simulation (Kulali *et al.*, 2007; Yang *et al.*, 2010). This section will introduce the example of efforts done to improve the PDN design.

2.2.5(a) Decoupling Capacitor

Decoupling capacitor is introduced in PDN to decouple one part of an electrical circuit from another. A switching event in one sub circuit may cause fluctuation in the power supply. In order to prevent other sub circuit to be affected by the noise, a decoupling capacitor is used. Noise induced by other circuit elements is shunted through the capacitor, reducing the effect of the noise on the other part of circuit (Thierauf, 2004).

Besides, capacitor also works as the circuit's local charge storage. It doesn't act as DC current supplier to circuit. It is charged up as soon as the power supply is turned on without serving other purpose. When a load is applied to a voltage source, certain amount of current is drawn. Voltage regulator has to supply this amount of current drawn with smallest change in supply voltage. However, voltage regulator can only supply low frequency current to keep the output voltage constant. The instantaneous current change as circuit start up in turn affects the transient voltage levels due to inductance in typical PDN. In this case, capacitor behaves as an instantaneous current supplier to the load. It effectively maintains stability of the power supply voltage.

The example of decoupling capacitors used in typical PDN in chipset is shown as below:

Voltage regulator – Bulk Capacitor

Motherboard – Edge Capacitor (EC), Back Side Capacitor (BSC)

Package – Die Side Capacitor (DSC), Land Side Capacitor (LSC)

Silicon / Die – Device Capacitor (Cdie), Mim Capacitor

Each type of capacitor serves its own purpose in controlling supply noise in PDN. Bulk capacitor is the nearest capacitor to voltage regulator. It can store large amount of charge and respond to lowest frequency of transient current change in circuit. The next capacitor is Edge Capacitor (EC) or Back-side Capacitor (BSC). These on-board capacitors normally placed as near as possible to package and responded to low and middle frequency of current change. On-package capacitors come after on-board capacitors. The example of on-package capacitors are Die-side Capacitor (DSC) or Land-side Capacitor (LSC). These capacitors are again mounted as near as possible to die for better efficiency. They are supplying charge to middle and high frequency of current drawn. The last decoupling capacitors are On-die Capacitors (Cdie), such as device capacitor and mim capacitor. These capacitors are the nearest to the transistor circuit and have the highest efficiency; playing a role in supplying highest frequency transient current change. The only limitation of these capacitors is their values are usually much smaller as compared with other capacitors. In addition, area constraint in silicon is limiting Cdie value to be increased further. Figure 2.15 shows some example capacitors used in PDN.

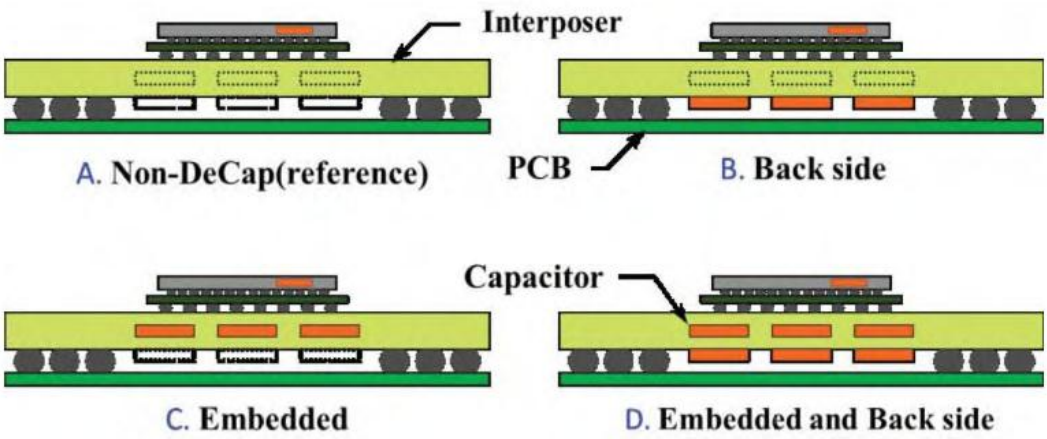

Figure 2.15: Example – Different decoupling capacitor placement (Nabeshima *et al.*, 2011)

Other than that, capacitor works as counter resonance to inductance in typical impedance profile plot of PDN as illustrated in Figure 2.16. Inductance results to high impedance in PDN especially when frequency goes up to MHz or GHz regions. High frequency impedance is suppressed by adding decoupling capacitor in PDN, by leaving only smaller resonance peak at middle frequency. The examples of power supply noise with and without decoupling capacitor are shown in Figure 2.17 and Figure 2.18.

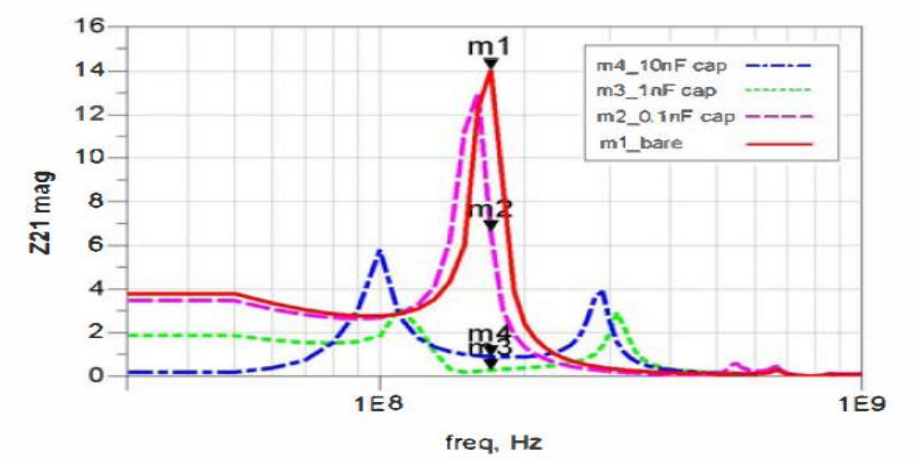

Figure 2.16: Impedance profile by different decoupling capacitors (Lin *et al.*, 2012)

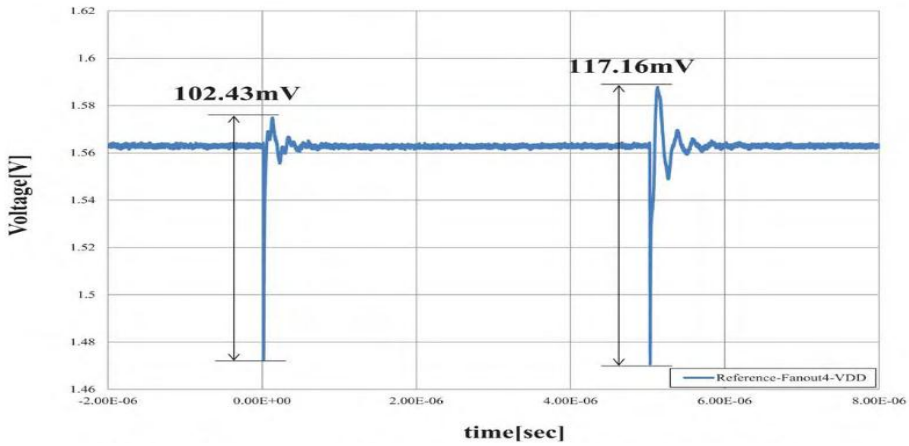

Figure 2.17: Power supply noise without on-die capacitor (Nabeshima *et al.*, 2011)

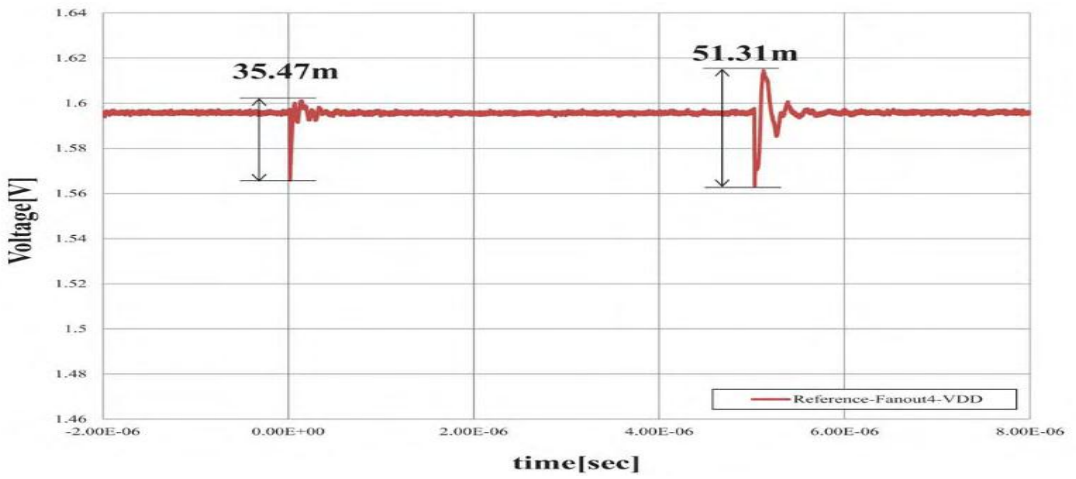

Figure 2.18: Power supply noise with on-die capacitor (Nabeshima *et al.*, 2011)

2.2.5(b) Layout Design

On top of decoupling capacitor, PDN layout is one of the keys parameter to be improved. Better package design reduces the effective inductance and resistance of PDN. Larger power plane in PDN is preferable in typical design. Ground plane is placed as close as possible to supply voltage to reduce the return path current loop. Reasonable number of vias and pins are placed to decrease the PDN resistance.

Besides, newer methodology in packaging is introduced as effort in optimizing PDN design. For example, silicon through-via (STV) (refer to Figure 2.19) is recommended in past research to decrease inductive impedance of PDN and suppressing SSN in 3-D stacked chip package. Significant reduction of inductive PDN impedance can be achieved by replacing the conventional bonding wires in multiple-stacked chip package by STV connections as shown in Figure 2.20. With such design methodology, high frequency SSN is reduced by 80% in the STV interconnects (Ryu *et al.*, 2007).