DEVELOPMENT AND IMPLEMENTATION OF A NEW TECHNIQUE FOR BERT (BIT ERROR RATE TESTER) USING SDR PLATFORM

BY

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DEDICATION

بِسْمِ اللَّهِ الرَّحْمَٰنِ الرَّحِيمِ

...قَالَ رَبِّ أَوْزِعْنِي أَنْ أَشْكُرَ نِعْمَتَكَ الَّتِي أَنْعَمْتَ عَلَيَّ وَعَلَىٰ وَالِدَيَّ وَأَنْ

أَعْمَلَ صَالِحًا تَرْضَاهُ وَأَصْلِحْ لِي فِي ذُرِّيَّتِي إِنِّي تُبْتُ إِلَيْكَ وَإِنِّي مِنَ الْمُسْلِمِينَ

سورة الأحقاف﴿١٥﴾

Praise be to Allah, the most gracious and most merciful. Without his blessing and guidance, my accomplishments would never have been possible

MY supervisorAssoc. Prof.Dr.Widad Ismail

My beloved late parents for making out of me the person who can present such a work...for doing all this with pleasure.

My dearest sisters and brothers give me all their supports

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"All praises and thanks to ALLAH"

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LIST OF ABBREVIATIONS

1G	First Generation
2G	Second-Generation
2.5G	Two and Half Generation
3G	Third Generation
4G	Fourth- Generation
ACI	Adjacent Channel interference
ACLR	Adjacent Channel Leakage Ratio
ADC	Analogy digital converter
AM	Amplitude Modulation
ANC	Active Noise Control
ASK	Amplitude Shift Keying
ASICs	Application Specific Integrated Circuits
AGC	Automatic Gain ControL
AWGN	Additive White Gaussian Noise
BER	Bit error rate
BERT	Bit Error Rate Tester
BPSK	Phase Shift Keying
BTS	Based Transceiver Station
CCStudio	Code Composer Studio
CDMA	Code Division Multiple Access
CLT	Central Limit Theorem
CPE	Customer-Premises Equipme
CPH	A control processor host
CPLD	Complex Programmable Logic Device

CPU	Central Processing Unit
CSMA-CA	Carrier Sense Multiple Access With Collision Detection
CVSD	Continuously Variable Slope Delta Modulation
DB	Digital Board
DCS	Digital Cellular System
DECT	Digital Enhanced Cordless Telecommunication
DAC	Digital-to-Analogue Converters
DP	Development Platform
DRP	Digital Receiver Processor
DSPs	Digital Signal Processors
DSL	Digital Subscriber Lines
DSSS	Direct – Sequence Spread spectrum
DVB	Digital Video Broadcasting
DUT	Design under Test
EHF	Extremely High Frequency
EIRP	Effective Isotropic Radiated Power
ELF	Extremely Low Frequency
EMI	Electromagnetic Interference
EMIF	External Memory Interface
ENR	Excess Noise Ratio
EVM	Error Vector Magnitude
FDL	Fiber Delay Line
FDATool	Filter Design Analysis Tool
FETs	Field-Effect Transistor

FHSS	Frequency-HoppingSpread *S*pectrum
FIFO	First-In- First-Out
FIR	Finite Impulse Response
FM	Frequency Modulation
FSK	Frequency Shift Keying
FPGAs	Field Programmable Gate Arrays
GPPs	General-Purpose Processors
GSM	Group Special Mobile
GPON	Gigabit-Capable Passive Optical Network
GMSK	Gaussian Minimum Shift Keying
HR	Hardware radio
HDL	Hardware Description Language
HIL	Hardware-in-the-loop co-simulation
HF	High Frequency
HW/SW	Hardware/Software
IC	Integrated Circuits
IEEE	Institute of Electrical and Electronics Engineers
ISR	Ideal software radio
IF	Intermediate Frequency
IIR Filters	Infinite Impulse Response Filters
I/O	Input/output
IQ	In-phase and Quadrature
IMT-2000	International Mobile Telecommunications 2000
IP	Internet Protocol
ISE	Integrated Software Environment

IS-95	Interim Standard 95
ISM	Industrial, Scientific, & Medical Radio Frequency Band
ITU	International Telecommunication Union
JTRS	Joint Test Action Group
KUAR	Kansas University Agile Radio
LA	Link Adaptation
LF	Low Frequency
LPF	low-Pass Filter
MAC	Medium Access Control
MADs	Number of Multiples and Adds
MAI	Multiple Access Interference
MARS	Maynooth Adaptable Radio System
MBDK	Model-Based Design Kit
MC	Modulation Classification
MDS	Minimum Detectable Signal
MDA	Model Driven Architecture
MF	Medium Frequency
MGT	Multi-Gigabit Transceiver
MILCOM	Military Communications
MI	Modulation Index
ML	Maximal Length
MODEM	Modulation – Demodulation
MSK	Minimum Shift Keying
NICT	Institute of Information and Communications Technology
NP	Network Processors

OFDM	Orthogonal Frequency Division Multiplexing
OOK	On-Off Keying
OPB	On-Chip Peripheral Bus
QPSK	Quadrate Phase Shift Keying
π/4 QPSK	π/4 Differential Quadrate Phase Keying
OMG	Object Management Group
OSI	Open Systems Interconnection model
QAM	Quadrature Amplitude Modulation
QoS	Quality of Service
PCS	Personal Communication Services
PDC	Personal Digital Cellular
PHY	Physical layer
PLL	Phase Locked Loop
PM	Phase modulation
PN	Pseudo-Random Noise
PRBS	Pseudo-Random Bit Sequence
PR	Partial Reconfiguration
RAM	Radar-Absorbing Material
RBP	Reprogrammable Baseband Processor
RF	Radio Frequency
RFPWM	RF Pulse Width Modulator
RISC	Reduced Instruction Set Computer
ROM	Read Only Memory
RTOS	Real-time Operating Systems
SD	Secure Digital

SD	Sphere Decode
SSB	Single Sideband
SDR	Software Defined Radio
SFF	Small Form Factor
SFF SDR	Small Form Factor SDR Evaluation Module/ Development
EVM/DP	Platform
SNR	Signal-to-Noise Ratio
SNR_{req}	SNR required
SHF	Super High Frequency
SLF	Super Low Frequency
SCR	Software controlled radio
SPI	Serial Peripheral Interconnection
SR	Software Radio
TETRA	Terrestrial Trunked Radio
TDMA	Time Division Multiple Access
TRF	Tuned Radio Frequency
UCS	Universal Signal Classifier
UHF	Ultra High Frequency
ULF	Ultra Low Frequency
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
USRP	Universal Software Radio Peripheral
VHF	Very High Frequency
VLF	Very Low Frequency
VLIW	Very Long Instruction Word

VOAs	Variable Optical Attenuators
VCO	Voltage Controlled Oscillator
VPBE	Video Processing Back-End
VPFE	Video Processing Front-End
VPSS	Video Processing Subsystem Protocol
v4	Xilinx virtex 4
v5	Xilinx virtex 5
VSB	Vestigial sideband modulation
WARP	Wireless Open-Access Research Platform
WCS	Wireless Communications Systems
WCDMA	Wideband Code Division Multiple Access
W-LAN	Wireless Local Area Network
W-PAN	Wireless Personal Area Network
XST	Xilinx Synthesis Technology

LIST OF SYMBOLS

E_b	Bit Energy
N_o	Noise Power
Pe	Error Probability
P_R	Received Power
P_T	Transmitter Power
P_R	Received Power
R	Data Rate
-	No value

PEMBANGUNAN DAN IMPLEMENTASI SATU TEKNIK BARU UNTUK BERT (BIT ERROR RATE TESTER) MENGGUNAKAN SDR PLATFORM

ABSTRAK

Pendekatan rekabentuk sepunya (perkakasan / perisian) menjadi pilihan berprospek kerana menawarkan kemampuan masa nyata sambil memberikan penyelesaian fleksibel yang merangkumi peningkatan sistem yang kompleks dan masa-untuk-pasaran. Rekabentuk Hybrid GPP / DSP / FPGA adalah penyelesaian yang layak untuk teknologi perisian radio ditakrifkan. Tesis ini menunjukkan rekabentuk yang praktikal dan prosedur pelaksanaan untuk membina model yang bermanfaat, cekap dan fleksibel dari kesalahan bit error rate tester (BERT) pada lapisan fizikal untuk UHF-band dari penghantar/penerima digital dengan menggunakan arkitektur baru di Radio Multi-Core Software-Defined platform. Sebuah BERT untuk penerima digital adalah melibatkan pemodelan saluran pemancar dan bising serta penerima itu sendiri. Secara tradisional BER dinilai menggunakan simulasi, yang sangat memakan masa dan tidak diautomasi dalam masa nyata. Untuk mengatasi masalah ini, tesis ini menyajikan skim untuk ujian BER dalam menggunakan SFFSDR dengan beberapa perintah nilai pemecutan besarnya dibandingkan. Penyelidikan ini menyajikan pembangunan penghantar/penerima digital yang dicadangkan pada platform SFFSDR dalam tiga langkah. Langkah pertama ialah tahap simulasi yang menggunakan Xilinx System Generator blok dan blok Lyrtech. Langkah kedua melibatkan rekabentuk Simulasi Co Hardware-(HIL) pelaksanaan pada perkakasan alat pemodelan FPGA. Langkah Ketiga menggambarkan rekabentuk berdasarkan Real Time DSP / FPGA perkakasan. Implementasi yang dicadangkan mempunyai penjana nombor rawak sebagai sumber

data. Data ini dimodulasi dan ditukar ke atas sebelum disuapkan ke modul RF SDR SFF. Isyarat yang diterima daripada RF yang kemudian ditukar ke bawah dan didemodulasi dan disuapkan ke komparator yang menghitung jumlah kesalahan dengan membandingkannya dengan bit dihantar. Dua skim modulasi koheren digunakan (iaitu FSK dan BPSK) untuk pelaksanaan ini secara nyata. Mha disaranka agar prototaip perkakasan hibrid termasuk kedua-dua blok DSP dan FPGA secra bersama adalah platform perkakasan yang ideal untuk melaksanakan sistem. Pendekatan yang dicadangkan BERT meminimumkan keperluan perkakasan ”custom" dan sistem ujian dengan mengintegrasikan fungsi jalur asas pada FPGA menggunakan SFFSDR. FPGA memberikan gabungan berprestasi modul pemprosesan isyarat dan berprestasi logik tinggi berkonfigurasi besar yang menghasilkan satu platform sesuai fabrik untuk prototaip sistem komunikasi. BER pendekatan dalam masa nyata telah diuji untuk berkesan pada digital BPSK dan FSK yang diperolehi berada dalam urutan 10^{-3} pada SNR 15 dB dan 17dB bagi setiap satu.

DEVELOPMENT AND IMPLEMENTATION OF A NEW TECHNIQUE FOR BERT (BIT ERROR RATE TESTER) USING SDR PLATFORM

ABSTRACT

Hardware/Software (HW/SW) co-design approaches become prospective choice due to its real time operation since these solutions are so flexible that cover extensive complicated systems and reduce time from design to market. Hybrid digital signal processors (DSPs), field programmable gate arrays (FPGAs) and general-purpose processors (GPPs) designs are viable solution for software defined radio (SDR) technology. This thesis demonstrates a practical design and implementation procedure for building a useful, efficient and flexible model of a bit error rate tester (BERT) on physical layer for UHF-band of the digital transceivers by using new architecture in Multi-Core Software-Defined Radio Platform. A BERT for a digital receiver involves modelling a transmitter and noisy channel, as well as the receiver itself. Typically, BER is calculated using simulations, which are very time-consuming and not automated in real time. In order to solve this problem, this thesis presents a scheme for BER testing using small form factor (SFF) SDR .This research presents the development of the proposed digital transceiver on the SFFSDR platform in three steps. The first step is the simulation level, which uses the Xilinx System Generator block and Lyrtech block. The second step involves the design of the Hardware-in-the-loop (HIL) Co-simulation and the implementation on FPGA hardware-modeling tool. The third step describes the design based on Real Time DSP/ FPGA hardware. The proposed implementation has a random number generator as data source. This data is modulated and up-converted before it is fed to the RF module of the SFFSDR .The received signal from the RF is later down-converted and demodulated and fed to the comparator which calculates the number

of errors by comparing it with the transmitted bits. Two types modulation (i.e. FSK and BPSK) are used to test proposed for real implementation. It is suggested that a hybrid hardware prototype including including both the DSP blocks, and FPGA together as an ideal hardware platform for implementing the system. The proposed BERT approach minimizes the need for custom hardware and test systems by integrating the baseband functionalities on FPGAs using SFFSDR. FPGAs provide a mix of high-performance dedicated signal processing modules and a large reconfigurable logic fabric, which makes them suitable platform for prototyping communication systems. The developed BERT is tested successfully for BPK and FSK digital transceivers with BER obtained to be in the order of 10^{-3} at SNR of 15dB and 17dB respectively.

CHAPTER 1

INTRODUCTION

1.1 General View and Motivation

The emergence of wireless communications is developing at an alarming pace and this has brought about the practice of new standards and protocols in the field of communications. Rapid implementation of the wireline-based Internet has led to the demand for wireless Internet connectivity but with added capabilities, such as integrated services that offer seamless global coverage and user-controlled quality of service (QoS). The challenge in inventing advance wireless Internet connectivity is assembled by the desire for future-proof radios, which keep radio hardware and software from becoming obsolete as new standards, techniques, and technology become addressable (Reed, 2002; Srikanteswara *et al*., 2000; Tuttlebee, 2004). Thus, this motivated the concept of a software-defined radio (SDR). This means that the digital-to-analogue and analogue-to-digital conversions perform as close as possible to the radio frequency. By implementing modulation, demodulation, channel coding and other required processing tasks in the software, the aim of extending the digital domain is achieved (Bonnet *et al.*, 2000; Jian *et al.*, 2000). Therefore, users, service providers and manufacturers become more independent of the realisation of one specific data transmission standard, since by downloading appropriate software code, a different functionality can be adopted by the communications system. Re-using the same software and reconfigurable hardware to handle different processing algorithms would enable an efficient, flexible alternative to current prototyping and implementation methods(Gonzalez *et al.*, 2009; Weiss *et al*., 2003).

As hybrid solutions verify a radio's potential and implementation, they are essential mechanisms for the operation and design of software radios. Since radio operations use programmable designs running on digital hardware, there is flexibility in implementing different wireless standards and waveforms. Hybrid solutions are available in various forms on single-chip custom integrated circuits (ICs), of which the most commonly used for software radio are digital signal processors (DSPs), field programmable gate arrays (FPGAs), general-purpose processors (GPPs), and application specific integrated circuits (ASICs). Hybrid GPP/DSP/FPGA architecture is a viable solution for the software- defined radio technology (Blume, Hubert, Feldkamper *et al.,* 2009).

Figure 1.1 shows the available digital signal processing devices (Safadi & Ndzi, 2006). Analysing the trade-offs among these options and determining the best digital hardware solution for a software radio system is a complex and challenging task for system designers. Some of the main factors in design composition of digital hardware of software radio are computational power, computational density, hardware flexibility, application flexibility, power consumption, reconfiguration time and the total cost involved, each of which providing varying levels of re-programmability and performance (Reed, 2002; Zhang ,2008) . Even though DSPs are less flexible they are often used to provide more deterministic implementation when compared to languages such as C/C++. FPGAs also offer better performance but require specialised programming tools and knowledge, which reduces their flexibility. Despite the ASIC offering the most optimised and efficient digital hardware implementation, their design is in fixed silicon with little or no flexibility(Farrell , 2009; Hee Kong *et al.*, 2006; Thabet *et al.*, 2009).

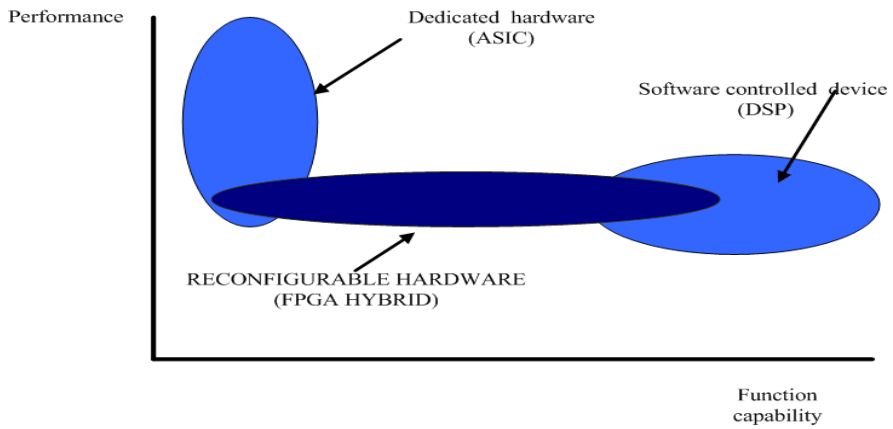

Figure 1.1: The Available Digital Signal Processing Devices(Safadi & Ndzi, 2006)

With the recent advent of software-defined radio (Mitola , 1995), wireless communication systems have become applicable solutions to a wider range of challenging applications. However,the different computational complexities of wireless communication standards requirements are as shown in Table 1.1(Boccuzzi, 2008; Crockett, 1998).

Table 1.1:Signal Processing Complexity(Boccuzzi, 2008; Crockett, 1998).

Wireless standard	**Approximate computational complexity (MIPS)**
802.11 a&b	9000
WCDMA	9000
IS-95	500
GPRS	300
GroupeSpeciale Mobile (GSM)	100

The feasibility of the SDR based implementation BERT (bit error rate tester) of the wireless digital modem on Multi-Core Software-Defined Radio Platform is studied in this thesis. In fact, this platform, called small form factor (SFF) SDR development platform, was a joint development between Texas Instruments

(TI), Xilinx and Lyrtech as well as a host of leading software tool vendors. Bit error rate (BER) and noise figure will be the main parameters used in measuring the noise. BER characteristic is one of the basic measures of the performance of any digital communication system. BER is the fundamental measurement used when testing receiver performance parameters such as sensitivity and selectivity(Ismail, 2003). It is the percentage of erroneous bits received compared to the total number of bits received during an observation period. As the Signal/Noise ratio decreases gradually, for example, the BER increases suddenly near the noise level where l's and 0's become confused. BER shows whether the system is dead or alive. Traditionally, BER is evaluated using code simulations, which are very time-consuming. To overtake these problems, this thesis presents a scheme for BER testing BPSK & FSK digital transceivers in FPGAs based on SFF SDR. BPSK is chosen for SFFSDR prototype because of its ability to tolerate low SNR values, as well as its simplicity, which is reflected in its low cost implementation. In this research, FSK is used in the implementation of wireless transceiver. FSK can be found in many low-cost, such as cordless phones, wireless audio speaker systems and RF consumer telemetry systems.

1.2 Tools System Requirement

During the work of this thesis, hardware and software requirement have been used to complete the tasks of building a BER tester of wireless modem-based SFFSDR. Following is a description of the SDR hardware and programs used and a description of their purpose.

1.2.1 SDR Hardware

The SDR hardware uses the SFF SDR DP manufactured by the Canadian-based company Lyrtech as shown in Figure 1.2 (Lyrtech, 2009). The platform is a development platform for radio applications and not used in production. It is a stand-alone device and consists of three major modules, each controllable by software instructions. This platform is designed as low-cost, off-the-shelf, integrated hardware and software development solutions, and packs some of the latest DSP (DM6446) and FPGA (virtex_4SX35) technology. It has various interfaces on the board, such as RS-232 serial port, 10/100 Mbps Ethernet port, universal serial bus (USB) port, and secure digital (SD) memory card slot. Unfortunately, until today the USB port and the SD memory card slot are not supported (Details of this hardware is in Chapter 3).

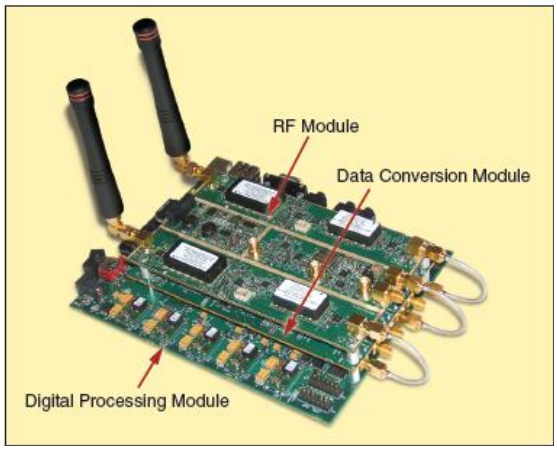

Figure 1.2: The Small Form Factor SDR Development Platform is modular in design (Lyrtech, 2009)

1.2.2 SDR Software

This Platform supports Lyrtech Advanced Development Platform Software, which requires MATLAB, Xilinx System Generator and Xilinx ISE. (Details of this software are in Chapter 3).

1.3 Problem Statement

One important measure of system reliability is the BER of a coding scheme for communication in the presence of noise. A BER tester for a digital receiver involves modelling a transmitter and noisy channel, as well as the receiver itself. As modern systems often require extremely reliable communication (e.g. error probability, P_e on the order of 10^{-10}), this means that a tester must process billions of symbols (or more) over a wide range of signal-to-noise ratios (SNR). Using traditional HDL and software simulations often requires days or weeks to obtain a BER curve (bit error rate as a function of SNR) for a single set of parameters for a decoder (e.g. code rate and trace back length). Simulations are generally not suitable for the evaluation of communication systems with a low BER. Therefore in order to overcome these problems, this research demonstrates how such tools can be used to build a bit error rate tester (BERT) hardware accelerators in FPGA linked to Simulink using System Generator, and also how HIL co-simulation and Real Time DSP / FPGA hardware of the entire system SFFSDR provide a high speed-up over a pure software simulation. Thus, there is a need for a practical design and implementation procedure for building a useful, efficient and flexible model of BERT on physical layer of the digital transceivers.

1.4 Objectives of Thesis

The aim of this research is to build a useful, efficient and flexible model of BERT that will be implemented in real time. This tester is developed to evaluate the bit error rate of digital baseband modem in wireless communication systems. The process of building is achieved by the rapid prototyping approach-based on SFFSDR platform that combines both hardware and software environments. The key features

of the introduced models are low complexity, low power consumption and efficient data transmission. The objectives of this research are summarised as shown below:

1- To design and develop Frequency Shift Keying(FSK) and Binary Phase Shift Keying (BPSK) based wireless communication transceiver by employing Xilinx System Generator blocks and Lyrtech SFFSDR models.
2- To integrate and implement a new approach of BERT design for the developed BPSK and FSK transceiver on SFFSDR development platform based on the simulation and HIL co-simulation, and Real Time DSP / FPGA hardware approaches.
3- To test and verify the proposed configuration to ascertain the repeatability and reliability of the proposed model and technique.
4- To analyse and compare the performance of propsed model for BER measurement.

1.5 Scope and Limitations

The scope of this present work is focused in designing and implementing BERTs for the digital transceiver on high-level simulation and to develop a prototype system on the SFFSDR board. This required the design and development of simulation program and experimental set up that could verify and validate the success of the proposed model and technique. This model and technique would later be developed and integrated on real time SFFSDR development platform. BERTs areactually used to evaluate the bit error rate of the digital modem in wireless communication systems. The BERTs that were developed are illustrated using simulation, HIL co-simulation and real-time on the SFFSDR development platform.

The BERT based Real Time DSP / FPGA Hardware on the Virtex-4 SX35 FPGA application is carried out and the BER performance results evaluated.

One of the major limitations involving this study is the research development time consumed in the learning of the System Generator blocks, ISE suiteneeded to design a fully functional transceiver. In addition, each algorithm used in the simulation has to be tested independently before being integrated into a communication system. Interconnection of different algorithm blocks must be tested to ensure proper operation with neighbouring blocks. Another limitation is with respect to the FPGA, which can only support the fixed-point operation but not the floating point. Therefore, the conversion from floating point to fixed-point using the fix-point arithmetic has to be carried out. The DSP and FPGA clock frequencies are 594MHz and 125 MHz, respectively. The process of normalizing the speeds is a tedious process and the verification step of the proposed system has to undergo numerous steps before it can be finalized.The bandwidth of the signal had to be limited to 20 MHz (Lyrtech, 2009).

1.6 Research Contribution

This research presents many attractive characteristics and also several contributions to the current state of information knowledge. The general and positive contributions include the following:

This was the first attempt to develop a combination of Simulink and Xilinx ISE based SFFSDR to design BERT system. A new technique for BERT design and FPGA implementation based on Multi-Core Software-Defined Radio platform for different digital transceiver systems were attempted. It showed how the Model-Based Design could be applied in the development of the SFFSDR platform leading to the development of component models of the physical system. It was shown that the use

of DSP blocks could significantly reduce the number of logic elements, which can be used to further expand system functionalities This research demonstrated the practicality of the design flow for Hybrid GPP/DSP/FPGA architecture for software-defined radio technology. Soft-core design was incorporated into the hardware to reduce the logic elements. The proposed implementation of Pseudo-Random Bit Sequence (PRBS) patterns as data source provided a convenient way of testing the high-speed interfaces, and is mainly used for BER. The performance comparisons of different modulation and demodulation techniques in SFFSDR implementation were carried out. For telemetric applications, PSK was considered efficient form of data modulation, providing the lowest probability of error for a given received signal level during the measurement of over one symbol period.

The transmitter and receiver systems design were carried out using three different modes. BPSK and FSK system using Xilinx System Generator Blocks and the Lyrtech SFFSDR models were proposed for system level simulation. HIL co-simulation models for transceiver of the FSK and BPSK system were used to validate certain portions of FPGA algorithms on actual hardware.

The real-time implementation of the transceiver for FSK and BPSK system and the distribution of the SDR modem components between the DSP core and the FPGA were implemented.

1.7 Structure of the Thesis

The outline of this work is shown in Figure 1.3. It is divided in two major parts: theory and implementation. The first few chapters cover the theoretical parts while the later chapters describe the work and the results.

Chapter 1 presents a brief introduction on the role of the reconfigurable solutions for implementing the sophisticated signal processing tasks in the digital communication

systems, with emphasis on the tasks performed by the digital transverse-based SFFSDR. This chapter also presents the objective, contribution of thesis and tools environment requirement.

Chapter 2 introduces the topic by giving a general survey about the related subjects in the design; an overview of SDR concept , followed by DSP and FPGA related topics, BERT and related work.

A more detailed description of the requirements of the proposed communication system design and methodology design is introduced in **Chapter 3.**

Chapter 4 presents the design implementation and results-based simulation level.

Chapter 5 presents the design implementation and results-based HIL co-simulation level.

Chapter 6 presents the design implementation and results-based Real Time DSP / FPGA hardware.

Finally, the conclusions made from this research are presented in **Chapter 7**.

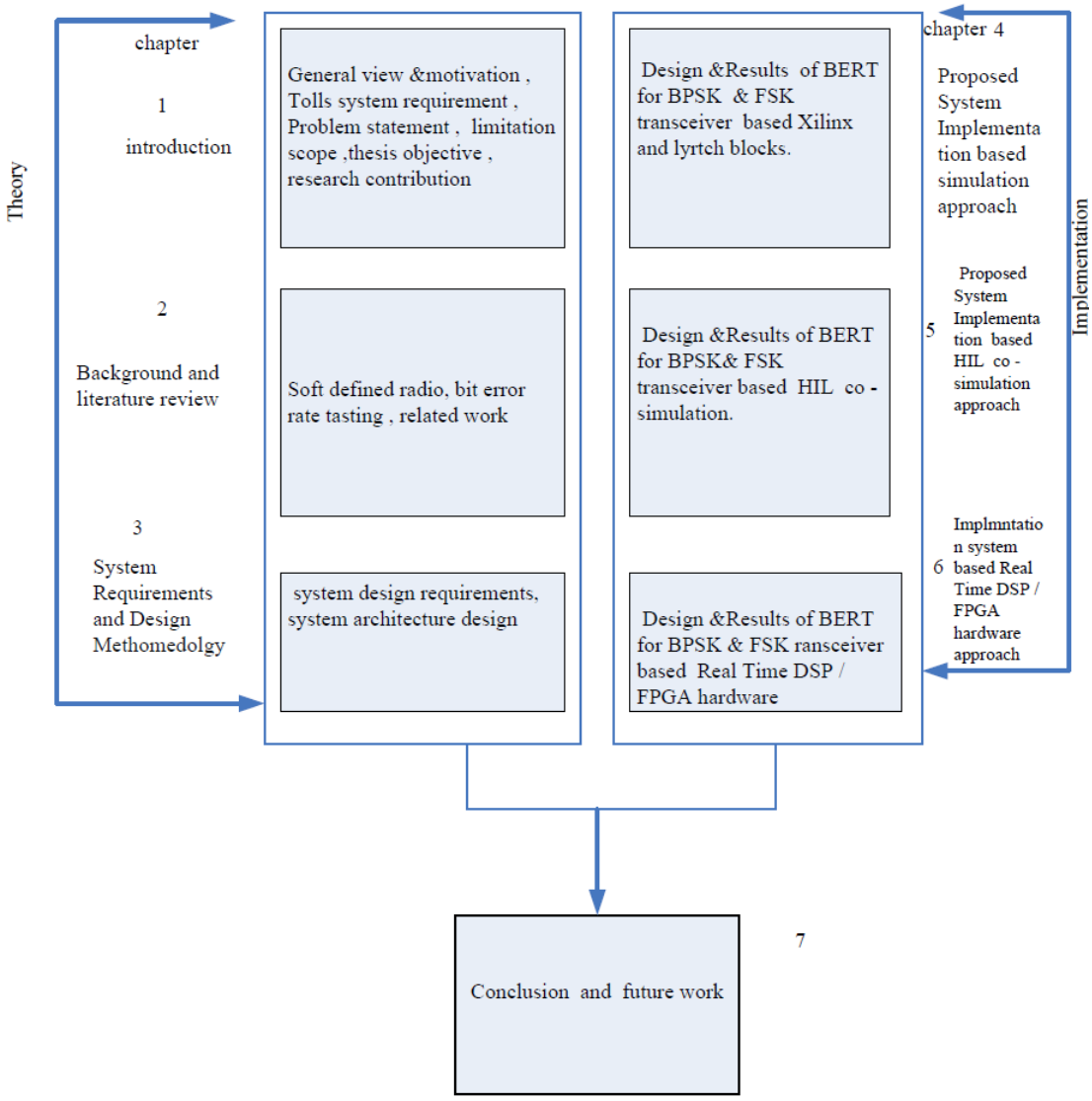

Figure 1.3 : Outline of the thesis

CHAPTER 2

Background and Literature Review

2.1 Introduction

The aim of this chapter is to provide theories, information and previous work about certain topics, which are needed for the design and implementation of this research. The key to understanding these high-level requirements that drive the radio specifications are the various waveforms the radio intends to support. A general description of Next Generation Receiver Architectures (Software-Defined Radio Technology) is introduced. A description of the Embedded Signal Processing, ASIC, DSP, GPP and FPGA is also presented. In addition, BERT theory and its related work to this research are presented.

2.2 Software-Defined Radio Technology

Due to recent increase in demand from wireless communications to IC designers, the trend now is to design extremely flexible receivers that can support multiple standards. The SDR concept has evolved over the past three or four decades, with applicability to various parts of a radio. A software-defined radio is a system, which uses software for modulation and demodulation of communication signals. The goal is to use as little hardware as possible(Schmid, *et.al*. 2006). The SDR Forum has developed a multi-tiered definition of SDR by establishing five tiers encompassing different categories of software radio systems. The five-tier concept is summarised in Table 2.1. Tier 0 represents the 'traditional' radio hardware and forms a baseline reference. The uppermost tier, Tier 4, represents the 'ultimate' vision of SDR. Reality falls somewhere in the middle. For most applications, state-of-the-art

SDR currently aligns with Tier 2 definition. Note that, as mentioned above, it may be argued that virtually all modern wireless communication equipment may be classified as being software-controlled radios (i.e., Tier One) (Alsliety & Aloi, 2007; Chen ,*et al*, 2010).

Table 2.1 : SDR Forum`s tier definitions (SDR)

Tier	Name	Description
0	***Hardware radio (HR)***	Baseline radio with fixed functionality. Implement all the radio functionality in hardware and any changes in functionality require physical intervention to implement. Multiple HRs is required to support several frequencies and protocols.
1	***Software-controlled radio (SCR)***	The radio's signal path is implemented using application-specific hardware, i.e., the signal path is essentially fixed. A software interface may allow certain parameters, e.g., transmit power, frequency, etc., to be changed in software
2	***Software defined radio (SDR)***	Much of the waveform, e.g., frequency, modulation/demodulation, security, etc., is performed in software. Thus, the signal path can, with reason, be reconfigured in software without requiring any hardware modifications. For the foreseeable future, the frequency bands supported may be constrained by the RF front-end.
3	***Ideal software radio (ISR)***	Compared to a 'standard' SDR, an ISR implements much more of the signal path in the digital domain. Ultimately, programmability extends to the entire system with analogue/digital conversion only at the antenna, speaker and microphones.
4	***Ultimate software radio (USR)***	The USR represents the 'blue-sky' vision of SDR. It accepts fully programmable traffic and control information, supports operation over a broad range of frequencies and can switch from one air-interface/application to another in milliseconds

2.2.1 Advantages and Disadvantages of Software-Defined Radios

SDR technology as part of a reconfigurable communication system will affect all parts of the communication network. Table 2.2 outlines the advantages of SDR deployment.

Table 2.2 : Advantages of Software-Defined Radio (Harrington, Hong, & Piazza, 2004)

Interoperability:	Support of multiple standards through multimode and multiband radio capabilities.
Flexibility:	Efficient shift of technology and resources.
Adaptability:	Faster migration towards new standards and technologies through programmability and reconfiguration.
Sustainability:	Increased utilisation through generic hardware platforms.
Reduced Ownership Costs:	Fewer infrastructures, less maintenance and easier deployment.

Although SDRs offer benefits (outlined above), there are disadvantages in the design and implementation of SDRs. These include (Mannan, 2005):

(1) The difficulties of designing softwares for various target systems or standards.

(2) The difficulties of designing air interfaces for digital signals and algorithms of different standards, and

(3) The problems of poor dynamic range in some communication systems design.

2.2.2 Critical SDR Components

Determining the digital hardware composition of an SDR is a step in the solution of the development of the design. Three main features are considered in the choice of the digital hardware platform (Jacek, 2003; Safadi & Ndzi, 2006; Ulversoy, 2010):

(1) Flexibility and configurability of hardware/software components.

(2) Price and performance trade-offs.

(3) Scalability and support for real-time operations.

The SDR hardware in real-time can be built using a variety of digital hardware consisting of ASIC, DSP, GPP and FPGA. The design of digital hardware includes computer-aided design of logic gates, creation of the schematic diagram, and building the printed circuit board. DSPs present the most commonly used type of hardware that can be programmed to perform almost any function, whereas an FPGA can be configured using logic gates with static functionality .The four different implementation platforms are shown in Figure 2.1.

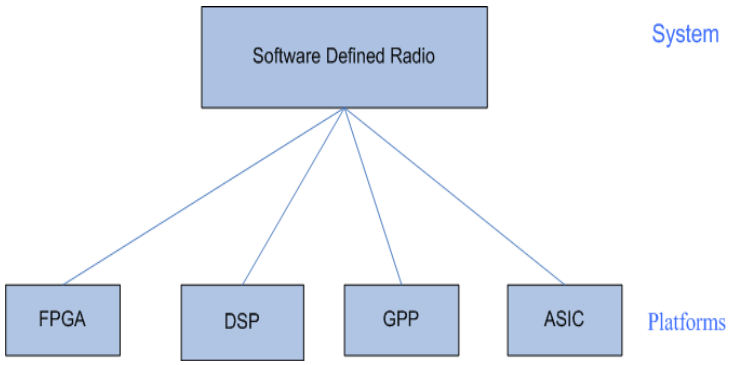

Figure 2.1: Hardware Implementation Platforms for SDR

2.2.2.1 DSP

The heart of the software-defined radios rests in the DSPs units. DSPs are microprocessors with specialised architectures designed to efficiently implement computational algorithms with high performance I/O. DSPs is now required in many application areas, such as wireless communications, audio and video processing, and industrial control systems as a core technology (Lapsley *et al*., 1998).

A recent concept of reconfigurable parallel DSP is based on a carefully dimensioned reconfigurable array fabric, and a number of specialised blocks, all included in SOC. The new DSP architecture is supported by a new programming approach, based on spatial mapping of the signal-processing algorithm to the computing fabric, using tools based around familiar C/C++ approaches (Tuttlebee , 2002).

The main drawback of DSP units is that they lack the suitable processing speeds needed for wideband transmissions. To compensate for inadequate performance, some designers propose that running two DSPs in parallel will result in sufficient function for SDR handsets, and can possibly accommodate the necessary encoding/decoding and symbol processing without the need of ASIC units (Harrington *et al.,* 2004) .High power consumption is another drawback of DSP devices. Mobility is of much concern nowadays including portable wireless devices, and in the future, this demand will likely increase. Many Bluetooth and WiFi products existand the demand for mobile communication will grow, requiring even more efficient DSP techniques.

2.2.2.2 GPPs

Until recently, the fabrication or engraving process for GPPs was one generation ahead of the engraving process for FPGAs. GPPs played a main function in the underlying architecture of all communication equipment although they were always designed to be a flexible computing "workhorse". Though the applications became more specific and demanding, new breeds of specialised processing engines began to emerge. With the data and voice elements of the network still separated, two key

devices were used to boost performance and capacities i.e., the DSP and Network Processors (NP).

GPP devices incorporating wideband vector processors, such as Intel's Xeon processor,have begun to gain acceptance in the wireless community as mainstream signal processing devices. This is evidenced through the acceptance of the Vanu software-defined GSM base station (Safadi & Ndzi, 2006).

2.2.2.3 ASIC

ASICs perform signal down-conversion, digital filtration, and perform at higher rates of speed than FPGAs.The ASIC is very rapid and consumes little power. Thus, it appears to be the only choice available to implement many of the requirements associated with a 3G-air interface. However, the amount of ASIC area and cost required are growing dramatically for 3G systems. It suffers from severe lack of flexibility and very long design cycle. A logic synthesis tool is then used to translate this high-level description into Boolean equations and then onto the logic elements that form the device (Safadi & Ndzi, 2006; Tuttlebee& NetLibrary Inc , 2002).

2.2.2.4 FPGAs

To meet the needs of evolving projects much more easily than a fixed hardware platform, the SDR designers have turned to FPGAs for flexibility. The capability to mix custom hardware for intensive applications, for example, video is also beneficial. FPGAs were introduced in the mid-1980s. An FPGA is a two dimensional array of logic blocks and flip-flops with electrically programmable interconnections between them. These interconnections are identified in Figures 2.2 and 2.3, which

are distinguished in local (or short) and long routing lines. Logic Tiles, also called Logic Slices according to other manufacturers, are the smallest blocks of logic (Nabaa, Azizi, Najm, & Actel, 2006).

The two leading manufacturers of FPGA devices are Altera Corporation and Xilinx Inc. Xilinx FPGA has main families, which are XC3000, XC4000, Virtex, Virtex E, Virtex-II, Virtex-4 etc. However, all these families have the same basic architecture idea with small differences in the logic block. The Xilinx Virtex series was the first line of FPGAs to offer one million system gates. Introduced in 1998, the Virtex product line fundamentally re-defined programmable logic by expanding the traditional capabilities of FPGAs to include a powerful set of features that address board level problems for high performance system designs (MacLean, 2005)

The Virtex-4 family is the latest addition to the Virtex series. Virtex-4 devices incorporate up to 200,000 logic cells, 500MHz performance, and unrivalled features to deliver twice the density, twice the performance, and half the power consumption of previous generation FPGAs. The Virtex-4 family offers three platforms i.e., LX, FX and SX, which are tailored to the requirements of different application domains. Virtex-4 LX is a high-performance logic applications solution. Virtex-4 FX is a high-performance, full-featured solution for embedded platform applications. Virtex-4 SX is a high performance solution for DSP applications.

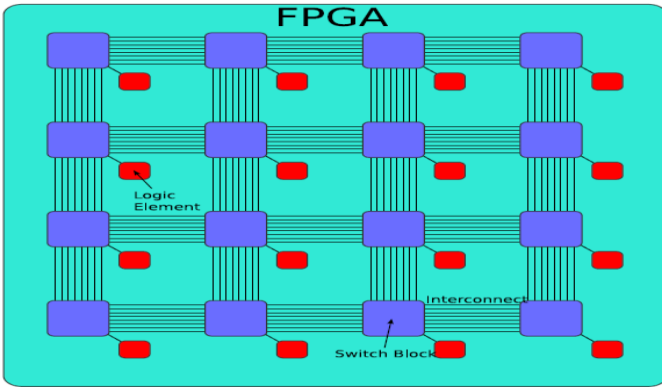

Figure 2.2: Simplified Version of FPGA Internal Architecture (Pietri, 2009).

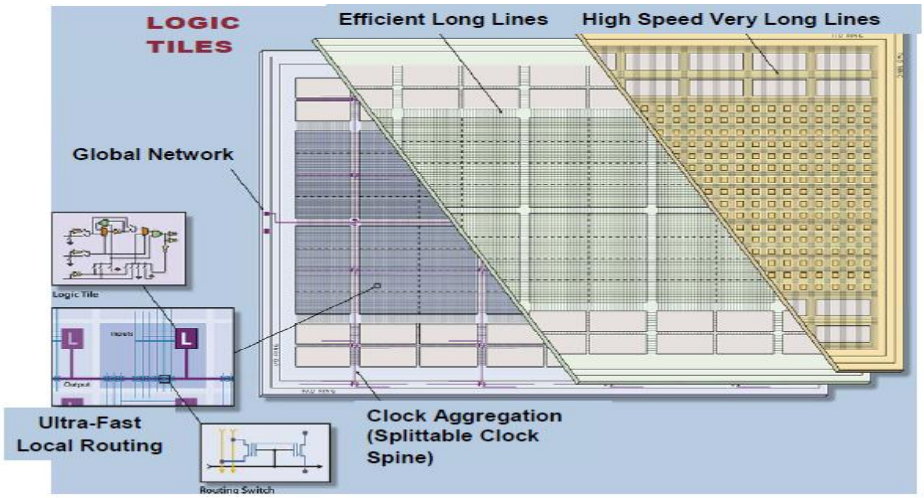

Figure 2.3: Typical FPGA Architecture (Peter, 2007)

Ultimately, there is a global evaluation of the above-mentioned DSP and FPGA, which is illustrated in Table 2.3 (Rapaka, Mody, & Prasad, 2007). It will be suitable to satisfy the instantaneous communication and display the powerful computing capability, if we can integrate the DSP and FPGA processors.

Table 2.3 : The available Digital Signal Processing Devices (Rapaka *et al*., 2007)

Evaluating Category	ASIC	FPGA	DSP	GPP
Programmability	Poor	Good	Excellent	Excellent
Development Cycle	Weak	Fair	Good	Excellent
Performance	Excellent	Excellent	Good	Weak
Power Consumption	Good	Weak	Weak	Weak

2.3 Existing SDR Platforms

Some of the high-performance architectures were reviewed for wireless SDR platform development proposed by the academia industry. One of the most promising hardware platforms in terms of performance is SFF SDR Development Platform from Lyrtech. This thesis uses the SFFSDR platform. The different experimental SDR platforms have made various choices in addressing the issues of flexibility, partitioning and application. To highlight the variety of architectures, eight popular platforms will be discussed briefly.

2.3.1 Universal Software Radio Peripheral (USRP)

USRP1 is a basic SDR platform, developed by a team led by Matt Ettus. The cost of the board is relatively cheap compared to the other SDR platforms. USRP also has a wide frequency range i.e., 0-5GHz. However, that frequency range depends on the type of the accompanying daughter board in use. This is an integrated board, which incorporates AD/DA converters, and some forms of RF front-end. It also includes a FPGA (Xilinx Spartan3), which helps with the high-speed general purpose operations such as digital up and down-conversion, decimation and interpolation. Since this board is mainly for developing software radios, the waveform-specific processing, like modulation and demodulation are usually done in the host processing unit. Typically, a USRP board consists of one motherboard and up to four daughter boards and it requires a PC or MAC with USB2 interface. The first USRP system, released in 2004, was a USB connected to a computer with a small FPGA. USRP1 was not a feasible SDR platform to develop 802.11-compliant ad-hoc test beds. To overcome this limitation, the second-generation platform USRP2 was released in September 2008 and utilises gigabit Ethernet to allow

support for 25MHz of bandwidth (Blossom, 2004; Hasan *et al*., 2010; Tong *et al*, 2009).

2.3.2 NICT SDR Platform

This is a software-defined radio platform development by The Japanese National Institute of Information and Communications Technology (NICT). It consists of two embedded processors, four Xilinx Virtex2 FPGA board, CPU board, and RF boards that could support 1.9 to 2.4 and 5.0 to 5.3GHz. The signal processing was divided between the CPU and the FPGA, with the CPU taking responsibility for the higher layers. Software packages for W-CDMA, IEEE802.11a/b, and digital terrestrial broadcasting, have been developed on the platform. Every software package consists of MAC/DLC layer, physical layer, IP layer, and application layer (Harada, 2005).

2.3.3 Berkeley Cognitive Radio Platform

This platform is a generic multipurpose FPGA based for computationally intensive applications. It is based around the Berkeley emulation engine (BEE2) .The BEE2 consists of, five high-powered Virtex2 FPGAs emulation engine and integrates 500 giga-operations per second, which are able to connect to 18 radio front-end boards via 10 Gbit/s full duplex InfiniBand interfaces. One FPGA is used for control, while the other four are targeted for user applications. Control FPGA runs on Linuxos and has a full IP protocol stack, convenient for connection to laptops and other network devices. User FPGAs are connected to 4GB of DDR2-SDRAM (R. Farrell *et al*, 2009; Tkachenko *et al*, 2006).

2.3.4 Kansas University Agile Radio (KUAR)

KUAR is used in the software-defined radio applications. This radio operates within the 5-6GHz band and is capable of implementing many modulation techniques, media access protocols and adaptation mechanisms. KUAR has five main components - a power source, a control processor, a programmable signal processor with A/D and D/A converters, an RF section, and active antennas. The platform includes, Xilinx Virtex2 FPGA, an embedded 1.4GHz general-purpose processor and supports gigabit Ethernet and PCIexpress connections back to a host computer (Guffey *et al*, 2007; Minden *et al*., 2007).

2.3.5 Maynooth Adaptable Radio System

The Maynooth Adaptable Radio System (MARS) has been in development since 2004. MARS was designed to be flexible, easy to use and inexpensive. To meet these requirements, it was decided to use direct conversion receiver and transmitter architectures. This approach allows large baseband bandwidth, avoids the use of fixed IF filters and has a lower component count than comparable super heterodyne or low IF configurations. Data and control communication is performed via a USB interface between the transceiver and a laptop PC. This platform was to endeavour to deliver a performance equivalent to that of a future mobile telephony base station and wireless communication standards in the frequency range of 1700MHz to 2450MHz.The strength of the MARS platform is in the quality of the RF elements of the circuit (Mora *et al*, 2008).

2.3.6 LYRTECH

LYRTECH also has a single unit SDR solution. This board includes GPP/DSP/FPGA on-board to do all of the signal processing. This system also includes processing on the board and increasing costs while improving the ability to achieving the full range of sample rates. While less expensive than the BEE2, this board is significantly more expensive than the USRP2 (Leferman, 2010)

In this study, the BER measurement of the wireless transceiver implemented uses a modular SFFSDR platform produced by Lyrtech (more details of this platform in Chapter 3).

2.3.7 WARP

The Rice University has developed the Wireless Open-Access Research Platform (WARP). WARP is a programmable wireless research tool that is both scalable and extensible for prototyping and researching the next-generation wireless networks. The custom design of the WARP physical (PHY) layer is tailored to the needs of high-performance wireless communications.WARP is designed to support wide band communication designs. WARP provides a general environment for a clean-slate MAC/PHY development unlike other platforms, which rely on off-the-shelf IEEE 802.11 cards, which limit experimentation only to modifications of existing standards. The main objective of WARP is to provide the community with a flexible wireless research tool. The platform consists of both custom hardware and FPGA implementations of key communications blocks. The hardware consists of FPGA-based processing boards coupled to wideband radios and other I/O interfaces. WARP has similar capabilities for other SDR hardware but costs more than the USRP2. The Radio Board can be tuned to frequencies in the 2.4 and 5.8 ISM bands (Amiri, *et al*., 2007; Murphy *et al*., 2006).

2.3.8 FLEX 3000

The FLEX 3000 is an SDR that uses minimum hardware/analogue components to produce a working frequency range of 10kHz to 60MHz, 100W all mode transceiver and a maximum RF bandwidth of only 48 kHz(FLEX, 2009). The FLEX 3000 falls in the same price range as the USRP products, but the USRP products are not as adaptable as The FLEX 3000 , and being focused on Ham radio applications and frequencies. Most of the low-cost hardware solutions are using 12-bits to 14-bits ADCs and DACs and handle bandwidths ranging from 96 KHz to 8MHz. The leading-edge solutions go up to 16 bits and 70MHz bandwidth or more. Some of the hardware also offers Transmitter and Receiver RF front-ends, usually as daughter boards or mezzanine boards to bring higher frequencies down to within the range of the digital sampling rate.

Table 2.4 show the comparisons of available SDR platforms. The table compares the maximum RF bandwidth of each of the systems; indicates where the processing is done andon what and how the device connects to the computer and costs. The processing partition refersto the location of the processing of the baseband signals, either on the device itself, on ahost system, or a mix of the two. The processing is done using GPPs, or using FPGAs, and GPP/DSP/FPGA-based software radio platform. The cost does not include the cost of the host system or the daughter boards required by each of the systems.