STUDIES OF THE EFFECT OF POST DEPOSITION ANNEALING TO THE CeO_2 THIN FILM ON P-TYPE SILICON AND N-TYPE SILICON CARBIDE SUBSTRATES

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UNIVERSITI SAINS MALAYSIA
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by

CHUAH SOO KIET

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DECLARATION

I hereby declare that this thesis is the result of my own research, that is does not incorporate without acknowledgement any material submitted for a degree or diploma in any university and does not contain any materials previously published, written or produced by another person except where due reference is made in the text.

Thank you.

Signed : _____

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Dated : _____

Signed : _____

Supervisor's name : Assoc. Prof. Ir. Dr. Cheong Kuan Yew

Dated : _____

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LIST OF ABREVATION

AFM	: Atomic force microscope
ALCVD	: Atomic layer chemical vapor deposition
ALD	: Atomic layer deposition
C-V	: Capacitance-voltage
DC	: Direct current
DRAM	: Dynamic random access memories
E-Beam	: Electron beam evaporation
EOT	: Equivalent oxide thickness
FESEM	: Field emission scanning microscope
F-N	: Fowler-Nordheim
GSMBE	: Gas source molecular beam epitaxy
ICDD	: International conference for diffraction data
I-V	: Current-voltage
J-E	: Leakage current density-electric field
J-V	: Leakage current density-electric field
LCR	: Inductance-capacitance-resistance
MBE	: Molecular beam epitaxy
MIS	: Metal insulator semiconductor
MOCVD	: Metal organic chemical vapor deposition
MOD	: Metal organic decomposition
MOS	: Metal oxide semiconductor
PDA	: Post deposition annealing
PLD	: Pulse laser deposition

PMA : Post metallization annealing

RCA : Radio Corporation of America

RF : Radio frequency

RMS : Root mean square

RTA : Rapid thermal annealing

SPA : Semiconductor parameter analyzer

STD : Slow trap density

TEM : Transmission electron microscope

TMA : Trimethylaluminum

XPS : X-ray photoelectron spectroscopy

XRD : X-ray diffraction

XRR : X-ray reflectometry

LIST OF SYMBOL

ΔV_{FB} : Flat band voltage shift (V)

ΔV_g : Difference between the ideal gate voltage and experimental gate

Å : Angstrom

A_G : Gate area (cm^{-2})

B : Slope of the straight line in the F-N tunneling plot

C : Capacitance (pF)

C_{ox} : Oxide capacitance (pF)

D_{it} : Interface trap density (cm^{-2} eV^{-1})

D_{total} : Total interface trap density (cm^{-2})

E : Electric field (MV/cm)

Ec : Conduction band edge (eV)

E_F : Fermi level energy (eV)

E_I : Intrinsic fermi energy (eV)

E_V : Valances band edge (eV)

I : Current (A)

J : Leakage current density (A/cm^2)

k : Dielectric constant

m : Free electron mass

m_{ox} : Effective electron mass in the oxide

n : Refractive index

q : Electron charge (C)

Q_{eff} : Effective oxide charge (cm^{-2})

Q_s : Surface potential

t_{ox} : Oxide thickness (nm)

V : Voltage (V)

V_B : Breakdown voltage (V)

V_{FB} : Flat band voltage (V)

V_G : Gate voltage (V)

ε_o : Permittivity of free space

θ : Angle (^{o})

Φ_B : Barrier height between oxide and semiconductor layer

LIST OF PUBLICATIONS

1. Chuah, S. K., Cheong, K. Y., Lockman, Z., Hassan, Z. (2011). Effect of post-deposition annealing temperature on CeO_2 thin film deposited on silicon substrate via RF magnetron sputtering technique. Materials Science in Semiconductor Processing, 14, pp. 101-107.

2. Chuah, S. K., Cheong, K. Y., Lockman, Z., Hassan, Z. (2011). Effect of post-deposition annealing on electrical properties of RF magnetron sputtered CeO_x gate on 4H-silicon carbide. Physical Status Solidi (a), 208, pp.1925-1930.

KAJIAN TENTANG KESAN PENYEPUHLINDAPAN KE ATAS FILEM NIPIS CeO_2 PADA SUBSTRAT SILIKON JENIS-P DAN SILIKON KARBIDA JENIS-N

ABSTRAK

Filem nipis serium oksida (CeO_2) telah didepositkan di atas substrat silikon (Si) dan silikon karbida (SiC) melalui teknik pemercitan frekuensi radio magnetron. Kesan penyepuhlindapan pada suhu yang berbeza (400, 600, 800 dan 1000^oC) di dalam persekitaran argon (Ar) selama 30 minit telah dikaji ke atas substrat Si jenis-p dan SiC jenis-n. Ketebalan filem nipis CeO_2 pada substrat Si dan SiC adalah dalam lingkungan 30 to 40 nm. Mikroskop imbasan electron dan mikroskop daya atom menunjukkan bahawa kedua-dua filem nipis CeO_2 pada substrat Si dan SiC bebas daripada kecacatan fizikal dan kekasaran permukaan menurun dengan peningkatan suhu penyepuhlindapan. Corak pembelauan sinar-x (XRD) menunjukkan berlakunya fasa CeO_2 dengan empat orientasi pembelauan [(111), (200), (220) dan (311)] dengan lebih memilih arah orientasi (200) untuk semua sampel sistem CeO_2/Si. Bagi sistem CeO_2/SiC, XRD telah menunjukkan kehadiran fasa CeO_2 dengan dua orientasi pembelauan [(111) dan (220)] dengan lebih memilih ke arah orientasi (111). Pengukuran kapasitan-voltan dan arus-voltan dilakukan untuk menyiasat sifat elektrik kapasitor Al/CeO_2/Si dan Al/CeO_2/SiC. Keputusan menunjukkan CeO_2 yang telah disepuhlindap pada suhu 1000^oC bagi kedua-dua substrat Si dan SiC menunjukkan kebocoran arus yang rendah dan kegagalan medan dielektrik yang tinggi.

STUDIES OF THE EFFECT OF POST DEPOSITION ANNEALING TO THE CeO_2 THIN FILM ON P-TYPE SILICON AND N-TYPE SILICON CARBIDE SUBSTRATES

ABSTRACT

Cerium Oxide (CeO_2) thin film has been deposited on silicon (Si) and silicon carbide (SiC) substrates using a radio frequency magnetron sputtering technique. The effect of post deposition annealing at different temperatures (400, 600, 800 and 1000^oC) in argon (Ar) ambient for 30 minutes has been investigated on p-type Si and n-type SiC substrates. The thickness of the CeO_2 thin films on Si and SiC substrates are in the range of 30 to 40 nm. Field emission scanning electron microscopy and atomic force microscopy show that both CeO_2 thin films on Si and SiC substrates are free of physical defects and the root mean square surface roughness are decreasing as the annealing temperature increases. X-ray diffraction (XRD) pattern indicates the occurrence of CeO_2 phase with four diffraction orientation [(111), (200), (220), and (311)] with the preferred orientation of (200) for all the investigated samples in CeO_2/Si system. For CeO_2/SiC system, XRD reveals the presence of CeO_2 phase with two diffraction planes [(111) and (220)] with preferred orientation of (111). Capacitance-voltage and current-voltage measurements are performed to investigate the electrical properties of Al/CeO_2/Si and Al/CeO_2/SiC capacitors. The result shows that the CeO_2 annealed at 1000^oC on both Si and SiC substrates have the lowest leakage current and the highest dielectric breakdown field.

CHAPTER 1

INTRODUCTION

1.1 Research background

In the past few decades, silicon (Si) based metal oxide semiconductor (MOS) devices have achieved superior advancement in terms of better fabrication techniques, high material quality and great device design in leading the microelectronic industry. Nevertheless, Si based MOS devices have limitation in terms of their ability to block high voltage, capability to withstand high electric field and demonstrate low leakage current density (Ranbir, 2006). To overcome these limitations of Si technology, efforts to find a replacement for Si with wide band gap semiconductors have been initiated. Of various wide band gap semiconductors, silicon carbide (SiC) is widely explored for application in high power devices due to its excellent properties (Moon et al., 2010; Lim et al., 2010; Palmieri et al., 2008).

SiC, which is chemically, mechanically and thermally more stable than Si, offers great prospects in the development of high power, high frequency and high temperature devices when compared to those devices based on Si (Moon et al., 2010; Lim et al., 2010; Palmieri et al., 2008). Table 1.1 shows the properties of SiC compared with Si in terms of the dielectric constant (k), band gap, thermal conductivity, breakdown field strength and high electron saturated drift velocity. From Table 1.1, one can see that the breakdown field and the band gap of the SiC are 4 times and 3 times larger than Si, respectively. The dielectric and thermal conductivity value of SiC are also higher than those of Si. Additionally, a stable native silicon oxide (SiO_2) can be grown on top of SiC by thermal oxidation, similar

to Si (Moon et al., 2010; Mahapatra et al., 2009; Palmieri et al., 2008). These excellent properties have enabled SiC to become the preferred choice, as it can be used as a substrate for high power based devices.

Table 2.1: Material properties between Si and SiC

Material Property	Silicon Carbide (SiC)	Silicon (Si)	References
Dielectric Constant (k)	10	3.9	(Tanner et al., 2007)
Band Gap (eV)	3	1.1	(Lim et al., 2010; Robertson, 2004)
Thermal Conductivity (W/cm-K)	4.9	1.4	(Palmieri et al., 2008)
Breakdown field strength (MV/cm)	4	0.3	(Palmieri et al., 2008)
Electron saturated drift velocity (x 10^7cm s^{-1})	2	1	(Palmieri et al., 2008)

Three main concerns are necessary to ensure the high performance of SiC MOS power devices; namely breakdown voltage (V_B), leakage current density (J) and operating temperature. These concerns are governed mainly by the gate dielectric sandwiched between a gate electrode and the SiC substrate as it may affect the performance and reliability of the device (Lori et al., 1999). The gate dielectric which forms between a gate electrode and SiC substrate must show great electrical properties such as low J, high V_B, high electrical field (E) and can withstand high operating temperature (> 600^{o}C) (Moon et al., 2010; Weng et al., 2006).

Radio frequency (RF) magnetron sputtering technique is a well known method in the field of thin film deposition technology. The RF magnetron sputtering

deposition technique is a process whereby an atom on the surface of a solid target is ejected due to the oxide target being bombarded by an inert plasma or a metal target being bombarded by an energetic particle (Wong et al., 2010). This deposition technique can provide a large deposition area within a short period and it is inexpensive (Swaroop et al., 2008; Lee et al., 2004).

1.2 Problem statement

Currently, the best gate oxide used in SiC based MOS devices is nitrided SiO_2 (Lim et al., 2010; Moon et al., 2010; Ranbir, 2006). However, there are still some problems which are preventing large scale usage of nitrided SiO_2 as a gate dielectric (Moon et al., 2010; Cheong et al., 2007). The three main problems are high dielectric semiconductor interface trap density (D_{it}), high J and relatively low k of the material. Due to the k value of SiO_2 (k = 3.9) is much lower when compared with SiC (k = 10), the E across the SiO_2 layer is 2.5 times higher than that in SiC (Tanner et al., 2007; Cheong et al., 2007). This indicates that the MOS device can only operate at E far below the breakdown field of SiC. Thus, the advantages of high E of SiC can be employed.

Over the past decades or so, many researchers have focused on finding solutions to overcome these issues. One approach to overcome this issue is to replace the existing low k nitrided SiO_2 with a high k dielectric material. Lately, numerous high k gate dielectric materials such as Al_2O_3 (Cheong et al., 2007; Avice et al., 2005), oxidized Ta_2Si (Perez et al., 2004; Perez et al. 2006), TiO_2 (Weng et al., 2009; Weng et al., 2006), Gd_2O_3 (Fissel et al., 2006), HfO_2 (Cheong et al., 2007; Wolborski et al., 2007), AlN (Olszyna et al., 2001; Tin et al., 1997; Aboelfotoh et al., 1996),

AlON (Wolborski et al., 2009; Hosoi et al., 2009), CeO_2 (Lim et al., 2010), La_2O_3 (Moon et al., 2006) and Pr_2O_3 (Henkel et al., 2008; Goryachko et al., 2004) have been investigated on SiC based MOS devices using various deposition techniques. In order to explore promising candidates for high k dielectric material, three important aspects need to be considered when selecting a high k dielectric material such as dielectric material properties, gate structure and the dielectric material fabrication process itself (Robertson, 2004; Wild et al., 2001).

Among all the high k dielectric materials studied thus far, cerium oxide (CeO_2) appears as a strong potential candidate to replace nitride SiO_2. CeO_2 is considered as a good high k dielectric material because it shows novel material properties such as large band gap (~ 6 eV) (Ta et al., 2008), high dielectric constant (k = ~ 23-52) (Chiu, 2008; Yamamoto et al., 2005) and a high refractive index (n = 2.2-2.8) (Chiu, 2008; Barreca et al. 2003).

In general, electrical properties of a high k dielectric can be improved by performing a post deposition annealing process (PDA) (Quah et al., 2010; Lim et al., 2010; Fukuda et al., 1998; Pan et al., 2008). The scheme of PDA, namely temperature, ambient and time must be well controlled and optimized in order to obtain the necessary improvement. The positive effect of PDA has been reported in many papers such as in metal-organic decomposed (MOD) CeO_2 thin film on n-type Si and SiC in argon (Ar) ambient (Lim et al., 2010; Quah et al., 2010), oxidation of sputtered ZrO_2 thin film on n-type SiC (Kurniawan, 2009) and in reactive sputtered Sm_2O_3 thin film on Si (Pan et al., 2008).

In this work, the RF magnetron sputtering technique has been used to deposit the CeO_2 thin film on Si and 4H-SiC substrates respectively. Then, PDA was performed to improve the physical and electrical properties of CeO_2 thin film. Up to date, the characteristics of RF magnetron sputtered CeO_2 thin film on Si and SiC substrate at different PDA temperatures in Ar ambient has yet to be investigated. Therefore, the effects of different PDA temperatures (400, 600, 800 and 1000^oC) in Ar ambient on the electrical and physical properties have been investigated systematically.

1.3 Objectives of the research

The main aim of this research is to investigate deposited CeO_2 thin films on Si and SiC substrates by RF magnetron sputtering technique. Several objectives are selected to achieve this purpose are listed below:

- To investigate the effect of the PDA temperatures (400, 600, 800 and 1000^oC) in Ar ambient on CeO_2 thin films deposited on Si and SiC substrates.
- To perform suitable physical and electrical characterizations on the properties of the CeO_2 thin films on Si and SiC substrates.

1.4 Scope of the study

In this study, the RF magnetron sputtering technique is selected to deposit CeO_2 thin films on Si and SiC substrates. The effect of PDA temperatures (400, 600, 800 and 1000^oC) in Ar ambient for 30 minutes is studied systematically. PDA more than 1000^oC is not performed in this work due to it may cause surface reconstructions on the SiC surfaces (Harris et al., 1997). At temperature more than

1000^{o}C The Si will have a tendency to decompose from SiC and cause the graphitization (Harris et al., 1997). This happen may degrade the quality of the SiC surface. Thus, the performance of the MOS devices may be influenced by the graphitization.

The physical characterization are carried out by analysis the surface morphology, root mean square (RMS) surface roughness, surface topography and the orientation of the CeO_2 thin films. Meanwhile, the electrical characterization of CeO_2 thin films are conducted by analysis the capacitance-voltage (C-V) curve, flat band voltage shift (ΔV_{FB}), effective oxide charge (Q_{eff}), interface trap density (D_{it}), total interface trap density (D_{total}), dielectric constant (k), leakage current density-voltage (J-V) curve, leakage current density-electric field (J-E) curve and the barrier height (Φ_B).

1.5 Thesis organization

This thesis is organized into five main chapters. Chapter one (introduction) briefly introduces the research background, problem statement, objectives of the research and scope of the study. Chapter two (literature review) discusses the theoretical background of this research. Chapter Three (materials and methodology) presents the materials and instruments used to produce the CeO_2 thin films on Si and 4H-SiC substrates, explains the experimental procedures and the characterization techniques that are used to conduct in this research. Chapter four (results and discussions) elucidates the results obtained from the experimental work and discusses the outcome of the results. Chapter five (conclusion and recommendation)

presents the conclusion of the results obtained in this research. The recommendations for further studies also are included in this chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 Metal oxide semiconductor (MOS) capacitor

2.1.1 Introduction

MOS structure consists of three layers, which are gate oxide, semiconductor substrate and metal contact layer. MOS structure is one of the useful devices and widely used as a core structure in electronic devices (Schroder, 2006; Donald, 2006). Furthermore, MOS capacitor is extensively used as a device to study the electrical and physical properties of the MOS based devices (Sze et al., 2007). Figure 2.1 presents the structure of MOS capacitor, which consists of an oxide layer that acts as gate dielectric, a semiconductor that acts as substrate and a metal layer that acts as gate electrode.

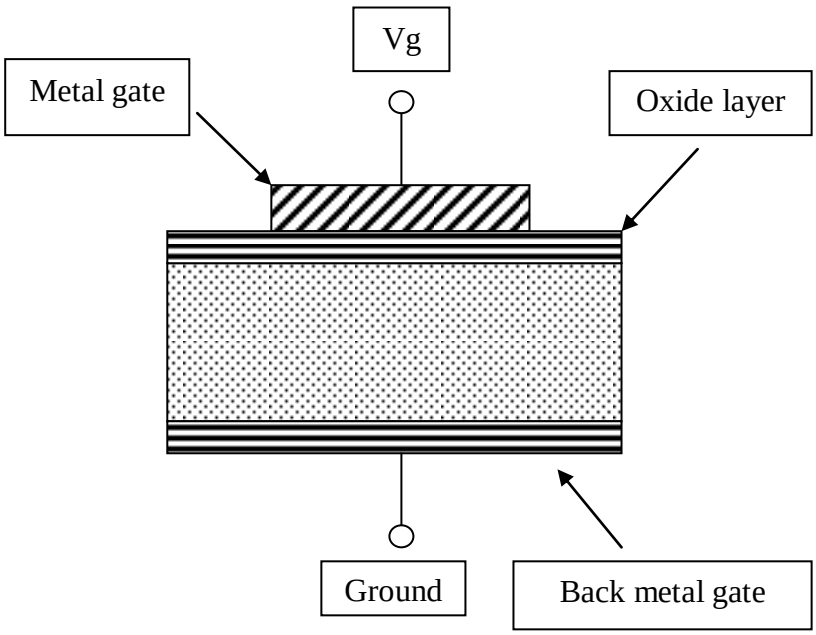


Figure 2.1**:** Metal oxide semiconductor (MOS) capacitor (Sze et al., 2007).

2.1.2 Operation of the MOS capacitor

The energy band diagram of ideal MOS capacitors without any bias is shown in Figure 2.2. The ideal MOS capacitor has the following properties such as: (1) the oxide layer acts as a perfect insulator with no current flowing through the oxide layer under all biasing conditions/resistivity of the oxide layer is infinite (Sze et al., 2007).; (2) no charges exist in oxide layer or at the interface between oxide/semiconductor and (3) the metal gate must be thick enough to act as conduction region under all biasing conditions (Sze et al., 2007; Schroder, 2006).

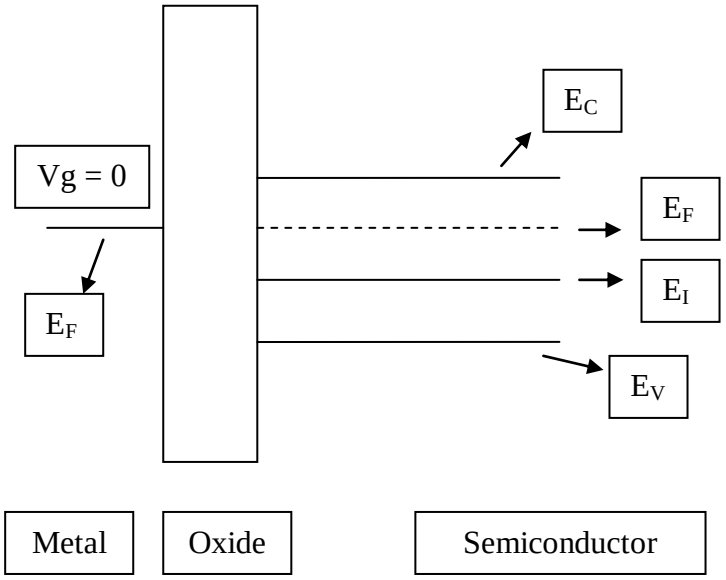


Figure 2.2**:** Energy band diagram for an ideal n-type MOS capacitor at Vg = 0 V (Sze et al., 2007).

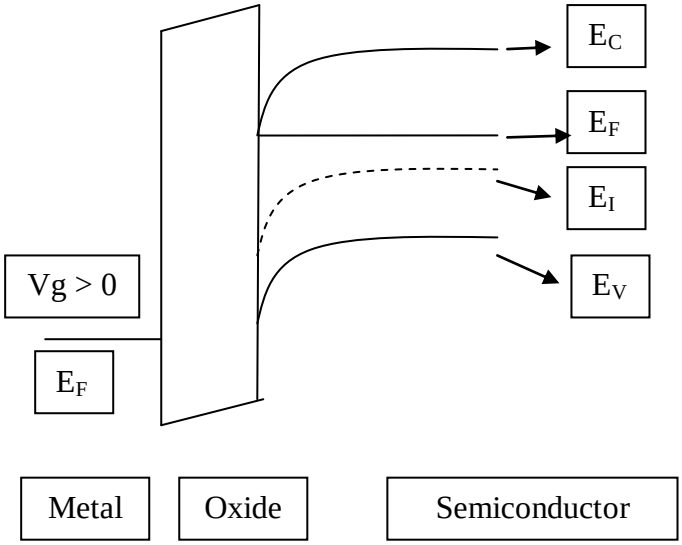


Figure 2.3**:** Energy band diagram for an ideal n-type MOS capacitor under accumulation condition (Sze et al., 2007).

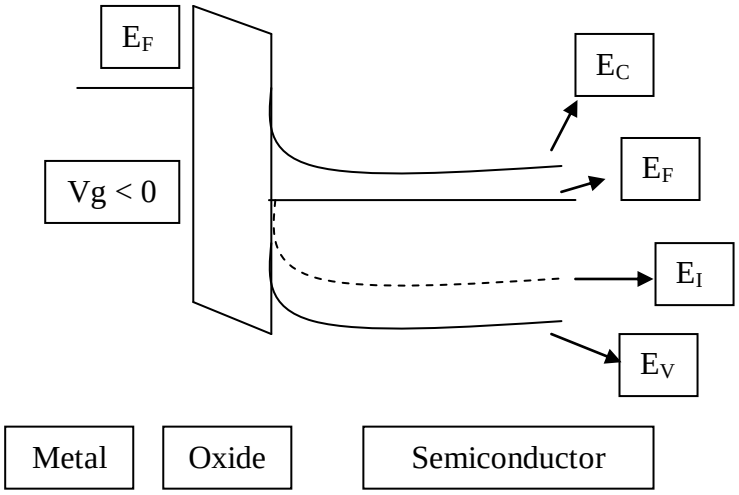


Figure 2.4**:** Energy band diagram for an ideal n-type MOS capacitor under depletion condition (Sze et al., 2007).

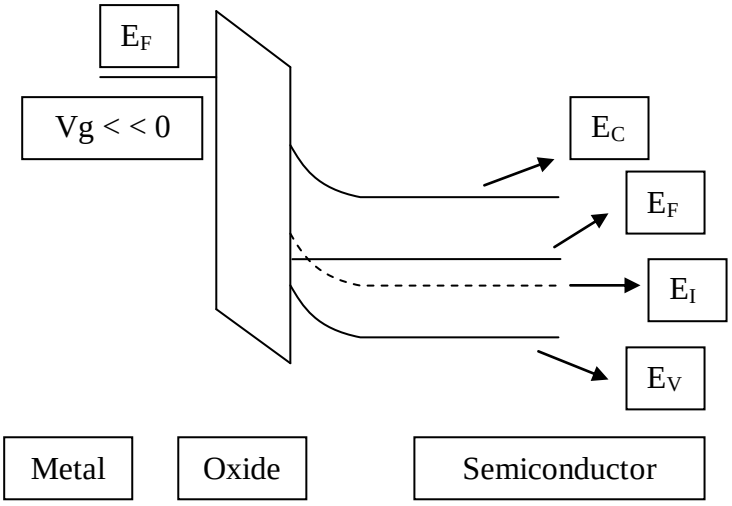


Figure 2.5**:** Energy band diagram for an ideal n-type MOS capacitor under inversion condition (Sze et al., 2007).

When an ideal n-type MOS capacitor is applied with positive bias (Vg > 0), an accumulation condition is obtained. Positive charges are occurs on the metal gate area due to Vg > 0. In this condition, the Fermi energy (E_F) of semiconductor substrate is higher than the E_F of a metal gate layer. Hence, the valence band edge (E_V) bends upward and is closer to the E_F (Figure 2.3). There are great amount of electrons (majority carrier) located near the interface of oxide/semiconductor in this condition.

When an ideal n-type MOS capacitor is applied with small negative bias (Vg < 0), a depletion condition is obtained. Small amount of the negative charge occurs on the metal gate area due to Vg < 0. In this condition, E_V bends downward (Figure 2.4). This occurs owing to E_F of the semiconductor substrate is lower than the E_F in metal gate. Under this condition, the majority carrier (electron) that is located near

the oxide/semiconductor interface is less than the doping concentration of the semiconductor (Sze et al., 2007).

As a larger negative bias is applied to n-type MOS capacitor (Vg << 0), inversion condition appears (Figure 2.5). In this condition, the amount of the holes (minority carrier) is larger than the electrons (majority carrier) near the interface of oxide/semiconductor. The E_F of the semiconductor substrate becomes lower than the E_F in the metal gate as compared to that of depletion condition (Sze et al., 2007).

2.2 Development of the gate oxide on MOS based device

2.2.1 Needs of high k dielectric on SiC substrate

The limitations of SiO_2 gate on SiC have prompted the search of an alternative gate dielectric in order for high power MOS devices to be operated near the breakdown field of SiC. The blocking voltage of SiO_2/SiC devices is limited by the gate dielectric breakdown field instead of the SiC breakdown field (Lim et al., 2010; Tanner et al., 2007; Cheong et al., 2007). The most promising approach to address this issue is by replacing the relatively low k SiO_2 with a high k dielectric material. The requirements of selecting a high k dielectric material deposited on SiC substrate will be reviewed in the next subsection.

2.2.2 High k dielectric requirements

Three important aspects need to be considered when selecting a high k dielectric material, namely: dielectric material properties, gate structure and dielectric material fabrication process (Robertson, 2004; Wilk et al., 2001). These three aspects may eventually influence the electrical and electronic performance of a

MOS device. Table 2.1 shows key requirements of three important aspects while Figure 2.6 shows the correlation between 3 main aspects with the electrical and electronic performance of the MOS device and their key requirements.

Table 2.1: Key requirements of three important aspects.

Aspect	Key Requirements	Reference
Dielectric material properties	- High k dielectric value (~ 10 to 30) - High band offset with SiC - Wide band gap - Thermodynamic and kinetic stable at the gate stack interface - Have good interface quality	Robertson, 2004; Wilk et al., 2001; Chin et al., 2011
Gate structure	- Structure A: single layer (eg: CeO_2/SiC) - Structure B: stacking layer (eg: HfO_2/SiO_2/SiC) - Structure C: stacking layer (eg: Pr_XO_Y/AlON/SiC) - Structure D: stacking layer (eg: Al_2O_3/SiN/SiO_2/SiC)	Moon et al., 2010; Lim et al., 2010; Cheong et al., 2007; Henkel et al., 2008
Dielectric material fabrication process	- Deposition technique - Oxidation condition - Thermal annealing process	Lim et al., 2010; Tanner et al., 2007; Perez et al., 2004; Moon et al., 2006; Zhao et al., 2006

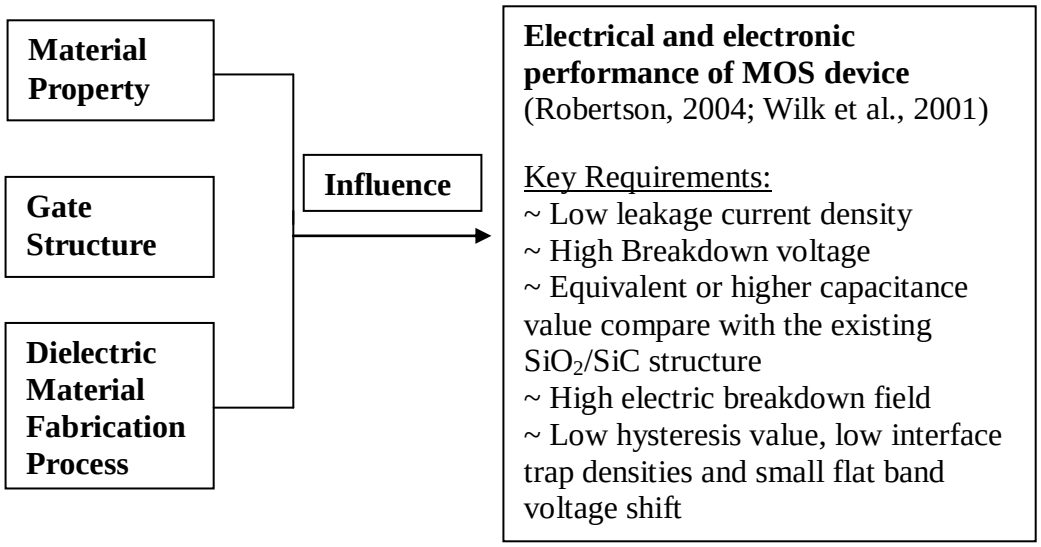


Figure 2.6: Correlation between the 3 main aspects with electrical and electronic performance of MOS devices and its key requirement.

Based on Table 2.1, the new high k dielectric material must show an excellent material property such as high k dielectric value, wide band gap, and large band offset with SiC, thermodynamic and kinetically stable with the gate stack interface and a good interface quality. All these key requirements are important when selecting a promising high k dielectric material.

There are four types of gate structure that have been reported (Figure 2.7). Structure A consists of a single layer of high k dielectric material directly deposited on SiC substrate (high k dielectric/SiC). Structures B and C both are structures with stacking layers on SiC, with structure B having a high k dielectric material deposited on a thermally grown SiO_2 on SiC. The grown SiO_2 acts as a buffer layer on SiC (high k dielectric material/SiO_2/SiC). For structure C, the high k dielectric material is used as a buffer layer instead of using SiO_2 (high k dielectric material/high k dielectric material/SiC). Structure D consists of 3 layers (high k dielectric

material/reaction barrier layer (RBL) (SiN)/SiO_2) on top of a SiC substrate, which Figure 2.7 illustrates four kinds of the gate structure.

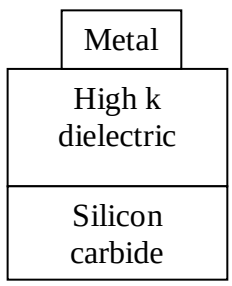
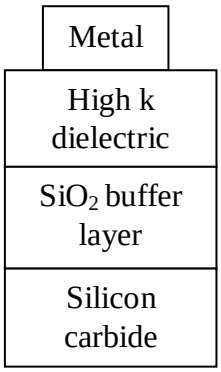
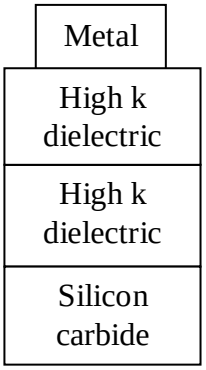
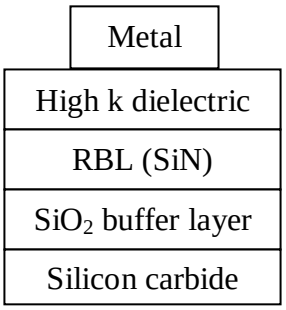
Structure A	Structure B	Structure C	Structure D
High k/SiC	High k/SiO_2/SiC	High k/High k/SiC	High k/RBL/SiO_2/SiC
			
Hoong et al., 2009	Cheong et al., 2007	Henkel et al., 2008	Moon et al., 2010

Figure 2.7: Schematic diagram of four different MOS gate structure.

The dielectric material must be able to be produced by a main stream MOS processing technology. The deposition, oxidation techniques and annealing receipts are among the three key requirements in producing a good layer of high k dielectric material. To ensure the deposited high k dielectric material shows an excellent property, critical understanding (chemical reaction and process fabrication) of each deposition technique is needed. Different deposition techniques may affect crystal structures, interface quality and electrical performance of a high k dielectric material. The papers presented by the researchers (Weng et al., 2009; Wolborski et al., 2009; Hoong et al., 2009; Lim et al., 2010) indicated that the thermal annealing could

improve electrical performance of a device and reduced the electrical defects of the deposited high k dielectric material.

The electrical and electronic performances of a MOS device are deeply influenced by the three aspects stated above, as illustrated in Figure 2.6. The MOS device deposited with a selected high k dielectric material must show a low J (to avoid power consumption and gate oxide reliability), high E and V_B (maximize the use of SiC substrate for high power application), have equivalent or higher capacitance value than SiO_2/SiC structure and less electrical defects (Mahapatra et al., 2009; Cheong et al., 2007; Tanner et al., 2007; Robertson, 2004; Zhao et al., 2006). In the next sub-section, the high k dielectric materials deposited on SiC substrate by various deposition techniques, oxidation and annealing condition will be discussed.

2.2.3 Alternative high k dielectric materials as gate oxide on SiC substrate

In the past few years, there have been extensive works and developments on high k dielectric material on SiC substrate. Many engineering journals, technical papers and technical conferences had reported various high k dielectric materials on SiC substrate using various deposition techniques. This demonstrated the importance of high k dielectric material in the future to replace existing SiO_2/SiC structure in MOS devices. The selected high k dielectric material must fulfil the key requirements illustrated in Table 2.1 before it can be considered as a good high k dielectric material used on SiC substrate. In this section, the deposition techniques, annealing condition and electrical characteristics of various high k dielectric materials on SiC are elucidated. The high k dielectric materials discussed below as

promising candidates to replace SiO_2 layer on SiC are tantalum pentoxide (Ta_2O_5), aluminum oxide (Al_2O_3), aluminum oxynitride (AlON), aluminum nitride (AlN), hafnium oxide (HfO_2), gadolinium oxide (Gd_2O_3), lanthanum oxide (La_2O_3), titanium oxide (TiO_2), cerium oxide (CeO_2) and praseodymium oxide (Pr_2O_3).

2.2.3.1 Tantalum Pentoxide (Ta_2O_5)

Ta_2O_5 is considered as a valuable candidate as high k dielectric material to replace SiO_2 due to its excellent material properties such as high k dielectric constant (25-57) (Perez et al., 2004; Zhao et al., 2006) and have good thermal and chemical stabilities (Zhao et al., 2006). Moreover, Ta_2O_5 also demonstrated good result as dielectric used in dynamic random access memories (DRAM) as well as gate dielectric material on Si system (Perez et al., 2004; Zhao et al., 2006).

Based on Zhao et al. (2006) work, the Ta_2O_5 (~ 60 nm) was sputtered on 4H-SiC using pulse DC magnetron sputtering system. This process took place by sputtering the tantalum target in a chamber with mixture of pure Ar and O_2 gases at room temperature. After the deposition process, the sample was subjected to annealing process (O_2 at 900^{o}C for 30 minutes). Two gate structures were fabricated in this work (Ta_2O_5/4H-SiC and Ta_2O_5/SiO_2/4H-SiC). Results obtained in this work demonstrated that the Ta_2O_5/4H-SiC structure showed high leakage current density (J) as compared with Ta_2O_5/SiO_2/4H-SiC structure. This happened owing to the small band gap of Ta_2O_5 that resulted in a small band offset between the Ta_2O_5 and 4H-SiC which eventually caused large J. Besides that, the Ta_2O_5/SiO_2/4H-SiC structure that went through the annealing process obtained small hysteresis, small amount of slow trap density (STD), small flat band voltage shift (ΔV_{FB}) and interface

trap density (D_{it}) as compared to the as-deposited structure. This indicated that the annealing process was able to reduce the defects on the oxide layer and improved the quality of the Ta_2O_5/SiO_2 interface.

Perez-Tomas et al. (2004) produced the Ta_2O_5 layer by sputtering the Ta_2Si target to deposit a thin layer of Ta_2Si on the 4H-SiC surface and then oxidized in pure O_2 ambient at various temperatures [750 & 850^oC (120 minutes), 950^oC (90 minutes) and 1050^oC (60 minutes)]. Annealing process was done on the samples oxidized at 850 and 950^oC (N_2 ambient at 950 and 1050^oC). According to the AFM result obtained in this work, the surface roughness of the Ta_2O_5 layer decreased as the oxidation temperature increased. The k obtained in this work was ~ 20. In this work, sample that was oxidized at 850^oC and annealed at 950^oC (60 minutes) and annealed again at 1050^oC (60 minutes) had the lowest D_{it} value if compared with other annealed sample (just annealed once at 950^oC). This demonstrated that high temperature annealing initially reduced the defects in the oxide layer and improved the reliability of the oxide layer. Furthermore, this work also demonstrated that thermal oxidation of Ta_2Si as a promising alternative method to produce Ta_2O_5 layer on 4H-SiC substrate.

Another work was reported by Perez-Tomas et al. (2006) using the same technique stated above to deposit a Ta_2Si thin layer. In this work, Perez-Tomas studied the effects of oxidation ambient (O_2 and N_2O) and oxidation time (5 minutes and 60 minutes) for Ta_2Si layer on 4H-SiC at 1050^oC. Sample oxidized at O_2 ambient with longer time (60 minutes) had the best electrical characteristics as compared with another 2 samples (O_2 and N_2 ambient with 5 minutes oxidation

time). Sample with longer oxidation time (60 minutes) in O_2 ambient demonstrated lowest D_{it} and J, small ΔV_{FB} and highest V_B and E as compared with others samples. As conclusion, the performance of oxidation in O_2 was better than in N_2O environment under same annealing condition while sample with longer oxidation time in O_2 ambient showed less interface defects in the oxide layer due to good electrical characteristics.

Investigation of direct sputtered Ta_2Si on 4H-SiC or SiO_2/4H-SiC structure was reported by Perez-Tomas et al. (2008). 50 nm thick Ta_2Si thin layer had been deposited on 4H-SiC (O-Ta_2Si) and SiO_2 (SiO_2/O-Ta_2Si). After the deposition, samples were sent for oxidation process (O_2 ambient at 1050^oC for 60 minutes) followed by annealing process for 60 minutes at 950^oC in Ar ambient. Both structure showed smooth surface obtained from AFM images. The O-Ta_2Si structure showed lowest D_{it} value as compared with SiO_2/O-Ta_2Si structure whiles the lowest J value and highest breakdown voltage was gained by SiO_2/O-Ta_2Si structure.

Figure 2.8 illustrates the comparison of leakage current density-voltage (J-V) characteristics of various experiments conducted by researchers. It can be noticed that research conducted by Perez et al. (2008) shows the lowest J and high V_B as compared with other experiments.

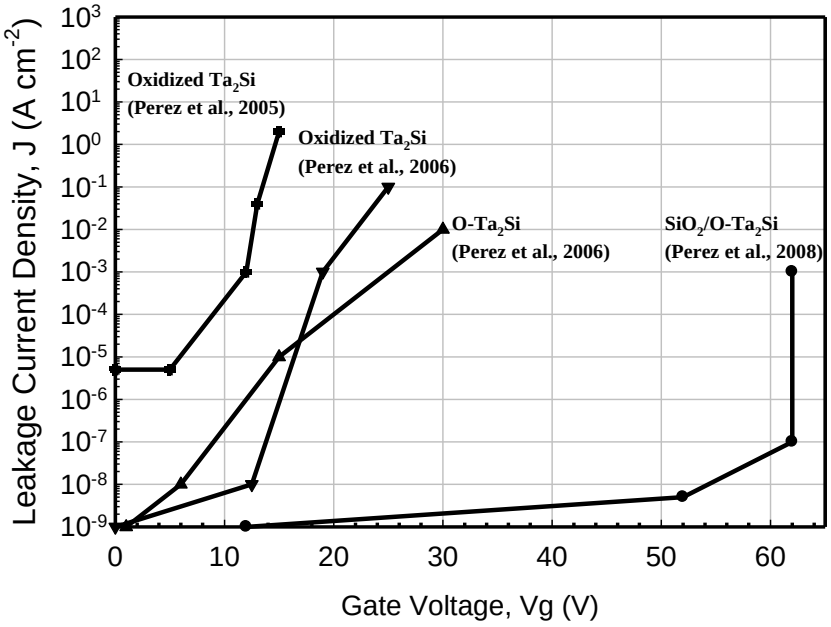


Figure 2.8: Comparison on J-V characteristics of Ta_2O_5 on SiC substrate reported in literatures. The data obtained from literatures were adapted as accurately as possible using a linear approximation (Perez et al., 2005; Perez et al., 2006; Perez et al., 2008; Perez et al., 2006).

Figure 2.9 presents D_{it} characteristics of Ta_2O_5 on SiC substrate reported by researchers. The D_{it} value obtained from researches were between 1 x 10^{11} cm^{-2} V^{-1} and 1 x 10^{12} cm^{-2} V^{-1} at Ec-E = 0.5 eV. This indicated that the Ta_2O_3 demonstrated low D_{it} value when deposited on 4H-SiC and this eventually would help to improve the J and V_B of the device.

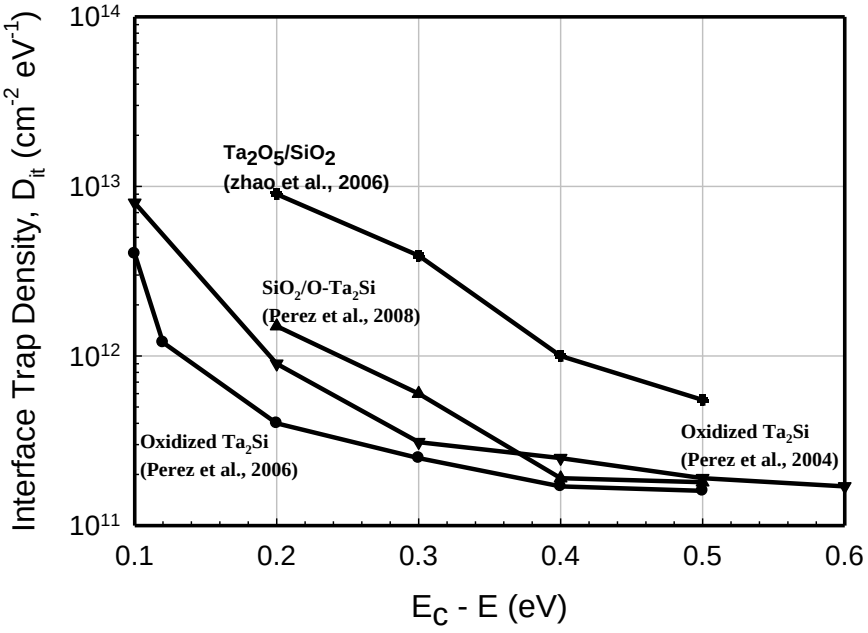


Figure 2.9: Comparison on D_{it} characteristics of Ta_2O_5 on SiC substrate reported in literatures. The data obtained from literatures were adapted as accurately as possible using a linear approximation (Zhao et al. 2006; Perez et al., 2004; Perez et al., 2006; Perez et al., 2008).

2.2.3.2 Hafnium Oxide (HfO_2)

HfO_2 appears as attractive high k dielectric material to replace traditional SiO_2 as gate oxide since it shows high dielectric constant (~ 20-25) (Tanner et al., 2006) and demonstrated good electrical characteristics on Si system (Tanner et al., 2006). Furthermore, many techniques can be used to deposit the HfO_2 on the SiC substrate (Hoong et al., 2009; Tanner et al., 2006; Wang et al., 2008).

Hino et al. (2006) reported that HfO_2 could be deposited on 4H-SiC using metal organic chemical vapour deposition technique (MOCVD). In this work, an effect of various deposition temperatures (190, 240, 280 and 400^{o}C) on

characteristics of HfO_2 was investigated. Low temperature deposition (190^oC) of the HfO_2 showed low J (> 10^{-4} A/cm^2) as well as had low D_{it} (2 x 10^{12} eV^{-1} cm^{-2} at 0.2 V) value when compared with the thermally grown SiO_2/SiC structure. Additional, the X-ray photoelectron spectroscopy (XPS) result illustrated that less SiO_x ($x < 2$) bonds were obtained from sample deposited at 190^oC as compared with sample deposited at 400^oC.

Based on the paper presented by Wolborski and co-researchers (Wolborski et al., 2007), HfO_2 was deposited directly on 4H-SiC substrate and on thermally grown SiO_2/4H-SiC structure using atomic layer deposition (ALD) technique at 250^oC. Thicknesses of thermally growth SiO_2 were 8 nm and 13 nm, respectively. The stacking structure (HfO_2/SiO_2/4H-SiC) demonstrated better results as compared with the single structure (HfO_2/4H-SiC). The highest electric breakdown field was achieved by stacking structure with 8 nm SiO_2 (6.6 MV/cm) as compared with 13 nm SiO_2 (4.0 MV/cm) and single structure (6.2 MV/cm). This indicated that the thickness of the SiO_2 buffer layer used must be less than 13 nm to achieve better electrical performance. However, the result shows that the stacking structure was not suitable to be used for high temperature. This was due to when operated at temperature more than 400^oC; a reaction between SiO_2 and HfO_2 was performed at this temperature and eventually would affect the electrical performance of the device. Nevertheless, the successful of the good quality SiO_2/SiC interface had reduced the D_{it} and J.

Sol-gel spin on coated HfO_2 thin film on 4H-SiC was reported by Wang and Cheong (Wang et al., 2008). The effect of different annealing temperatures (550, 750

and 850°C) in Ar ambient for 30 minutes on physical and electrical characteristics of HfO_2 was studied. As the annealing temperature increased from 750°C to 850°C, a phase transformation from monoclinic phase HfO_2 to orthorhombic phase HfO_2 was observed from XRD. The refractive index obtained in this work ranged from 1.83 to 2.13. Sample annealed at 700°C revealed best device performances owing to lowest J and D_{it} value, highest refractive index and k as compared another two annealed samples. Vice versa, the sample annealed at 850°C demonstrated worst oxide reliability.

Electrical characteristics of the HfO_2 thin film on 4H-SiC deposited using sol-gel spin on coating technique at different annealing temperatures (850, 950 and 1050°C) for 30 minutes in forming gas (5% H_2 in 95% N_2) had been investigated by Hoong and Cheong (Hoong et al. 2009). All samples demonstrated negative ΔV_{FB} indicated the occurrence of positive effective oxide charge (Q_{eff}) in the oxide layer. Sample annealed at 850°C demonstrated the lowest total interface trap density (D_{total}) and D_{it} value. This eventually influenced the J value, in which sample with the lowest annealing temperature (850°C) had the least J value. Results obtained in this work show that, J value increased as the annealing temperature increased.

Interface and carrier transport behavior in Al/HfO_2/SiC structure using electron beam deposition (E-Beam) technique was reported by Mahapatra and co-authors (Mahapatra et al., 2009). In this study, a metallic Hf was evaporated by E-Beam to produce a thick layer of HfO_2 (25 nm) on SiO_2/SiC structure. After deposition, sample was sent for oxidation (O_2 for 60 minutes at 650°C). The D_{it},

barrier height (Φ_B) and oxide trap charge gained from this experiment were ~ 7 x 10^{11} eV^{-1} cm^{-2} at Ec-E = 0.2 eV, ~ 1.5 eV and ~ 4.8 x10^{11} cm^{-2}, respectively.

Cheong et al. (2007) investigated the electronic performance of stacking gate dielectric of HfO_2/nitrided SiO_2/4H-SiC. 13 nm HfO_2 layer was deposited on nitrided SiO_2/4H-SiC structure using ALD technique. 3 different thicknesses (2, 4 and 6 nm) of the nitrided SiO_2 were formed between the HfO_2 layer and 4H-SiC substrate. Stacking structure with different thickness of nitrided SiO_2 showed low hysteresis and Q_{eff} value as compared with single structure (HfO_2/4H-SiC). This proposed that STD and ΔV_{FB} in the stacking structure was much lower than the single structure. The improvement of stacking structure as compared with the single structure was a result of the difference in conduction band offset of HfO_2/SiC and HfO_2/SiO_2/4H-SiC. Among different thicknesses of the nitride SiO_2 layer, nitrided SiO_2 with 6 nm thick presented the lowest D_{it}, D_{total} and Q_{eff} value and the highest dielectric reliability and E as compared with other stacking samples.

Figure 2.10 shows comparison on leakage current density-electric field (J-E) characteristics of HfO_2 on SiC reported by researches. Research conducted by Cheong et al. (2007) illustrated the lowest J value and the highest E as compared with other works. It was observed that by applying a layer of SiO_2 between the HfO_2 and SiC substrate, it could improve the electrical performance of the device as compared without the SiO_2 layer.