EFFECT OF GROWTH TEMPERATURE AND CATALYST ON THE FORMATION OF ONE-DIMENSIONAL SILICON NANOSTRUCTURES VIA THERMAL EVAPORATION TECHNIQUE

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by

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In The Name of Allah, The Most Merciful, The Most Compassionate Peace and Blessing be Upon His Beloved Prophet Muhammad

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LIST OF ABBREVIATIONS

AFM	Atomic Force Microscopy
Ar	Argon
Au	Aurum
AuPd	Aurum-palladium
C	Carbon
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon nanotube
CNWS	Carbon nanowires
Cu	Copper
CVD	Chemical Vapor Deposition
EDX	Energy Dispersive X-ray
Fe	Ferum
FESEM	Field emission scanning electron microscope
FET	Field-effect transistors
Ge	Germanium
HCl	Hydrochloric acid
HF	Hydrogen fluoride
H_2O_2	Hydrogen peroxide
IC	Integrated circuit
ICDD	International Conference for Diffraction Data
In	Indium
MBE	Molecular beam epitaxial
MOFSET	Metal oxide semiconductor field-effect transistor
MOS	Metal oxide semiconductor

NH_4OH	Ammonium hydroxide
Ni	Nickel
OAG	Oxide-assisted-growth
PECVD	Plasma-enhanced chemical vapor deposition
PL	Photoluminescence
Pd	Palladium
RCA	Radio Corporation of America
RTDs	Resonant- tunneling diodes
SEM	Scanning electron microscope
SETs	Single-electron-transistors
Si	Silicon
SiNWs	Silicon nanowires
SiO_2	Silicon dioxide
SiO_x	Silicon oxide
SPA	Semiconductor parameter analyzer
SPM	Scanning probe microscope
STM	Scanning tunneling microscope
TEM	Transmission electron microscope
VLS	Vapor-liquid-solid
XRD	X-ray Diffraction
0D	Zero-dimensional
1D	One-dimensional
2D	Two-dimensional

LIST OF SYMBOLS

A	Area	m^2
d	Diameter	m
I	Current	A
R	Resistance	Ω
V	Voltage	V
σ	Conductivity	$(\Omega\ cm)^{-1}$
ρ	Resistivity	Ω cm

KESAN SUHU PERTUMBUHAN DAN MANGKIN KE ATAS PEMBENTUKAN SATU-DIMENSI SILIKON BERSTRUKTUR NANO MELALUI TEKNIK PENGEWAPAN TERMA

ABSTRAK

Pembentukan silikon berstruktur nano melalui teknik pengewapan terma telah dikaji dengan fungsi suhu penyepuhlindap dan pemangkin yang memainkan peranan penting dalam proses ini. Serbuk silikon sebagai bahan mentah telah digunakan bagi membolehkan pengewapan berlaku pada suhu yang tinggi (900-1100^{o}C) dalam aliran gas argon (Ar). Silikon berstruktur nano telah dikumpulkan pada permukaan substrat silikon (111) yang dilapisi dengan atau tanpa pemangkin pada jarak yang berbeza dari sumber bahan mentah. Dengan mengawal kadar pemanasan, kadar aliran gas, suhu dan masa sepuhlindap, kedudukan dan lokasi substrat, pada keadaan yang optimum, silikon berstruktur nano yang terbaik telah berjaya dihasilkan. Dalam kajian ini, parameter yang terbaik untuk menghasilkan silikon berstruktur nano adalah pada suhu 1100°C dengan kadar pemanasan 20°C/min dalam aliran Ar 100 ml/min; di mana satu-dimensi (1D) silikon berstruktur nano tumbuh di atas substrat yang berada 6cm daripada sumber bahan pada keadaan mendatar dalam 3 jam masa pertumbuhan. Perbezaan jenis pemangkin yang digunakan memberi kesan ke atas silikon berstruktur nano yang diperolehi. Bagi pemangkin emas (Au), silikon berstruktur nano dengan diameter antara 50 nm hingga 100 nm diperolehi. Sementara untuk mangkin aloi emas-paladium (AuPd), silikon nanowayar dengan diameter antara 20 nm hingga 40 nm dihasilkan, mempunyai struktur sfera yang mengandungi AuPd pada hujung wayar dengan diameter 40 nm yang dilihat. Berdasarkan kajian ini, mekanisme pertumbuhan silikon berstruktur nano sesuai dengan mekanisme

wap-cecair-pepejal (VLS). Di samping itu, sampel tanpa mangkin dengan pengaruh masa sepuh lindap (1 jam dan 3 jam) pada pembentukan silikon berstruktur nano juga dikaji. Didapati bahawa faktor ini mempengaruhi morfologi struktur, di mana silikon berstruktur nano yang mempunyai diameter 30 nm hingga 100 nm telah diperolehi. Berdasarkan keputusan ini, mekanisme pertumbuhan silikon berstruktur nano mengikut mekanisme pertumbuhan dibantu-oksida (OAG).

EFFECT OF GROWTH TEMPERATURE AND CATALYST ON THE FORMATION OF ONE-DIMENSIONAL SILICON NANOSTRUCTURES VIA THERMAL EVAPORATION TECHNIQUE

ABSTRACT

The formation of silicon nanostructures, via thermal evaporation techniques, was studied as a function of annealing temperature and catalyst (Au and AuPd).The silicon powder, serving as the starting source material, was evaporated at a high temperature (900-1100°C) in the flow of argon gas. Grown silicon nanostructures were collected on (111) a silicon substrate surface. The substrate, coated with or without catalyst, was placed at different distances from the source material. By controlling the heating rate, gas flow rate, annealing temperature and time, substrate position, and location, silicon nanostructures can be produced. In this work, the best parameter to produce silicon nanowires is by using a temperature of 1100°C, with a heating rate of 20°C/min, and an Ar flow rate of 100 ml/min. Under these conditions, one dimensional silicon nanostructures will grow on a horizontally-positioned substrate, provided that it is located 6cm from the source material and the time of growth, is 3 hours. Different types of catalyst will affect the morphology of the silicon nanostructures obtained. If an Au catalyst is used, the nanostructures, with diameters ranging between 50 nm to 100 nm, will be obtained. Meanwhile if AuPd is used, a bundle of silicon nanowires, with diameters ranging between 20 nm to 40 nm and a high conductivity of 1.117 $x10^{-4}(\Omega\ cm)^{-1}$, will be produced. Spherical AuPd at the tip of the structures, with a diameter of 40nm, were also observed. The silicon nanostructure's growth mechanism is in agreement to the well-known Vapor-Liquid-Solid (VLS) mechanism. Besides that, the effect of the annealing time (1 hour and 3 hours) on the formation of silicon nanostructures was studied for samples without a

catalyst. This factor influenced the morphology of the structures, where silicon nanostructures with diameters ranging from 30 nm to 100 nm, were obtained. Based on this result, the silicon nanostructure's growth mechanism is an Oxide-Assisted-Growth (OAG).

CHAPTER 1

INTRODUCTION

The requirement for multi-compact devices, such as the iPhone and the iPad, has been growing at a high rate, putting pressure on manufacturers to fit more powerful electronic circuits, into smaller packages. However, while Moore's Law has so far been a reliable measure of this progress, limits of current manufacturing methods have been identified. Solutions are now involving nanotechnology, specifically the use of nanotubes and nanowires. As the name suggests, nanowires are wires with dimensions in nanometres. Although many research works have been conducted on Carbon-Based Nanotubes (CNTs) and nanowires (CNWs), not many have focused on Silicon Nanowires (SiNWs) (Wei and Charles, 2006). In this study, the fabrication of SiNWs, via a thermal evaporation technique, was studied.

1.1 Overview of One-Dimensional Systems

One-dimensional silicon nanostructures have attracted much attention in recent years, for their valuable electrical and optical properties, as well as their potential applications in mesoscopic research and nanodevices (Jun *et al.*, 2006). This is because they showed electronic, optical, chemical, mechanical, and thermal properties, different to their bulkier counterparts (Stelzner *et al.*, 2007). Moreover, silicon nanowires offer the possibility of integration with conventional silicon integrated circuit technology (Kwak *et al.*, 2006).

There are two approaches for synthesizing silicon nanowires, namely; top-down and bottom-up. Lithography is an example of a top-down approach, while bottom-up strategies, include laser ablation, Chemical Vapor Deposition (CVD), and thermal evaporation. Since the thriving development of nanotechnology is governed by the successful growth of nanomaterials with pre-determined morphology and chemical composition, the currently employed top-down approach of defining silicon nanowires by the lithography technique, is approaching its limits in regards to equipment and cost barriers. Furthermore, the quality of the silicon nanowires is limited as a consequence of process induced damage (Rao *et al*., 2003).

The most common method currently used for synthesized silicon nanowires, is CVD. Slight variations of this technique include the widely used Plasma-Enhanced Chemical Vapor Deposition (PECVD). Any process that uses CVD generally uses the Vapor-Liquid-Solid (VLS) technique for the fabrication of silicon nanowires. In the VLS technique, a catalyst metal droplet acts as a site for the vapor-phase adsorption of Si atoms (Elder *et al.*, 2006). Nanowires achieved by this crystal growth mechanism are catalysed by a metal eutectic nanodroplet. Therefore, metallic nanoparticles play a key-role in the VLS process. Due to its physical and chemical properties, a gold catalyst is frequently used. However, many other catalysts, such as nickel (Ni) or copper (Cu), can be used. Zhou and co-workers (2006) demonstrated that homogenous nanowire diameters can be controlled by the size of the catalyst droplet.

Silicon whisker was first discovered by Wagner and Ellis in 1964, with diameters from 100 nanometers to hundreds of microns. This was described in detail by Givargizov in 1975 (Cao, 2004). However, according to the current demand for systematic nanostructure synthesis and the progress in the formation technique of metal nanosized particles, there is a transformed interest in the VLS technique.

In a VLS growth, the growth species are firstly evaporated, and then diffused and dissolved into liquid droplets. The surface of the liquid has a large area; therefore, it is a preferred site for deposition. The saturated growth of species in the liquid droplet will diffuse into the precipitate at the interface between the crystal growths. Continued precipitation or growth will separate the substrate and the liquid droplet, resulting in nanowire growth (Cao, 2004). Finally, silicon nanowires of a high purity are obtained, except at the tip, which contains the solidified metallic catalyst.

This metal particle plays the role of the catalyst and determines the diameter of the nanostructures. Hence, the choice of the metal catalyst depends on its physical and chemical properties, which eventually determines many of the nanowire's properties. To find a suitable metal, the phase diagram is first consulted in order to select a metal that can form a liquid alloy with the nanowire material of choice.

1.2 Problem Statement

Park *et al.,* (2007)*;* Liu *et al.,* (2000)*;* Niu *et al.,* (2004), have successfully fabricated silicon nanowires using Au and AuPd as catalysts, via VLS, using Si

wafer as the source. However, there are no reports on the effects of substrate location during thermal evaporation. Therefore, in this work, the thermal evaporation method has been applied, in order to fabricate silicon nanowires using Au and AuPd catalysts, deposited on a silicon wafer, using silicon powder as a source. To date, no other work has reported about use Si powder as the source. The thermal evaporation method has been applied in this study to grow nanowires, because it is a simple and easy procedure. Traditionally, the fabrication of silicon nanowires using a catalyst, involves a complicated deposition to replace a layer of the catalyst, on the substrate. Therefore, in this work, a simple sputtering coated deposition method has been used for AuPd and Au as catalyst layer.

In addition, the optimum substrate location has also been investigated. The quality of the silicon nanowires can be judged by their morphology. Accordingly, a series of tests, involving the location of the substrate from the source material, with different growth temperatures, was performed in order to determine the optimum condition to produce one-dimensional silicon nanostructures.

1.3 Objectives of the Project

The goal of this study is to achieve the following objectives:

1. To synthesize one dimensional silicon nanostructures, using a thermal evaporation technique, with and without a metal catalyst.
2. To characterize the morphology and electrical properties of the silicon nanostructures formed.
3. To determine the optimum conditions (location and catalyst) for the formation of one-dimensional silicon nanowires.

1.4 Scope of the Project

The scope of this study is the synthesizing and the characterizing of silicon nanowires by a thermal evaporation technique, either with or without a catalyst. A simple sputter coating was performed to prepare the thin layer of metal catalyst on the silicon substrate that was required for the synthesis of silicon nanostructures, by the VLS mechanism. Observation of the structure, morphology, topography, and composition of the silicon nanostructures, was carried out to evaluate the optimum parameters, which would achieve a successful growth of silicon nanostructures. The structures were investigated using X-ray diffraction (XRD) and the morphology and elemental composition was investigated using FESEM (equipped with an EDX spectrometer). Transmission Electron Microscopy (TEM) and Scanning Probe Microscopy (SPM) were used to determine the size, shape, and topography, of the silicon nanostructures. In order to investigate the electrical properties of the silicon nanostructures, a Conductive-Atomic Force Microscope (CAFM) and a Semiconducting Parameter Analyser (SPA) were used to determine their resistivity and conductivity.

CHAPTER 2

LITERATURE REVIEW

2.1 Nanotechnology

Nanotechnology is defined as the science of materials and systems with structures and components which display improved novel physical, chemical and biological properties; phenomena that exist in the nanosize (1-100 nm) (Wang, 2008). The word *nano* means 10^{-9}, or one billionth of a meter. As comparison, a virus is roughly 100 nanometers (nm) in size. Nanotechnology can work from top-down (which means reducing the size of the smallest structures to nanoscale such as photonics applications in nanoelectronic and nanoengineering) or bottom-up (which involves manipulating individual atoms and molecules structures and more closely resembles chemistry or biology) (Wilson, 2002). Materials at the nanosacale often exhibit very different properties than their normal size counterparts. These differences includes the physical strength, chemical reactivity, electrical conductance, magnetism and optical effect (Silva, 2004).

2.1.1 Nanostructures and nanomaterials

In this modern day, nanostructures and nanomaterials became the well-known terms used by researchers and experts to study as a result of their peculiar and fascinating properties and applications superior to their bulk counterparts. The capabilities to produce such small structures are important in modern science and technology as there are many opportunities that might be realized by these new types of nanostructures. In microelectronics, the smaller meant have a greater performance

in invention of integrated circuits where the more components per chip resulted in a faster operation, lower cost and less consumption (Xia *et al*, 2003).

Miniaturization may also represent the development in a range of other technologies. As example in information storage there are many active efforts to develop magnetic and optical storage components with critical dimensions as small as ten of nanometers. It is also clear that a wealth of interesting and new phenomenon are associated with nanometer-sized structures, with the best established examples including size dependent excitation or emission, quantized (or ballistic) conductance, coulomb blockade and metal-insulator transition. It is generally accepted that quantum confinement of electrons by the potential wells of nanometer-sized structures may provide one the most powerful and (yet versatile) means to control the electrical, optical, magnetic, and thermoelectric properties of a solid-state functional material (Xia *et al*, 2003).

Nanostructures and nanomaterials are classified according to dimensionality of their elements, since bulk materials are considered three-dimensional (3D) structures. According to (Wang, 2000), there are three different classes of nanostructures;

i. zero-dimensional (0D) nanostructures : nanoparticle
ii. one-dimensional (1D) nanostructures : nanotube or nanorod
iii. two-dimensional (2D) nanostructures : nanodisk

2.1.2 Method of synthesizing nanosized materials

There are basically two approaches to produce nanomaterials which top-down and bottom-up methods. The bottom-up approach of nanomaterials synthesis first forms the nanostructure building blocks (nanoparticles) and then assembles them into the final materials. An example of this approach is the formation of powder components through aerosol techniques and then the compaction of the components into the final material. These techniques have been used extensively in the formation of structural composite nanomaterials (Cohen, 2001; Demami et al., 2010).

The top-down approach begins with a suitable starting material and then "sculpts" the functionality from the material. This technique is similar to the approach used by the semiconductor industry in forming devices out of an electronic substrate (silicon), using pattern formation (such as electron beam lithography) and pattern transfer processes (such as reactive ion etching) that have the necessary spatial resolution to achieve creation of structures at the nanoscale. This particular area of nanostructure formation has tremendous scope and is a driving issue for the electronic industry. The best known example of top-down approach is the photolithography technique used by the semiconductor industry to create integrated circuits by etching patterns in silicon wafers (Hu *et al*, 1999; Demami *et al*., 2010)

2.2 Strategies for achieving 1D growth

The essence of 1D nanostructure formation is about crystallization, a process that has already been investigated for hundreds years. The development of solid structure from vapor, liquid, or solid phase involve two fundamental steps: nucleation and growth. As the concentration of the building blocks (atoms, ions or

molecules) of solid becomes sufficiently high, the aggregate into small clusters (or nuclei) through homogenous nucleation. Therefore, with a continuous supply of the building blocks, these nuclei can serve as seeds for further growth to form larger structures.

In (2003), Xia *et al*., reported that the formation of perfect crystal requires a revisable pathway between the building blocks on the solid surface and those in a fluid phase (i.e., vapor, solution or melt) generally was accepted. These conditions allow the building blocks to accept easily correct positions in developing in the long-range-ordered, crystalline lattice. In addition the building blocks also need to be supplied at a well controlled, rate to obtain crystals having a homogenous composition and uniform morphology.

In fabricating nanostructures, the most important issue that one needs to be addressed is the simultaneous control over dimensions, morphology and monodispersity. In the past several years, a variety of chemical methods have been demonstrated as the bottom-up approach for generating 1D nanostructures with different levels of control over these parameters. Figure 2.1 shows schematically illustrates of these synthetic strategies that include i) use of the intrinsically anisotropic crystallographic structure of a solid to accomplish 1D growth Figure 2.1(A); ii) introduction of liquid solid interface to reduce the symmetry of seed Figure 2.1(B); iii) use various templates with 1D morphologies to direct the formation of 1D nanostructures Figure 2.1(C); iv) use of supersaturation control to modify the growth habits of seed; v) use of appropriate of various facets of a seed

Figure 2.1(D); vi) self assembly of 0D nanostructures Figure 2.1 (E); vii) size reduction of 1D microstructure Figure 2.1 (F).

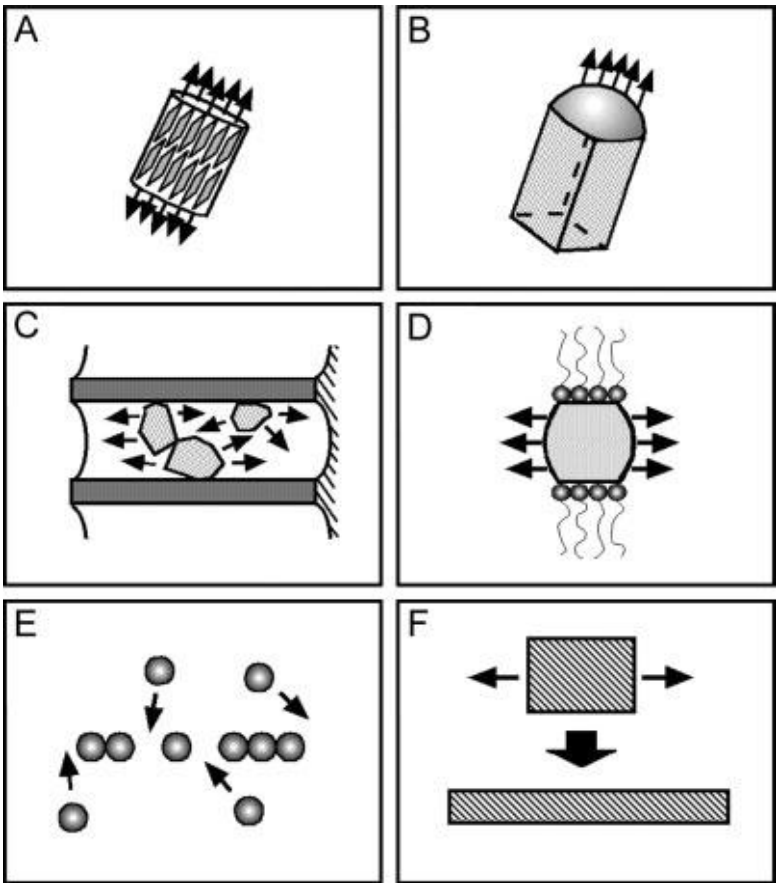

Figure 2.1: Schematic illustrations of six different strategies that have been demonstrated for achieving 1D growth (Xia *et al*, 2003).

2.3 Inorganic nanowires

Since discovery of carbon nanotube by Ijima (Cao, 2004), there has been great attention in the synthesis of 1D structure. Inorganic nanowires can act as active component in devices, as obtained by recent investigations. In the last 4-5 years, nanowires of various inorganic materials have been synthesized and characterized. Rao and his colleagues (2004) in a review have summarized the results drawn from their laboratory work in producing a variety of inorganic nanowires together with the

synthetic work have done. These include nanowires of elements, oxides, nitrides, carbides and chalcogenides.

2.4 Silicon nanowires

Westmaster and co-workers (1995) reported on the fabrication process of silicon nanowires. Silicon nanowires, is a new class of one-dimensional materials and this is ideal systems for investigating the dependence of electrical transport and mechanical properties on dimensionality and the size confinement. Silicon nanowires are expected to play an important role, both as interconnects in the fabrication of nanoscale electric and optoelectronic (Zhang *et al*, 2007; Huang *et al*., 2010).

2.4.1 Structure and properties

Silicon has been the basis element in electronic industry for years because of its band gap, superb natural oxide, outstanding physical properties and its abundant present in nature**.** Silicon is base material used in the manufacture of high purity polycrystalline silicon. These products are used in the manufacture of semiconductors, microchips for computer and solar cells used to capture electrical energy from the sun (Chan & Sze, 2000).

The investigation for suitable device and systems applications of nanostructures is continuing process. Therefore the knowledge about silicon together with existing production lines makes silicon the most special material for many potential applications of nanostructures (Schwartz, M., 2006).

It is known that the electrical and optical properties of the silicon nanowires are strongly related to their size, such as a single silicon nanowire is expected to show quantum confinement effect that in the bulk does not show. The size dependence of the photoluminescence of Si nanowires showed that the band structure of the thin Si nanowires could be changed from the indirect band gap of the bulk solid into the direct band gap (Xing, *et.al*, 2003). Zheng and co-workers (2005) reported that the intrinsic band structure and density of states of nanowires depend directly on the structural design and quality, in particular on the occurrence of growth-related defects. Summary of finding related to SiNWs are listed in Table 2.1.

Table 2.1: Summary of finding related to SiNWs

Authors	**Properties**
Kikkawa *et al*., (2005)	SiNW turns to direct band-gap semiconductor at nanometer size due to quantum confinement, so it could be applied in optoelectronic
Santoni *et al*., (2005)	SiNWs have the advantages of an easy integration in existing Si technology together with the reproducible of the control electronic properties.
Ni *et al*., (2007)	SiNWs offered interesting electrical and thermal properties in dimensionally confined system.
Xiong *et al*., (2008)	SiNWs have outstanding physical properties and potential application in many fields such as optoelectronic, chemical and biology sensor. Example: diameter less than 4nm show the quantum confinement effect which is on carriers would push the photoluminescence (PL) peak into visible range - useful in optoelectronic integration device.
Li *et al*., (2008)	the electrical and optical properties of the Si nanowires are strongly related to their size.

2.4.2 Potential application

Since silicon nanowires posses unique, beneficial physical properties they are expected to be integrated in electronic devices for wide variety of applications. These applications include; single electron transistors (SETs), resonant tunneling diodes (RTDs) and as biological sensor.

The applications of silicon nanowires generated devices are based on the field effect of mechanism manifested by field-effect transistors (FET). In microelectronic industry, FET is used in a circuit to amplify electrical signals as in Hi-Fi amplifier or to function as switching devices in computer for the processing and storage of information. In conventional FET for example metal oxide semiconductor field-effect transistor (MOFSET), the two conducting electrodes called the source and drain are connected by channel made of semiconducting material. The gate electrode is placed on top of an insulating layer. When the gate source voltage is zero, there are no free electrons in the channel and the transistor is in off state. Applying a voltage to the gate electrode results in accumulation of electrons just beneath the insulating layer thus made the channel conducting. When the sizes of field-effect transistors FETs are smaller, the quantum properties of electrons and atoms become significant and an improvement in the atomic structure of the fabricated devices must accompany the size reduction process. Instead of field-effect mechanism, the single electron transistor (SETs) or resonant tunneling transistors (RTTs) a new type of switching device that use controlled electron tunneling to amplify current (Devorett, 2000).

So far many possible applications of nanowires in the semiconductor industry have been proposed but a promising industry scale processing of nanowires is far from reality. Semiconductor nanowires have promising applications in nanoelectronics, nanophotonic devices and integrated nanosystems (Chang *et al*, 2004, Park *et al.*, 2005, Verheijen *et al.*, 2006). In Table 2.2 listed the example of applications of SiNWs.

Table 2.2 : Example of the application of SiNWs

Authors	**Applications**
Deverot and Robert, (2000)	Single-electron transistor.
Cui *et al*., (2003)	Fabricated SiNWs as Field effect transistors
Elibol *et al*., (2003)	Fabricated SiNWs as integrated sensors
Huang *et al.*, (2006)	Fabricated field effect phototransistor of SiNWs where was used as sensing layer
Li *et al*., (2007)	Fabricated SiNWs non-volatile memory devices based on CVD grown nanowires and self alignment technique
Servati *et al*., (2007)	Fabricated scalable and addressable SiNWs as photodiodes
Gunawan and Guha (2008)	Fabricated and characterized SiNWs as solar cell that form core-shell radial p-n junction structures
Argawal *et al*., (2008)	Demonstrated and fabricated SiNWs as a temperature sensor for localized temperature measurement in bio-chemical reaction.

2.5 Method of synthesizing SiNWs

The methods employed to produce silicon nanowires are numerous with each method having advantages and disadvantages depending on the desired properties or

application. Though for the means integration in functional device, these various methods are normally classified to either the two approaches. First the top-down approach in which SiNWs are patterned in bulk materials by subtractive technique for example lithography and etching. Despite the success of this strategy in electronic industry during the past few decades, it soon will face the limitation in creating very small features because this approach depends on the tools. The second approach is called the bottom-up which refers to build-up material from the bottom atom-by-atom, molecule-by-molecule and cluster-by-cluster. In this approach, every single atom or molecules are self assembled precisely when it is needed.

2.5.1 Chemical Vapor Deposition (CVD)

CVD technique has been used by some researcher in formation of silicon nanowires. Normally it was employed for deposition thin film on silicon wafer in semiconductor industry. However in this technique, the desired deposited product was achieved by exposure of the substrate to volatile precursors which react and decompose on the substrate surface. The gas flow is essential to remove the volatile by products produced upon the reaction. The use of modified substrate surface for example metal-coated surface or masked-surface is among the additional step taken in fabricating silicon nanowires. Figure 2.2 show the diagrammatic sketch of the CVD system.

Niu and co-workers (2004) reported that a large-scale, tiny and long silicon nanowires has been synthesized using the simple approach of CVD method at 630^{o}C. Silicon nanowires were generated on p-type (111) silicon wafer, with resistivity about 0.001Ω, and silicon wafer were covered with gold thin film (100nm to 200nm)

using magnetic sputtering technique. List of researchers who did on the researches on fabrication of silicon nanowires via CVD are stated in Table 2.3.

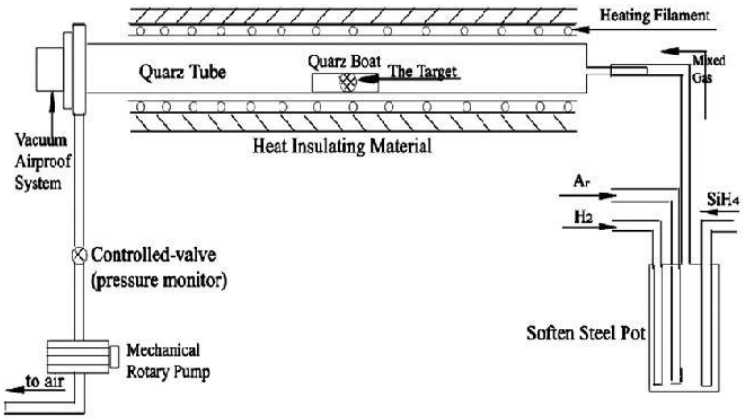

Figure 2.2: Schematic of CVD system (Niu *et al*, 2008).

Table 2.3: The authors working on SiNWs through CVD technique.

Authors, Year	**Method of fabrication**	**Result**
Yu *et al*., 2001	CVD- VLS mechanism	uniform, 1µm in length, 25 nm in diameter
Sharma *et al*., 2004	CVD- VLS mechanism	40–80 nm in diameter at the base, tapering to less than 10 nm at the tip over 1–3 mm in length.
Chen *et al*., 2005	CVD-VLS mechanism	SiNWs; 50-70 nm in diameter, several microns in length
Kwak *et al*., 2006	CVD-VLS mechanism	SiNWs; 30-100 nm in diameter, 0.4-12µm in length
Zhang *et al*., 2006	CVD- VLS mechanism	long and well-aligned silicon oxide nanowires

2.5.2 Laser ablation

Among the various techniques developed to synthesize nanowires which long, uniform-sized, of particular attentions is the laser ablation of metal-containing solid targets or related techniques, by which bulk quantity nanowires can be readily

gained directly from solid source materials (Chen, 2002; Wang *et al*., 2008). Laser ablation has been combined with the VLS method synthesize semiconductor nanowires. In this process, laser ablation is employed to prepare catalyst cluster in nanometer size that define the size of the Si/Ge nanowires produce by the VLS growth (Rao *et al*, 2003).

Morales (1997) were among the first to introduce laser ablation technique in the producing silicon nanowires. In this technique, a laser beam is directed to the solid target of material. It would produce interaction between the laser beam and the target then the formation of silicon nanowires occurs. This process allows the in-situ growth of nanostructures with moderately clean surface because multiple targets can be loaded inside the chamber on a rotating holder. It can be applied to expose sequentially different target to the laser beam. However, the requirement for special apparatus and the use of laser increase the cost of technique. Figure 2.3 show the schematic of the experimental setup for synthesizing silicon nanowires by laser ablation technique.

Hu *et al*., (1999) reported SiNWs with uniform diameters about 10 nm with length >1μm obtained using laser ablation approach of Si-Fe target at temperature $\geq$ 1200^{o}C. In this process, laser ablation of Si-Fe target produces a vapor of Si and Fe that rapidly condenses into Si-rich liquid Fe-Si nanoclusters become supersaturated in Si, the coexisting pure Si phase precipates and crystallizes as nanowires. Figure 2.4 show the mechanism involves in producing silicon nanowires by laser ablation.

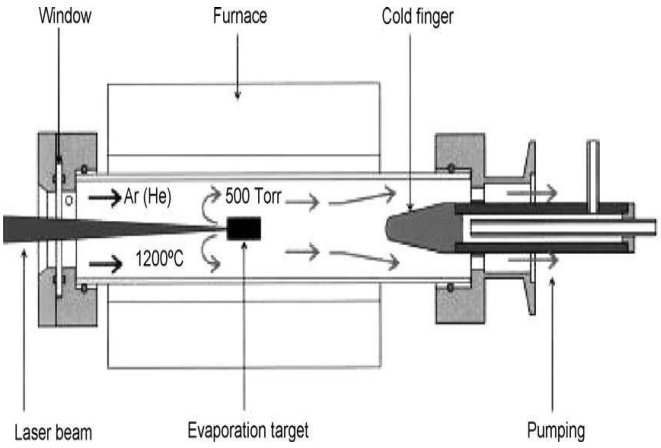

Figure 2.3: Experimental setup for synthesizing silicon nanowires by laser ablation (Wang *et al*, 2008).

Apart from the investigation, Hu *et al*., (1999), also addressed the critical catalyst, Si: catalyst composition and the temperature for nanowires growth can be determined by examining the Si-rich region of binary metal-Si phase diagrams. For example Fe-Si phase diagram (Figure 2.5).

Furthermore, Lee and group (2000) had demonstrated the typical experiment by using an excimer laser to ablate the target in evacuate quartz tube fill with Ar gas. The temperature around targets was in the range between 1200-1400^{O}C. As a result SiNWs which more extremely long and highly curved with a typical diameter of ~20 nm was obtained as shown in Figure 2.6. The authors also reported that nanoparticles of metal or metal silicate in large quantity are rather easy to obtain from the high temperature laser ablation method using metal-containing Si target compared to the classical VLS method.

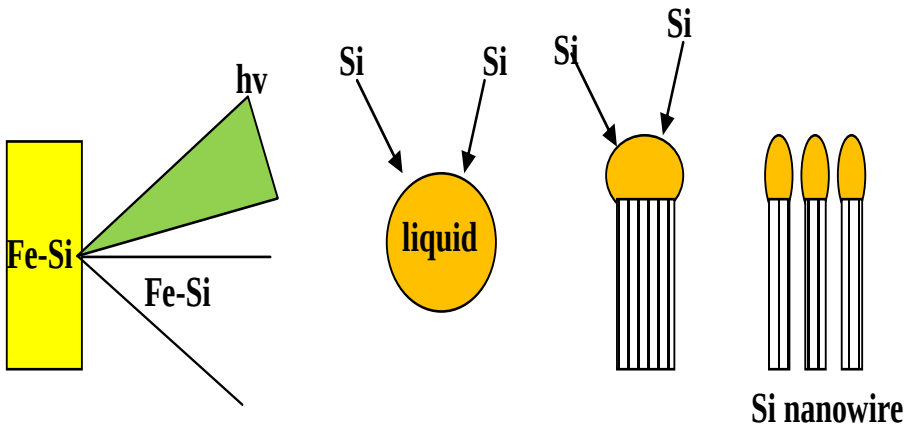

Figure 2.4: Nanowire growth process by laser ablation (Hu *et al*, 1999).

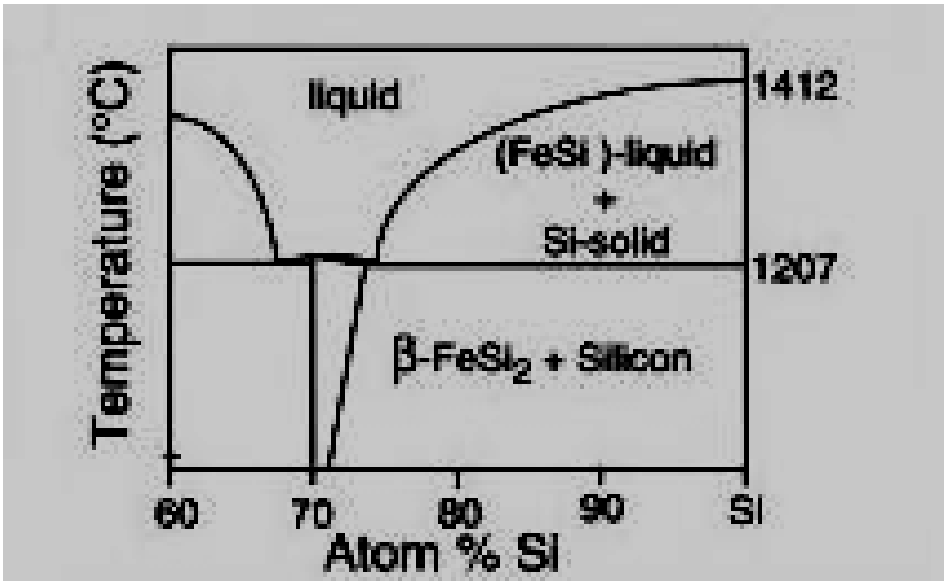

Figure 2.5: Silicon-rich region of the Fe-Si binary phase diagram (Hu *et al.*, 1999).

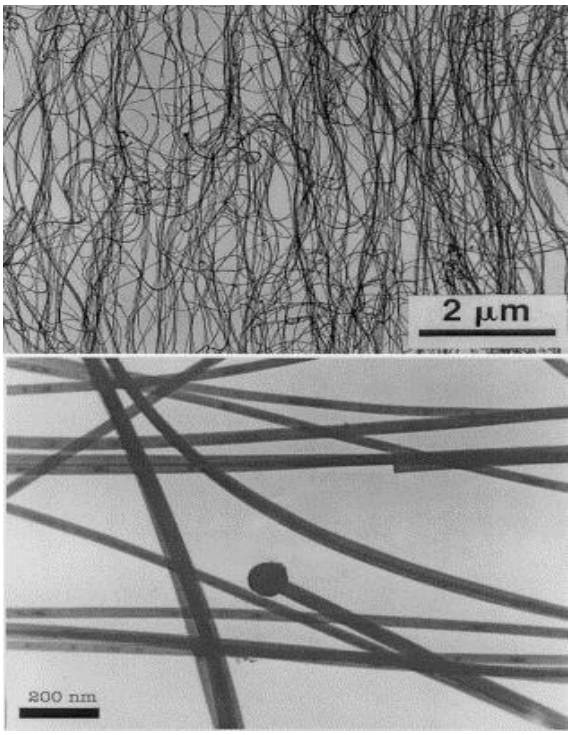

Figure 2.6: TEM micrograph of Silicon nanowires (Lee *et al*., 2000).

The silicon nanowires with different diameters and morphologies were synthesized by laser ablation of a target containing metals over a temperature range 910-1120^{o}C. The octopus-shaped wires of larger diameters were formed in lower temperature zone (910-960^{o}C), while silicon nanowires and silicon nanoparticle chains of smaller diameters in higher temperature zone (960-1120^{o}C), as shown in Figure 2.7. The study shows that the morphology and diameter of silicon nanowires synthesized by laser ablation is not only determined by the growth temperature of silicon nanowires, but also the nature of a catalyst. By change of nucleation temperature and critical nucleus size of nucleus droplets in vapor–liquid–solid (VLS) growth process, a catalyst can change relationships between the morphology, diameter, and growth temperature of silicon nanowires (Chen, *et.al,* 2002).