INVESTIGATION OF METAL ORGANIC DEPOSITION DERIVED CERIUM OXIDE THIN FILMS ON SILICON WAFER

by

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In The Name of Allah, The Most Merciful The Most Compassionate

Peace and Blessings be Upon His Beloved Prophet Muhammad

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LIST OF ABREVIATIONS

AFM	:	Atomic force microscope
c-Ce_2O_3	:	Cubic cerium oxide
CaF_2	:	Calcium fluorite
Ce	:	Cerium
CeO_2	:	Cerium oxide
$Ce_2Si_2O_7$	:	Cerium silicate
CSD	:	Chemical solution deposition
C-V	:	Capacitance-voltage
EDX	:	Energy dispersive X-ray
FESEM	:	Field emission scanning electron microscope
h-Ce_2O_3	:	Hexagonal cerium oxide
IC	:	Integrated circuits
ICDD	:	International Conference for Diffraction Data
I-V	:	Current-voltage
MBE	:	Molecular beam epitaxy
MOD	:	Metal organic decomposition
MOS	:	Metal-oxide-semiconductor
MOSFET	:	Metal-oxide-semiconductor field-effect transistor
PLD	:	Pulse laser deposition
RMS	:	Root-mean-square
Si	:	Silicon
SiO_2	:	Silicon dioxide
SiO_x	:	Silicon oxide
SPA	:	Semiconductor parameter analyzer
TZDB	:	Time zero dielectric breakdown
XRD	:	X-ray diffraction

LIST OF SYMBOLS

A	:	Area (cm^2)
C	:	Capacitance (pF)
C_{ox}	:	Oxide capacitance (pF)
D	:	Crystallite size (nm)
D_{it}	:	Interface trap density (cm^{-2} eV^{-1})
D_{ot}	:	Total interface trap density (cm^{-2})
E	:	Electric field (MV/cm)
E_B	:	Oxide breakdown field (MV/cm)
E_{it}	:	Potential energy
I	:	Current (A)
J	:	Current density (A/cm^2)
k	:	Dielectric constant
q	:	Electron charge (Coulomb)
T_{hkl}	:	Coefficient of texture
t_{ox}	:	Thickness of the oxide (nm)
Q_{eff}	:	Effective oxide charge (cm^{-2})
V	:	Voltage
ΔV_{FB}	:	Flatband voltage (V)
ΔV_{it}	:	Difference between ideal and forward voltage (V)
Å	:	Angstrom
β	:	Corrected full width half maximum (radians)
ε	:	Strain
ε_o	:	Permittivity
θ	:	Diffraction angle (^{o})
λ	:	Wavelength (Å)
δ	:	Dislocation density ($lines/m^2$)

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1. Hock Jin Quah, Kuan Yew Cheong, Zainuriah Hassan, Zainovia Lockman, Farah Anis Jasni and Way Foong Lim. (2010). Effects of postdeposition annealing in argon ambient on metallorganic decomposed CeO_2 gate spin coated on silicon. Journal of The Electrochemical Society, 157 (1), pp. H6-H12.

2. Way Foong Lim, Kuan Yew Cheong, Zainovia Lockman, Farah Anis Jasni and Hock Jin Quah. (2010). Effects of post-deposition annealing on CeO_2 gate prepared by metal-organic decomposition (MOD) method on 4H-SiC. Materials Science Forum, vol. 645-648, pp. 837-840.

3. Farah Anis Jasni, Kuan Yew Cheong, Zainovia Lockman and Zainuriah Hassan. (2009). Metal-oxide-semiconductor (MOS) characteristics of metal-organic decomposed CeO_2 gate spin-coated on silicon. Semiconductor Science and Technology (Institute of Physics Publishing) – submitted.

4. Farah Anis Jasni, Kuan Yew Cheong, Zainovia Lockman and Zainuriah Hassan. (2008). Effects of annealing temperature on cerium oxide thin film deposited on silicon via metal organic decomposition. Malaysian Journal of Microscopy (Electron Microscopy Society of Malaysia), vol. 4, pp. 180-185.

5. Farah Anis Jasni, Kuan Yew Cheong, Zainovia Lockman and Zainuriah Hassan. (2008). Structural and morphological evolution of cerium oxide thin film on silicon prepared by metal-organic decomposition route. Proceedings of 4th International Conference on X-Rays and Related Techniques in Research and Industries 2008 (ICXRI 2008), Universiti Malaysia Sabah, Kota Kinabalu, Malaysia, 2nd – 3rd June 2008.

6. Farah Anis Jasni, Kuan Yew Cheong, Zainovia Lockman and Zainuriah Hassan. (2007). Effects of annealing temperature on cerium oxide thin film deposited on silicon via metal organic decomposition. Proceedings of 6th ASEAN Microscopy Conference, Pahang, Malaysia, 10 – 12 December 2007.

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8. Kuan Yew Cheong and Farah Anis Jasni. (2007). Effects of precursor aging and post-deposition treatment time on photo-assisted sol-gel derived low-dielectric constant SiO_2 thin film on Si. Microelectronics Journal (Elsevier), vol. 38, pp. 227-230.

PENYIASATAN FILEM NIPIS SERIUM OKSIDA DI ATAS WAFER SILIKON MELALUI PROSES PENGENDAPAN LOGAM ORGANIK

ABSTRAK

Filem nipis serium oksida (CeO_2) telah dibentuk di atas substrat silikon (Si) melalui proses penguraian logam organik dalam usaha mengenalpasti keberkesanan oksida ini untuk digunakan sebagai get dielektrik dalam aplikasi logam-oksida-semikonduktor (MOS). Garam serium(III) nitrat dan serium(III) asetilasetonat telah digunakan secara berasingan sebagai bahan pemula dengan penambahan metanol dan asid asetik untuk membentuk larutan berkepekatan malar 0.25 M. Larutan kemudiannya melalui proses pemutaran di atas substrat Si. Proses penyepuhlindapan telah dilakukan pada suhu 400^{o}C hingga 1000^{o}C selama 15 minit di dalam persekitaran gas argon. Selepas itu, sampel terus dikeluarkan dari relau dan disejukkan ke suhu bilik. Analisis kimia melalui sistem pembelauan sinar-X dan spektroskopi Raman menunjukkan bahawa filem CeO_2 telah berjaya dibentuk di atas substrat Si. Struktur dan komposisi fasa filem selepas penyepuhlindapan didapati bergantung sepenuhnya kepada suhu. Morfologi permukaan telah dikenalpasti bergantung kepada garam serium pemula yang digunakan. Filem yang difabrikasi menggunakan serium(III) nitrat menunjukkan keretakan yang nyata manakala filem yang difabrikasi menggunakan serium(III) asetilasetonat mempamerkan kualiti filem yang baik tanpa kecacatan yang nyata. Oksida dengan lapisan epitaksi yang kukuh pada arah orientasi (200) telah diperolehi pada sampel yang disepuhlindap pada suhu 600^{o}C. Arah orientasi didapati berubah dari (200) ke (111) dengan pertambahan suhu sepuhlindap. Nilai pemalar dieletrik dan ketumpatan perangkap permukaan semikonduktor-oksida untuk semua sampel telah dikenalpasti melalui pengukuran kapasitan-voltan frekuensi tinggi dan ia dikaitkan dengan kebocoran arus menembusi lapisan oksida. Oksida yang disepuhlindap pada suhu 600^{o}C didapati mempunyai arus bocor yang paling rendah dengan keboleharapan oksida yang paling baik manakala oksida yang disepuhlindap pada suhu 1000^{o}C mempamerkan keboleharapan yang paling rendah. Oleh itu, dapat dirumuskan bahawa sifat MOS dapat ditingkatkan dengan penggunaan filem oksida CeO_2 berorientasi tinggi.

INVESTIGATION OF METAL ORGANIC DEPOSITION DERIVED CERIUM OXIDE THIN FILMS ON SILICON WAFER

ABSTRACT

Cerium oxide (CeO_2) thin films have been formed on silicon (Si) substrates via metal organic decomposition route in order to resolve the usefulness of this oxide as an alternative gate dielectric for Si-based metal-oxide-semiconductor (MOS) applications. Salts of cerium(III) nitrate and cerium(III) acetylacetonate were independently used as the starting material with the addition of methanol and acetic acid to form a constant concentration of 0.25 M. Solution was spin coated on a Si substrate. Conversion to oxide was done by annealing at temperatures ranging from 400^{o}C to 1000^{o}C for 15 minutes in argon. The samples were quenched to room temperature. Chemical analysis via X-ray diffraction methods and Raman spectroscopy indicated that CeO_2 formed on the substrate after annealing. Structure and phase composition of the films, after heat treatment, were strongly temperature dependent. Surface morphologies were characterized by field emission scanning electron microscope. The morphologies were strongly dependent on the initial cerium salts being used and temperature of annealing. Films fabricated via cerium(III) nitrate showed apparent cracking and peeling. Nevertheless, films formed using cerium(III) acetylacetonate are better quality without obvious defects. An epitaxial-like oxide was obtained on sample annealed at 600^{o}C with a strong preferred orientation along (200) direction. Growth preferential direction was altered from (200) to (111) plane as the annealing temperature increases. Dielectric constant and semiconductor-oxide interface trap density of the samples were extracted from high frequency capacitance-voltage measurements and it was related to the leakage current through the oxides. It has been recorded that the oxide annealed at 600^{o}C has established the lowest leakage current and the best oxide reliability whereby oxide annealed at 1000^{o}C displayed the worst oxide reliability. It was clarified from this work that MOS characteristics are significantly improved by having highly oriented CeO_2 film.

CHAPTER 1

INTRODUCTION

1.1 Background and Problem Statement

Electronic devices have become infused into many facets of our lives, ranging from the use in computers to the use in cellular phones to digital cameras to coffee makers, etc. Life is unimaginable without them. In the early days of electronics, before 1950s, the basic electronic device was the electron tube (which is also known as vacuum tube). Electron tubes made early electronics such as radio, possible but they had some severe limitations. Their filaments tend to burn out just like a light bulb, and it requires a large quantity to make something work. Engineers had tried to investigate ways for better and smaller tubes.

Things began to change in 1950s as engineers turned to a new class of materials called semiconductors. The employment of semiconductor in device fabrication was initiated by physicists John Bardeen and Walter Braittain along with William Shockley in 1947 when they invented the germanium transistor (Kessler, 1997). It was a milestone to semiconductor device fabrication, but germanium was unreliable and engineers sought out new materials to construct transistors. They found an answer in silicon (Si), as it proved to be a better material for making transistors. It was this type of transistor, introduced by Texas Instruments in 1954, that revolutionized the field of microelectronics, the guts of modern electronics.

Ever since then, Si has been the materials of choice in fabricating semiconductor devices. At the beginning of 21st century, the electronics industry is still dominated by silicon and scientists predicted that it is likely to remain so for at least another decade (Intel, 2001).

There are a number of semiconductor devices that employs the unique electrical properties of Si to perform specific electronic functions. Among them are the metal-oxide-semiconductor (MOS) devices that are known to serve as the foundation of the largest industry in the world recently – the electronic industry. In practical applications, the MOS device is the heart of the metal-oxide-semiconductor field-effect transistor (MOSFET) – the most important device for advanced integrated circuits (ICs). The first IC invented in 1958 had just a few transistors, yet the latest microprocessors have over 40 million (Chau, 2004).

Intel cofounder Gordon Moore, was the first to observe this exponential growth in the number of transistors per IC and predicted this trend would continue. In a groundbreaking article written in 1965, he described "Moore's Law," states that the number of transistors on ICs doubles approximately every 24 months, resulting in higher performance at lower cost (Chau, 2004).

To keep Moore's Law rolling forward, transistor geometries scaled to the point where the traditional silicon dioxide (SiO_2) gate dielectric becomes just a few atomic layers thick, tunneling current leakage and the resulting increase in power dissipation and heat become critical issues. Solving these gate dielectric problems is a critical issue for the industry.

Substantial amount of research been carried out to circumvent this dilemma. Alternative gate dielectric has been vigorously sought after as a way to resolve the gate oxide thickness problem. The motivation is to find gate dielectric materials with higher dielectric constant (high-*k*) value than that of SiO_2 (k=3.9) so that it can be made physically thicker while maintaining the same device performance (same gate capacitance per unit area) in order to prevent gate leakage. *k* stands for dielectric constant, a measure of how much charge a material can hold.

There are various studies conducted to find the most suitable high-*k* dielectric to replace SiO_2. Al_2O_3 has many favorable properties, but the drawback is that it has only $k \sim$ 8-10, therefore makes it a relatively short term solution for industry's need. There has also been research conducted on material that has an exceptionally very high-*k* ranging from 80 – 100 such as Ta_2O_5, $SrTiO_3$ and TiO_2, however these materials are thermodynamically unstable on Si. Thus far, it appears that ZrO_2 and HfO_2 with $k \sim$ 23-25 achieve special attention. Nevertheless, due to the well known fast diffusion of oxygen through both oxides, uncontrollable interfacial layer with Si always forms, which is undesirable. Many issues associates with these materials system are yet poorly understood and need further investigation to attain the level of maturity needed for MOS devices.

Researchers begin to look into the use of rare-earth oxides as interesting candidates for gate oxides because according to the thermodynamic calculations they are stable on Si (Hubbard and Schlom, 1996). The other advantages are good general thermal stability, relative high dielectric constants from 28 to 30 and high conduction

band offset with Si. Yet, another attractive feature of rare-earth oxides is the close lattice match with Si.

Owing to these interesting facts, cerium oxide (CeO_2), a rare earth oxide, appears to be promising alternative gate dielectric. CeO_2 has been widely investigated for the use as buffer layer for superconductor but comparatively little research has been done on the application of CeO_2 as gate dielectric on Si.

In the case of CeO_2, most of the early works are contributed to the fabrication of CeO_2 thin film on Si wafer. Some of the methods most commonly used include sputtering (Song *et al*, 2000), laser ablation deposition (Yoshimoto *et al*,1990), metal organic chemical vapor deposition (Ami and Suzuki, 1998), and dual ion beam deposition (Kang *et al*, 1998). However, these vacuum deposition techniques are rather costly and require complex equipments.

Chemical solution deposition via metal organic decomposition (MOD) route appears to be a promising way as it is a scalable non-vacuum technique. It is advantageous over other deposition techniques for its accuracy in composition control and for its simplicity in processing control. Apart from that, thin film produced by MOD demonstrated good stability which is comparable to those prepared by a more typical chemical solution processes like sol-gel method. However until recently, MOD route have only been used in fabricating CeO_2 as buffer layer for various superconductor substrates such as on textured Nickel-alloy substrates for yttrium barium copper oxide (YBCO) superconductor (Steward *et al*,

2005), bi-axially textured Nickel tape (Rousseau *et al*, 2005) and yttria-stabilized zirconia oxide (YSZ)/Hastelloy template (Wang *et al*, 2005).

Fabrication and characterizations of MOD-derived CeO_2 films on Si is not under intensive investigation and thus far to our knowledge, there are only two publications reviewed on the fabrication of CeO_2 via MOD route onto Si substrates. Lee *et al.* (2004) produced CeO_2 thin film as a buffer layer on Si substrate and $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) as a ferroelectric layer in their effort to show that the BLT-based metal-ferroelectric-insulator-semiconductor (MFIS) structure is suitable for memory device application.

Fukuda *et al*. (1998) have also successfully fabricated CeO_2 films via MOD route whereby 3 wt% of MOD solution of Ce-containing alkoxide acid was directly deposited on Si(100) wafers by spin-coating techniques and post deposition annealing was conducted at temperature ranging from 600^oC to 800^oC in oxygen ambient. Nevertheless, it was observed that during crystallization in oxygen ambient, a reaction between CeO_2 and Si occurred at the interface which resulted in the formation of a thin interfacial layer of SiO_2. This interfacial layer is undesirable in gate dielectric application as it could reduce the dielectric constant of the oxide.

Reports related to the annealing in oxygen ambient are very common. However, there is no report on the effects of argon annealing on the MOD-derived CeO_2 films on Si(100) substrate. Therefore, research on the effects of Argon annealing ambient on physical and electrical properties of CeO_2 films have to be systematically carried out and investigated.

1.2 Objectives and Scope of Project

This dissertation is concerned with the implementation of alternative high-*k* gate dielectric to overcome the problem associated with the scaling of MOS devices. The main aim of this research is to determining the usefulness of CeO_2 as gate dielectric for MOS application. To achieve this aim, several objectives are identified, as follows:

1. To form a smooth and good morphology of CeO_2 film on Si via chemical solution deposition through MOD route.
2. To perform substantial investigation on the morphology, phase formed and optical characteristic of CeO_2 film on Si.
3. To discover the effect of heat treatment temperatures in post deposition annealing processes.
4. To conduct a comprehensive analysis on the electrical performance of the CeO_2 film on Si.

In order to achieve the objectives of the dissertation, several tasks have been identified and carried out. In order to achieve smooth and good film morphology, cerium(III) nitrate and cerium(III) acetylacetonate are used as starting precursors to form CeO_2 film via MOD. CeO_2 film is then deposited on Si by spin-on-coating technique. Variation of annealing temperature is employed to each sample with different starting precursors in order to determine its effects during annealing procedure in argon ambient. Substantial testing is carried out using appropriate testing machine to obtain the morphology, phase formed and optical characteristic of CeO_2 film on Si. Evaluation of the electrical performance of CeO_2 film on Si is

carried out from the overall response of the capacitance-voltage (C-V) and current-voltage (I-V) measurement conducted on the samples.

1.3 Dissertation Outline

This dissertation is organized in such a way that it systematically leads to achievement of the research objectives, as follows.

Chapter 1 begins with an introduction to the research work. The motivations of this research are discussed, and the objectives, scope and approach are identified. Chapter 2 provides an extensive review on the field of semiconductor that is related to this research. This chapter will cover the current and past researches that have been conducted worldwide. Chapter 3 explains the experimental procedures employed in this project, details of the laboratory equipment used as well as testing and characterization that are conducted on the samples. Chapter 4 discusses the outcome results of the samples. The detail performance analysis of the samples is converse in this chapter. Chapter 5 contains the concluding remarks and presents the contribution of this research. Some improvement for future study is also suggested.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this modern day, everything is predominantly powered by electronic devices. Electronic devices are everywhere; assemble within your cameras, iPod, computers, coffee makers, cars, cell phone gadgets, etc. Life is unimaginable without them.

Back in the 1940s and 1950s, electronic devices only relegated to just radios and televisions. The first general purpose electronic computer called ENIAC, short for Electronic Numerical Integrator And Computer was developed in 1940s (Hally, 2005). ENIAC was so large that it filled the entire room. It looks more like furniture than like a cutting-edge electronic device. Machine like ENIAC is predecessors to the personal computers or laptops that we have nowadays. People tend to look for small, lightweight, powerful and less expensive computers these days. To fulfill the trend, engineers begin to work on designing better and smaller computers. It is a very hard attempt since computers are extremely complicated technological systems. Inside a computer, there are a whole range of different electronic chips such as memory chips and microprocessors.

A chip is a home for transistor, which is usually used as a switch rather than an amplifier. A whole lot of these transistors are needed to make up a complicated logic circuit that allows computers to function. There are over millions of transistors

inside a typical memory chip. Most of these transistors are often in a form of MOSFET. The basic structure of MOSFET is shown in Figure 2.1.

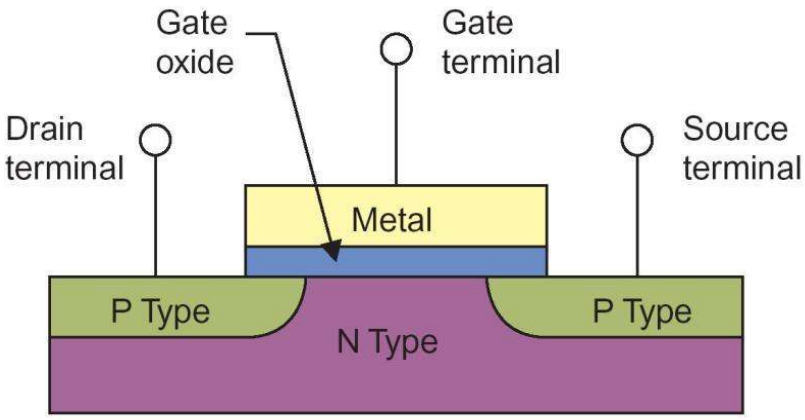

Figure 2.1: Basic MOSFET structure.

Apart from transistors, a chip is also a home for other elements, such as resistors, capacitors and interconnecting conductors. In order to pack so many transistors and circuit elements onto one chip, engineers need to shrink the size of these electronic components.

2.2 Gate Oxide in MOS Devices

In an attempt to shrink electronic components, we must first understand the basic principle of the structure of these components. Most transistors are often based on metal-oxide-semiconductor or MOS structure, a device that was invented by Kahng and Attala (Schroder, 1998). A MOS capacitor is the simplest of a MOS-based devices and it is the structural heart of all MOS devices. MOS capacitor is basically a simple two terminals device composed of a thin layer oxide sandwiched in between a Si substrate and a metallic plate as shown in Figure 2.2.

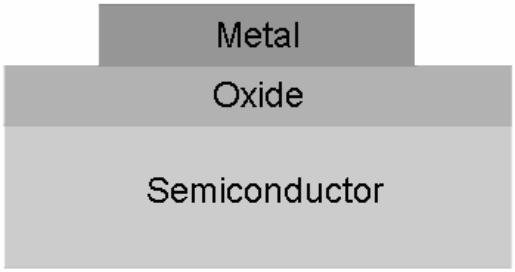

Figure 2.2: A MOS Structure.

The thin oxide layer in a MOS capacitor serves as a gate oxide. In an ideal MOS structure, the oxide is a perfect insulator with zero current flowing through the oxide layer under all static biasing conditions (Schroder, 1998). SiO_2 has been used as a gate oxide in MOS devices for the past three decades. The key advantage of SiO_2 as the gate oxide is due to the outstanding properties of SiO_2, such as high quality Si-SiO_2 interface, thermodynamic and electrical stable as well as superior electrical insulation properties. SiO_2 serves as an almost perfect insulator until a few years back, where researchers encounter a problem with it.

The traditional approach of scaling the gate dielectric in MOS devices has been related to reducing SiO_2 thickness (d) to increase the oxide capacitance (C_{ox}), which is defined as (Robertson, 2004):

$$C_{ox} = k \varepsilon_o A / d \qquad (1.1)$$

where k is the dielectric constant of the oxide (term given to the number relating the ability of a material to carry alternating current to the ability of vacuum to carry alternating current) and ε_o is the permittivity of free space (8.85×10^{-3} F/m).

In their attempt to shrink down or down scaling MOS devices to fulfill the current demand of smaller and smaller devices, researchers realized that the thin layer of SiO_2 is one critical part of MOS devices that could not be shrunk any longer. The insulating layer has been slimmed and shrunk with each new generation until it has becomes a scant five atoms thick (Bohr *et al*, 2007). At five atoms, the SiO_2 layer was so thin that it has begun to lose its insulating properties. This thin layer allows large and exponentially increasing leakage current that arise from the quantum mechanical tunneling of electrons through the SiO_2.

2.2.1 Scaling of the gate oxide

Major semiconductor firms and researchers in university labs are aware of problems related to the down scaling of MOS devices and extensive research programs had been launched to come up with a solution. They have been experimenting on replacing SiO_2 with high-k as compared to SiO_2 (k=3.9) and the need for these high-k oxides has been emphasized in numerous scientific reports.

What will actually happen if the k value increases? And what will happen if the thickness of the oxide increases as well? This can further explained by Figure 2.3 that shows the illustration of the correlation between high-k and oxide thickness.

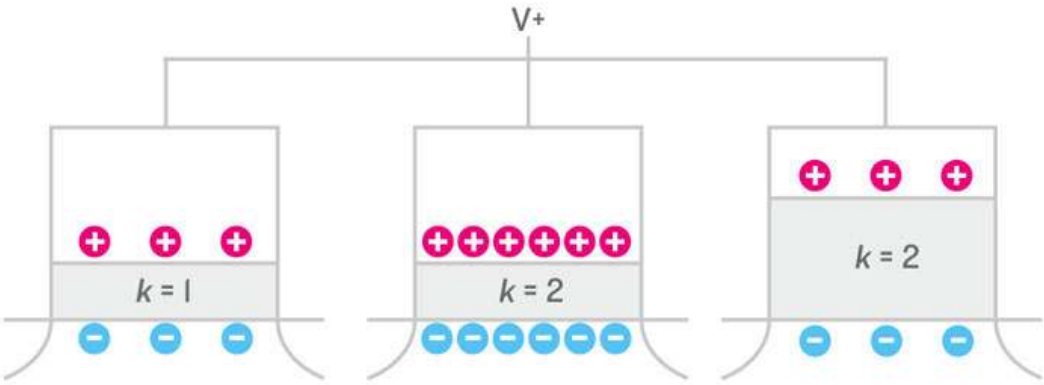

Figure 2.3: The illustration of the correlation between high-*k* and oxide thickness (Bohr *et al*, 2007).

From Figure 2.3, if one gate oxide has twice the dielectric constant of another, a given voltage will draw twice as much charge. It means that high-*k* oxide provide increased capacitance with the same thickness of oxide. However, one can also have the same amount of accumulated charge if the high-*k* oxide is made twice as thicker.

2.2.2 Considerations for high-*k* gate oxide materials

Much work and several approaches have been used in identifying potential high-*k* candidates and to simplify this, Robertson has addressed a few requirements of a new oxide (Robertson, 2004):

1. It must have high enough *k* than SiO_2 (*k*=3.9) for the reason that it will be used for a practical number of years scaling.
2. The oxide is in direct contact with the Si channel (as shown in Figure 2.1), so it must be thermodynamically stable with it, in order to prevent the formation of thick SiO_x interfacial layer and or the formation of silicide layers.

3. It must be kinetically stable, and be compatible with MOS processing up to as high as 1000^{o}C high temperature processing.
4. It must act as an insulator, by having band offsets with Si of over 1 eV to minimize carrier injection into its bands.
5. It must form a good electrical interface with Si, in terms of roughness and the absence of interface defects.
6. It must have low density of electrically active defects at the Si-dielectric interface and in the bulk material, providing high mobility of charge carriers in the channel and sufficient gate dielectric lifetime.

Above requirements are necessary to limits a wide range of oxides into a few potential oxides to be considered as alternative gate dielectric to SiO_2.

2.2.3 Alternative high-*k* gate dielectric

There are numerous potential candidates have been considered as an alternative high-*k* gate dielectric to SiO_2. Han *et al*. (1995) and Pan *et al.* (2000) give an excellent overview of the use of silicon oxynitrides (SiO_xN_y) as gate dielectrics and recently Yeo *et al.* (2000) have successfully prepared silicon nitride MOS devices with promising characteristics. Despite the efforts given to the use of oxynitrides and oxide/nitrate stacks, not much could be gained for the use of these materials as alternative gate dielectric for the reason that their band gap and band offsets with Si are always going to be less as compared to SiO_2 with gaining much on the dielectric constant (pure Si_3N_4 has k~7) (Robertson, 2004).

Alumina (Al_2O_3) has been extensively studied for many applications and several studies have proposed the use of it as an alternative gate dielectric. Al_2O_3 is indeed has many favorable characteristic including a high band gap as compared to Si_3N_4 and it is thermodynamically stable on Si up to high temperatures. Stability on Si is imperative in order to prevent reactions with Si that will eventually leads to formation of thick interfacial SiO_x or silicide layers. Nevertheless, the drawback is that the *k* value of Al_2O_3 is only ~ 8-10, therefore makes it a relatively short term solution for the industry. For a longer term of scaling, the *k* value should be over 10, preferably 25-30.

Many other metal oxides with a very high *k* value have also been proposed. The first step of culling these proposed high *k* metal oxides is that it had to be thermally (up to 1000^{o}C) and chemically stable in contact with Si in view of the fact that high temperature annealing conditions are typically employed in standard MOS processes. It is also considered in most cases, the dominant factor in determining the overall electrical properties (Wilk *et al*, 2001). The most comprehensive study on the thermal stability of oxide with respect to Si at 1000K has been systematically assessed by Hubbard and Schlom (1996). Metal oxides were characterized as thermodynamically stable or unstable in contact with Si. The results of this comprehensive study on the thermodynamic stability of oxides with Si are graphically summarized by the periodic table in Figure 2.4 (Schlom *et al*, 2008).

Most of the binary oxides are thermodynamically unstable on Si at 1000K except for elements from columns II, III, IV and the lanthanides of the Periodic table shown in Figure 2.4. This restrict the possible wide range of alternative gate oxides

to a very few that is stable on Si such as SrO, CaO, BaO, Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3 and the lanthanides. It excludes some otherwise useful and familiar oxide with a very high *k* such as TiO_2 (*k*~80-110), Ta_2O_5 (*k*~22), and the titanates including $SrTiO_3$ (*k*~2000) as well as $BaTiO_3$. Nevertheless, the group II oxides such as SrO and etcetera are not also favoured themselves due to the fact that they were very reactive with water.

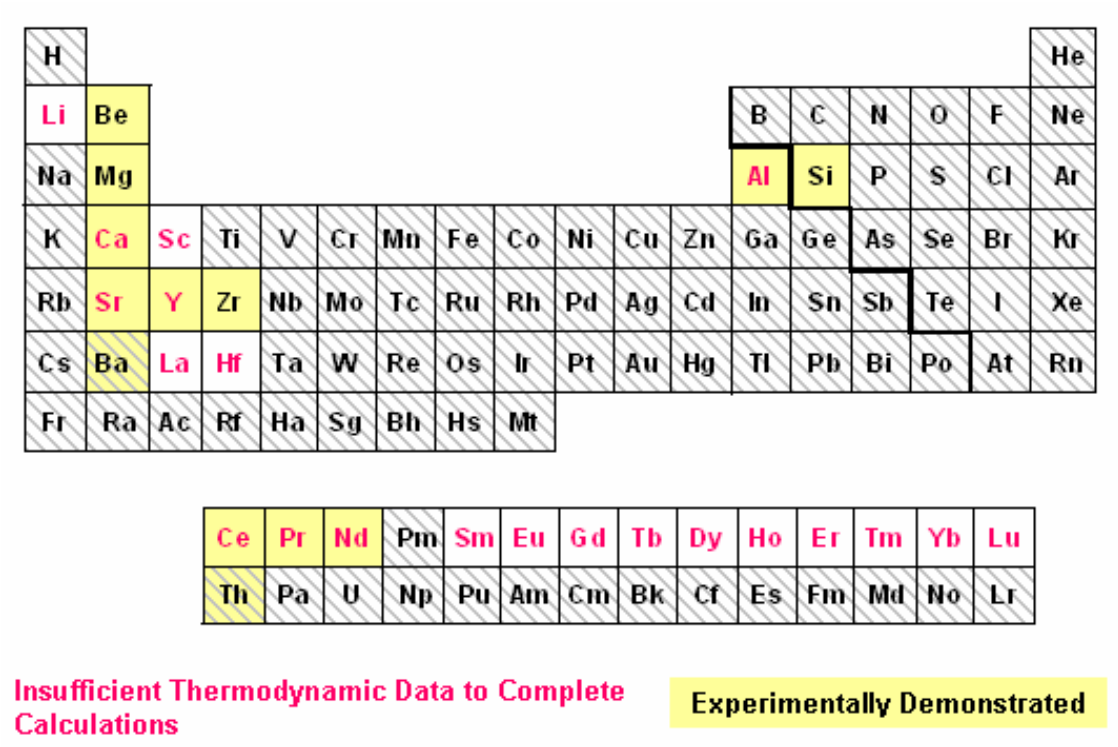

Figure 2.4: Periodic table showing which elements has oxides that might be stable in contact with Si. Elements having no thermodynamically stable or potentially thermodynamically stable oxide are shaded (hatched). Also presented in the periodic table are the elements having an oxide that had been experimentally demonstrated to be stable in direct contact with Si (Schlom *et al*, 2008).

Hence, apart from various lanthanide oxides such as CeO_2, Pr_2O_3 and Nd_2O_3, this leaves only a few possible oxides of ZrO_2, HfO_2, Y_2O_3 and La_2O_3. However, it turns out that thermodynamic data for these certain oxides was not so accurate after all. Ferrari and Scarel (2004) reported that ZrO_2 and HfO_2 fabricated via atomic layer deposition process are revealed to be slightly unstable on Si. It was reported that an interfacial layer always formed through post annealing process due to the well-known fast diffusion of oxygen through ZrO_2 and HfO_2. Oxygen which diffuses through these metal oxides was found to react with Si at the interface to form an uncontrolled interfacial layer. On the other hand, Y_2O_3 and La_2O_3 are reported to be under-constrained with respect to SiO_2, which will eventually leads to the formation of a high density of electrical defects near the Si-dielectric interface, resulting in poor electrical properties (Wilk *et al*, 2001).

Researchers begin to look into the use of lanthanide oxides (rare-earth oxides) as interesting candidates for gate oxides because according to the thermodynamic calculations, most of them are stable on Si (Hubbard and Schlom, 1996). The other advantages are good general thermal stability, relatively high-*k* from 20 to 30 and high conduction band offset with Si. Yet, another attractive feature of some thermodynamically stable phases of rare earth oxides is their closer lattice match with Si compared to ZrO_2 and HfO_2, which is an advantage for epitaxial dielectrics for future applications (Leskela *et al*, 2006).

Among various lanthanide oxides, cerium oxide (CeO_2) attracts particular attention due to its remarkable properties. CeO_2, a rare earth oxide (k ~ 15-26) with a cubic fluorite structure, appears to be a promising alternative gate dielectric to SiO_2 (Inoue *et al*, 1990). Besides, a small lattice mismatch between Si (Δd = -0.35%), an energy band gap of ~5.5 eV, as well as its excellent thermal stability at high temperature have promoted this oxide to be considered as a potential gate dielectric on Si (Nishikawa *et al*, 2002).

Thus far, CeO_2 has been widely investigated for the use as a buffer layer for superconductor applications but comparatively little research has been done on this type of oxide as gate dielectric on Si. Combined with its favorable properties, it is clear that there should be significant experimental effort put forth in determining the usefulness of applying CeO_2 to Si-based electronics.

2.3 Cerium Oxide (CeO_2)

2.3.1 Introduction

Cerium oxide, also known as ceric oxide, ceria, cerium (IV) oxide or cerium dioxide is an oxide of the rare earth metal cerium (Ce). Ce is known to be the most abundant member of the lanthanides series of elements in Periodic table (Barry, 1992). Ce oxide has three phases namely CeO_2 with the calcium fluorite (CaF_2) structure, and hexagonal (h-) and cubic (c-) Ce_2O_3 respectively (Yamamoto *et al*, 2005). The crystal structures of the three phases of Ce oxide are shown in Figure 2.5.

Pure stoichiometric CeO_2 exhibit the CaF_2 type of structure with space group Fm3m over the whole temperature range from room temperature to the melting point. It has 8-coordinate cations and 4-coordinate anions. CeO_2 is known for its primary role in oxygen storage, whereby it could release oxygen under reduction conditions forming a series of reduced oxides with stoichiometric Ce_2O_3 as an end product, which in turn easily takes up oxygen under oxidizing conditions, turning the Ce_2O_3 back to CeO_2. In other words, during oxygen poor conditions, Ce_2O_3 with oxygen vacancy is formed. In Ce_2O_3, 4 f states of Ce are reduced, and the valence is changed from +4 to +3 (Skorodumova *et al*, 2001). Note that Ce formally has the valence +4 in CeO_2, the most oxidized form of Ce, and the valence +3 in Ce_2O_3. At room temperature, the hexagonal Ce_2O_3 crystal is unstable in air, but stable under anaerobic condition. The cubic Ce_2O_3 crystal, which can be considered as the CeO_2 crystal with ordered oxygen vacancies, is known to exist at a non-stoichiometric state in the temperature range of 1000°C–1200°C in hydrogen atmosphere (Yamamoto *et al*, 2005).

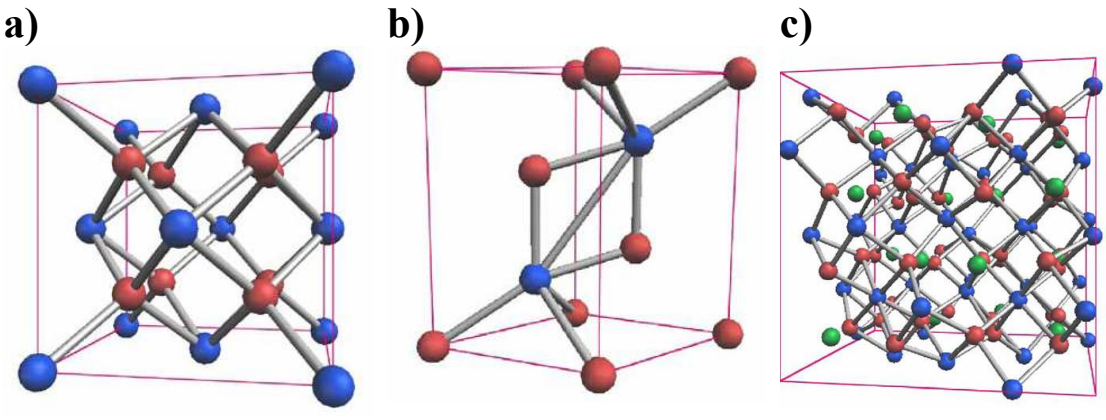

Figure 2.5: Crystal structures of (a) CeO_2, (b) h-Ce_2O_3 and (c) c-Ce_2O_3. Ce, O atoms, and O vacancies are indicated as blue, red, and green spheres, respectively (Yamamoto *et al*, 2005).

2.3.2 Properties of CeO_2

The basic chemical and physical properties of CeO_2 had been recapitulated in Table 2.1.

Table 2.1: The basic chemical and physical properties of CeO_2 (Barry, 1992)

PROPERTIES	UNITS
Systematic name	Cerium (IV) oxide
Other names	ceric oxide, ceria, cerium oxide, cerium dioxide
Molecular formula	CeO_2
Chemical abs. no.	1306-38-3
Molar mass	172.115 g/mol
Melting Point	~2750 K
Density	7.28 gcm^{-3}
Specific Heat	~460 $Jkg^{-1}K^{-1}$
Thermal Conductivity	~12 $Wm^{-1}K^{-1}$
Thermal Expansion	~11 x 10^{-6} K^{-1}
Refractive Index	~2.1 (visible) ~2.2 (infra-red)
Young's Modulus	~165 x 10^{9} Nm^{-2}
Poisson's ratio	~0.3
Hardness	~5 – 6 mhos

Aside from the basic chemical and physical properties mentioned in the Table 2.1, there are many other significant properties of CeO_2 which could be exploits in order for it to be acknowledged as strong substitute for SiO_2 as gate dielectric in MOS technology. Exhibit a high dielectric constant (k ~ 15-26), small lattice mismatch between Si (Δd = -0.35%), energy band gap of ~5.5 eV, as well as its excellent thermal stability at high temperature have promoted this oxide to be considered as a potential gate dielectric on Si (Nishikawa *et al*, 2002).

In addition, CeO_2 is preferred as regards to process simplicity compared to other conventional high-*k* candidates, such as TiO_2 and Ta_2O_3, which require an extra barrier layer to prevent inter diffusion with the substrate. To further evaluate the electrical properties of CeO_2 in order for it to be considered as alternative high-*k* candidates, Table 2.2 is used to presents the properties of CeO_2 as compared to the conventional SiO_2 used at present.

Table 2.2: Materials properties of CeO_2 as compared to SiO_2 (Preisler, 2003)

PROPERTIES	**SiO_2**	**CeO_2**
Structure	Amorphous	Cubic
Crystallization temperature (^oC)	NA	≥600
Crystalline growth	No	Yes
Density (g/cm^3)	2.2	7.28
Melting point (^oC)	~1600	2400
Lattice parameter (Å)	NA	5.411
Refractive index	1.46	~2.1 (visible) ~2.2 (infrared)
Dielectric constant (*k*)	3.9	15-26
Band gap (eV)	9	5.5
Interface trap density (eV^{-1} cm^{-2})	$\leq 1\times10^{10}$	2×10^{11}

All in all, the CeO_2 have properties that may possibly be advantageous for it to be considered as an alternative to SiO_2. Thus, it also has been studied far less in terms of its use as a gate dielectric and a lot more research is needed to make the final evaluation from its possibilities as gate oxide.

2.4 Fabrication Technique of CeO_2 Films via Chemical Solution Deposition

The deposition method of choice has a large impact on the properties of the high- *k* layers. A wide range of deposition method has been presented in literature for high-*k* dielectrics. Each deposition method has its own unique merits and demerits that affect the microstructural and electrical properties of layers, for example typical deposition temperatures, the chemistry involved, layer uniformity and reproducibility.

In the case of CeO_2, most of the early works are contributed to the fabrication of CeO_2 thin film on Si wafer. Up to date, all of the thin film deposition techniques being reported were purely concentrated on methods such as molecular beam epitaxy (MBE) (Yoshimoto *et al*, 1995), pulsed laser deposition (PLD) (Hirschauer *et al*, 1999) (Wang *et al*, 1999), electron beam evaporation (Djanovski *et al*, 2006), RF magnetron sputtering (Kim *et al*, 2000) and dual ion beam reactive sputtering (Kang *et al*, 1998).

However, it is well acknowledged that vacuum deposition techniques are rather costly and require complex equipments. Therefore, non-vacuum and scalable technique such as chemical solution deposition route appears to be a promising technique over others. The details of the chemical solution deposition process will be discussed in the following sub-section.

2.4.1 Overview of the Chemical Solution Deposition (CSD) Process

A range of requirements must be fulfilled by the solution chemistry, substrates, and processing conditions for successful implementation of the CSD technique (Schwartz *et al*, 2004). These include:

- solubility of the precursors must be adequate in order to form a stable coating solution;
- decomposition and may be pyrolization process during synthesis of precursors must not leave out any undesirable residues during thermal treatment;
- there is no macroscopic phase separation of precursor components during drying or pyrolysis, for example crystallization of the individual components upon solvent evaporation should be avoided and homogeneity at an 'atomic' level should be preserved;
- tolerable wetting of the substrate;
- the deposition approach as well as the deposition parameters employed must be satisfactorily adjusted to the solution rheology to avoid thickness variations;
- there is no crack formation or compositional non uniformities during pyrolysis or crystallization process;
- minimum interdiffusion of film and substrate constituents;
- minimal degradation of substrate properties during film processing;
- acceptably sufficient long-term stability of the solution to avoid non-reproducible film properties that are dependent on solution aging.

CSD technique could be a successful rapid and cost-effective method for synthesizing high-quality electronic oxide thin films if all of the requirements mentioned above are fulfilled and the fabrication conditions are optimized. Schwartz *et al*. (2004) in its review describe that various CSD routes utilized for electronic oxide film fabrication can be divided into three principal categories, which are:

1) **Sol-gel processes**: This classical process utilized the use of metal alkoxide (metal ion bonded to the oxygen) in organic solvents. The key reactions leading to the formation of the precursor species are primarily the hydrolysis and condensation process, in which metal–oxygen–metal (M–O–M) bonds are formed and R represent alkyl group:

   - *hydrolysis*

     $$M(OR)_x + H_2O \rightarrow M(OR)_{x-1}(OH) + ROH \quad (2.1)$$

   - *condensation (alcohol elimination)*

     $$2\ M(OR)_{x-1}(OH) \rightarrow M_2O(OR)_{2x-3}(OH) + ROH \quad (2.2)$$

   - *condensation (water elimination)*

     $$2\ M(OR)_{x-1}(OH) \rightarrow M_2O(OR)_{2x-2}(OH) + H_2O \quad (2.3)$$

   It has also been demonstrated that through manipulation of the above reactions, for instance by controlling the reflux, catalysis, and hydrolysis conditions, the nature of the resulting solution precursors and gels may be controlled, allowing better control of material properties. Nevertheless, the drawback of this process is that the uses of metal alkoxide are usually sensitive to the atmosphere humidity.

2) **Metal organic decomposition (MOD) routes**: This process fundamentally utilized carboxylate precursors that do not undergo significant condensation reactions during either solution preparation or film deposition.

A carboxylate anion, RCO_2^-, is an ion with negative charge that contains the group $-COO^-$. It is the conjugate base of a carboxylic acid as shown in Figure 2.6 (Fox and Whitesell, 1997).

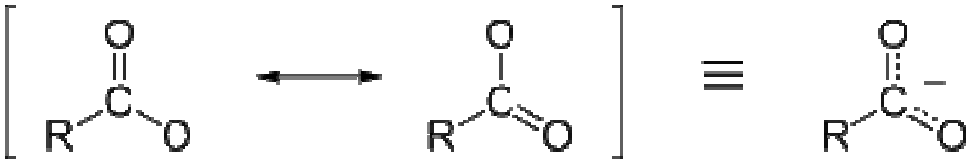

Figure 2.6: Examples of the conjugate base of a carboxylic acid. The R represents alkyl groups (Fox and Whitesell, 1997).

The basic approach consists of simply dissolving the metal-organic compounds in a common solvent and combining the solutions to yield the desired stoichiometry. For solution preparation, researchers in labs have used commercially available as well as in-house synthesized precursors.

Despite the fact that the MOD process is straightforward, it possessed a number of limitations, whereby the major problem is related to the used of the large organic ligands that may cause cracking during thin film processing due to the excessive weight loss and shrinkage that can occur. Nevertheless, Schwartz *et al.* (2004) reported that Haertling has developed an alternative MOD strategy that minimizes this problem. Low reactivity starting reagents