A STUDY ON PROCESS-GENERATED CRYSTAL DEFECTS AND CORRESPONDING LEAKAGE CURRENT OF P-N JUNCTIONS IN BIPOLAR TRANSISTORS

by

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C.Y. Cheah

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

BJT	Bipolar junction transistor
COP	Crystal-originated pit
CZ	Czochralski
EDX	Energy dispersive X-ray
FZ	Float zone
HR-TEM	High resolution transmission electron microscopy
LSL	Lower specification limit
MOSFET	Metal-oxide-semiconductor field effect transistor
PEM	Photoemission microscopy
RCA	Radio Corporation of America
SEM	Scanning electron microscopy
TED	Transient enhanced diffusion
USL	Upper specification limit
XRT	X-ray topography

LIST OF SYMBOLS

A	Cross-sectional area of diode
D_N	Electron diffusivity constant
D_p	Hole diffusivity constant
E_C	Conduction band energy level
E_F	Fermi energy level
E_i	Intrinsic energy level
E_t	Intermediate energy level of recombination center
E_V	Valence band energy level
e_s	Semiconductor permittivity constant
f	Failure density
F	Unreliability
G_L	Photogeneration current
I	Current
I	Reverse current
I_R	Reverse saturation current
J	Current density
J_N	Diffusion current density of electrons
$J_{n,drift}$	Drift current density of electrons
J_P	Diffusion current density of holes
$J_{p,drift}$	Drift current density of holes
k	Boltzmann constant
L_N	Diffusion length of electrons

L_p	Diffusion length of holes
l	Failure rate
m	Mass of carrier
m_n	Electron mobility
m_p	Hole mobility
n	Diode ideality factor
n	Concentration of free electrons
n	Total sampling population
n_i	Intrinsic carrier concentration
N_A	Number of acceptor carriers
N_D	Number of donor carriers
N_t	Number of recombination centers
n_i	Intrinsic charge concentration
n_p	Electron concentration
u_{dp}	Average drift velocity of holes
n_{th}	Thermal velocity of carrier
p	Concentration of free holes
p_n	Hole concentration
q	Electronic charge
r	Number of failed items
R	Reliability
R_s	Sheet resistance
Si_i	Silicon self-interstitial

Si_v	Vacancy in the silicon lattice
s	Proportionality constant
t	Time
T	Temperature
t_n	Mean carrier recombination lifetime
U	Rate of generation-recombination
V	Voltage
V_{BD}	Breakdown voltage
V_{bi}	Built-in potential
W	Width of depletion region
x	Space in x-direction

SUATU KAJIAN MENGENAI KECACATAN HABLUR HASIL PEMPROSESAN DAN ARUS BOCOR YANG SEPADAN BAGI PERSIMPANGAN P-N DALAM TRANSISTOR DWIKUTUB

ABSTRAK

Suatu kajian mengenai arus bocor songsang lebihan struktur kawalan proses simpang *p-n* dalam teknologi transistor dwikutub industri diperincikan dalam kerja ini. Kebocoran lebihan disebabkan oleh kecacatan hablur seakan-akan batang hasil daripada proses implantasi boron. Kecacatan hablur dicadangkan terdiri daripada celahan diri dalam kekisi silikon. Kecacatan tersebut dikurangkan dengan menambahbaik penumbuhan oksida penyerak sebelum implantasi. Model-model kejadian yang menerangkan bagaimana celahan diri dikurangkan melalui penambahbaikan proses kemudian dicadangkan. Pengoksidaan dijalankan dalam persekitaran kering dan menjangkaui suhu alir likat untuk memulihkan tegasan antaramuka semasa penumbuhan oksida. Penyuntikan celahan ke dalam silikon dicadangkan tidak berlaku. Pada ketebalan optimum oksida penyerak, ion-ion boron tuju dicegah daripada membentuk celahan dalam kekisi silikon. Ketebalan optimum bagi oksida iaitu ~ 62 nm daripada eksperimen bersetuju dengan keputusan simulasi. Selain itu, suatu proses sepuh lindap suhu tinggi dijalankan selepas pengoksidaan untuk mencairkan kumpulan celahan yang hadir di dalam kekisi. Sebagai keputusan sampingan, persekitaran berklorin disahkan dapat mengurangkan kecacatan hablur. Dicadangkan bahawa atom-atom klorin mencipta kekosongan pada permukaan silikon yang mengeluarkan celahan daripada permukaan silikon. Peningkatan 13 hingga 15 % dalam hasilan elektrik dilaporkan daripada penambahbaikan proses tanpa memudarat ciri-ciri elektrik dan fizikal teknologi dwikutub.

A STUDY ON PROCESS-GENERATED CRYSTAL DEFECTS AND CORRESPONDING LEAKAGE CURRENT OF P-N JUNCTIONS IN BIPOLAR TRANSISTORS

ABSTRACT

An investigation into excess reverse leakage current of *p-n* junction process control structures in an industrial bipolar junction transistor technology is detailed in this work. Excess leakage is shown to be caused by rod-like crystal defects generated from a boron implantation process. The rod-like defects are suggested to consist of self-interstitials in the silicon lattice. The defects were reduced by optimizing the scattering oxide growth prior to implantation. Phenomenological models are then proposed to explain how self-interstitials were reduced by process optimization. Oxidation was performed in dry ambient and above the viscous flow temperature to relieve the interfacial stress during oxide growth. It is suggested that by doing so, interstitial injection into silicon is eliminated. At an optimum thickness of scattering oxide, incident boron ions are suggested to be prevented from creating interstitials in the silicon lattice. The optimum oxide thickness value of ~ 62 nm from experiment is in agreement with the simulation results. In addition, a high temperature annealing process is performed after the oxidation to dissolve away any existing interstitial clusters in the lattice. As a side result in this thesis, a chlorinated ambient has been confirmed to reduce crystal defects. It is suggested that the chlorine atoms create vacancies on the silicon surface which eliminate interstitials from the silicon surface. A 13 to 15 % improvement in electrical yield has been shown from the process optimization, without any adverse effects on the electrical and physical properties of the bipolar technology.

CHAPTER 1

INTRODUCTION

Wafer processing during device fabrication introduces a host of crystal defects. These defects can degrade the electrical properties of various semiconductor devices. As such, defects should be minimized to maintain the quality and reliability of the device. In line with industrial requirements for Zero Defects, processing-defect reduction is a continuous effort in the semiconductor industry. Zero Defects is especially critical for bipolar devices produced for use in the automotive sector, such as the ones under study in this work.

This project investigates a topic in a mass-produced industrial product, namely the silicon bipolar junction transistor (BJT) technology. The topic of interest is electrical failures in the form of excess reverse leakage current in *p*-*n* junction process control structures of the BJT technology. Excess reverse leakage is commonly associated with the presence of crystal defects generating during a fabrication process. Such defects might compromise the quality and reliability of the BJTs, and justifies pursuant of this study.

A device which flows excessive current increases the power dissipated from an electronic circuit. In the worst case, the circuit would overheat due to excessive power dissipation and lead to equipment failure. It is for this reason that sparked the recent massive vehicle recall by Ford Motor Company (Krisher & Manning, 2009). At the start of this study, the severity of electrical failure is gauged from an analysis of six month data of reverse current testing, Fig. 1.1. The data are obtained from Infineon Technologies with a sample size of 14,648 data points. We refer the reader to Appendix

A.1 for an introduction to cumulative probability curves. It is seen from the figure that the cumulative probability of data points with reverse current magnitudes below the upper specification limit (USL) is 82 %. This value is the “baseline yield” of the tested structures.

1.1 Scope and objectives of study

This study would examine various processes involved in BJT fabrication. The processes comprise the 200-odd operations involved in creating a BJT integrated circuit from a bare silicon wafer. Several hypotheses of the electrical failure would be gleaned from literature review and subsequently tested. Various processing conditions such as time, temperature and ambient gases would be explored and compared to the baseline (i.e. standard) performance. The main boundary condition of this study is that the integration scheme of the technology is maintained without changing the electrical or physical properties of the devices.

The objectives in this study are threefold. As 200-odd processing steps are involved in the fabrication of the BJT from a silicon substrate wafer, the first objective is to identify the process(es) which impact significantly the excess reverse leakage current (also referred to as excess leakage current, for short, in this thesis). Further from this, the second objective would be to determine the exact root cause, i.e. how the process(es) can contribute to the exhibition of the excess reverse leakage. Finally, the third objective is to eliminate, or significantly reduce, these electrical failures based on the knowledge of the previous two objectives. In such manner, the quality and reliability of the BJT devices would be improved.

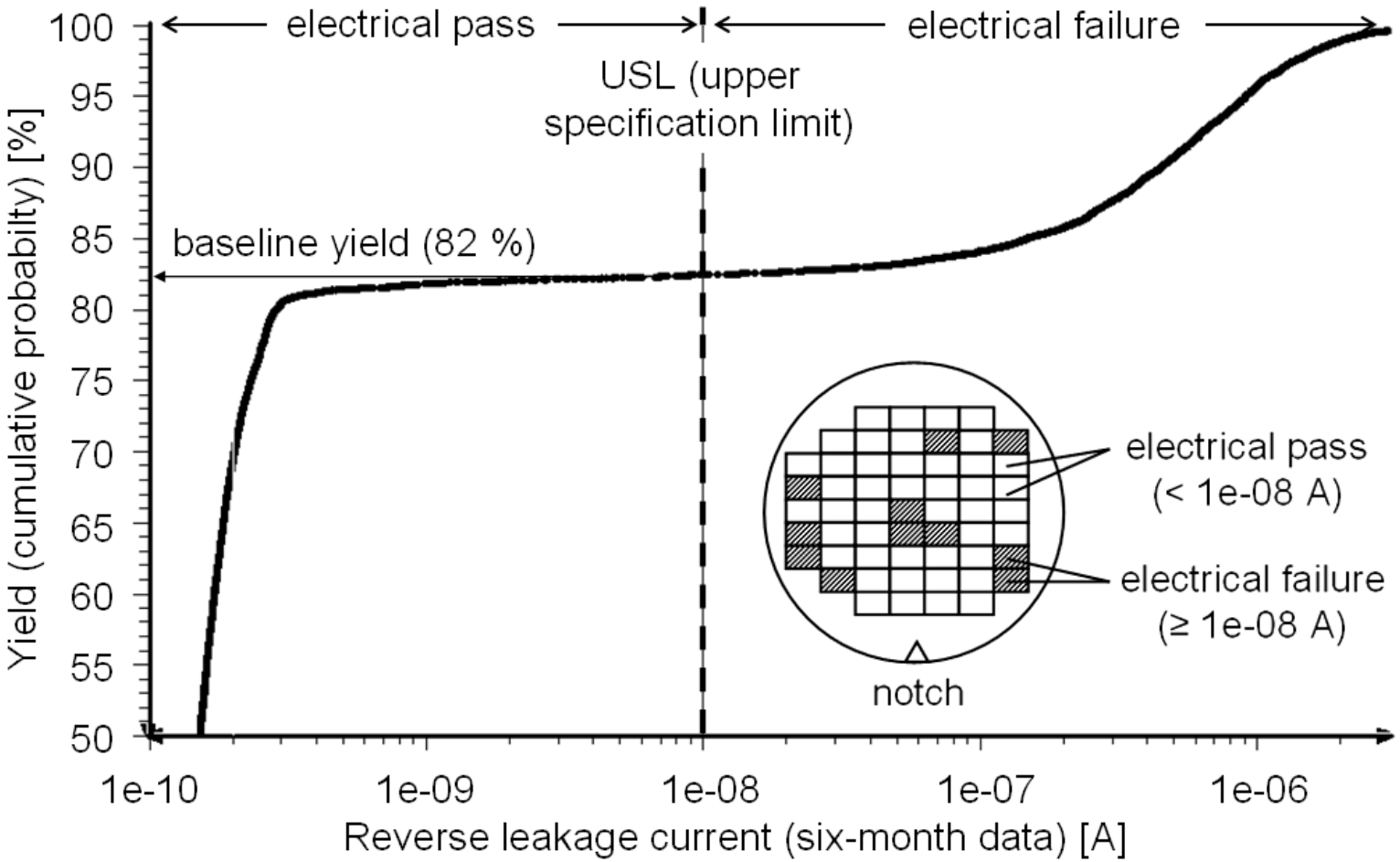


Fig. 1.1. Reverse leakage current collected from six-month production data at the start of the study (Infineon Technologies, unpublished). The baseline yield is 82 %. The yield is obtained from intersection of the curve with the USL (upper specification limit) line. Inset diagram shows an example of the test status of several process control structures on a wafer.

1.2 Action plan

This study can be divided into four main stages as shown in Fig. 1.2. In the initial phase of the study, two stages run concurrently i.e. identifying factors of leakage current as well as defect delineation. The former is performed based on knowledge from available literature with a focus on materials and processes involved in silicon device fabrication. Following these two stages, having obtained a concrete idea of the root cause of the excess leakage current, further experiments are then performed in the third stage to reduce the occurrence of the electrical failures. The fourth and final stage of the study would then reproduce the successful experiments from the previous stage – that is, those where the excess leakage current was significantly reduced – in order to confirm their efficacy.

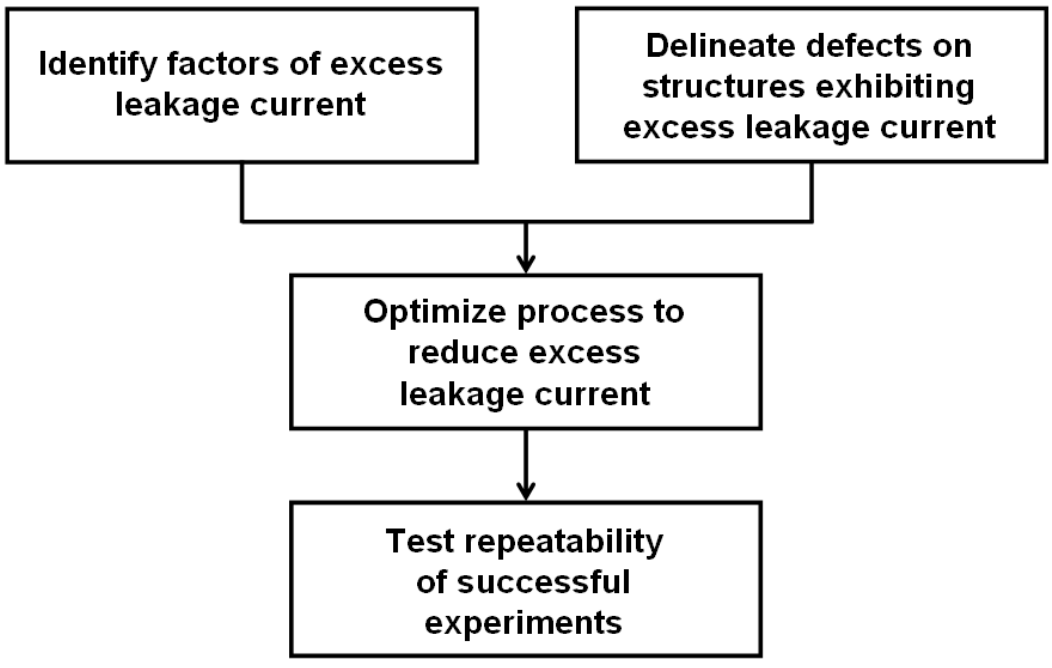


Fig. 1.2. Action plan showing the four main stages of study.

1.3 Thesis outline

This thesis consists of six chapters. Chapter 1 – Introduction has established the general background of this study. Chapter 2 – Literature Review will then present a survey of existing knowledge related to the study. The fundamental physics behind this study is detailed in Chapter 3 – Theory. Chapter 4 – Experimentation describes the materials, methods and machines used in investigating this topic. The results are then presented and discussed in Chapter 5 – Results and Discussion. Chapter 6 – Summary recapitulates the main findings in this study and concludes the thesis by recommending areas of future work.

CHAPTER 2

LITERATURE REVIEW

2.1 Excess reverse leakage current in silicon devices

Excess reverse leakage current can be root caused to either crystal defects or impurity contamination in silicon devices. It is also possible that both factors exist together in the form of impurity-decorated crystal defects. Crystal defects and impurity contamination would be discussed in the following sections, followed by sources of crystal defects and then sources of impurity contamination during device fabrication.

2.1.1 Crystal defects in silicon

In this study, “crystal defects” are defined as structural defects in the silicon lattice (Wolf & Tauber, 2000). Crystal defects can be classified according to their dimensions, namely zero-, one-, two- and three-dimensional defects. Zero-dimensional defects are commonly termed “point defects” or “atomic size defects”. The most common zero-dimensional defects are vacancies and interstitials. Interstitial sites can be occupied by atoms of the lattice itself, or impurity atoms. Interstitial atoms of the same type as the perfect lattice are termed “self-interstitials”. Alternatively, the impurity atom can displace and occupy the site previously occupied by a lattice atom. In this case, it is referred to as a “substitutional” atom (Föll, 2009).

One-dimensional defects or “line” defects include edge and screw dislocations. Also, dislocation loops fall in this category. Meanwhile, two-dimensional or “area” defects are for example, stacking faults and grain boundaries. Three-dimensional defects

include precipitation of impurity atoms such as oxygen or metal (Föll, 2009; Wolf & Tauber, 2000, p. 36). Fig. 2.1 illustrates various crystal defects in a simple cubic lattice.

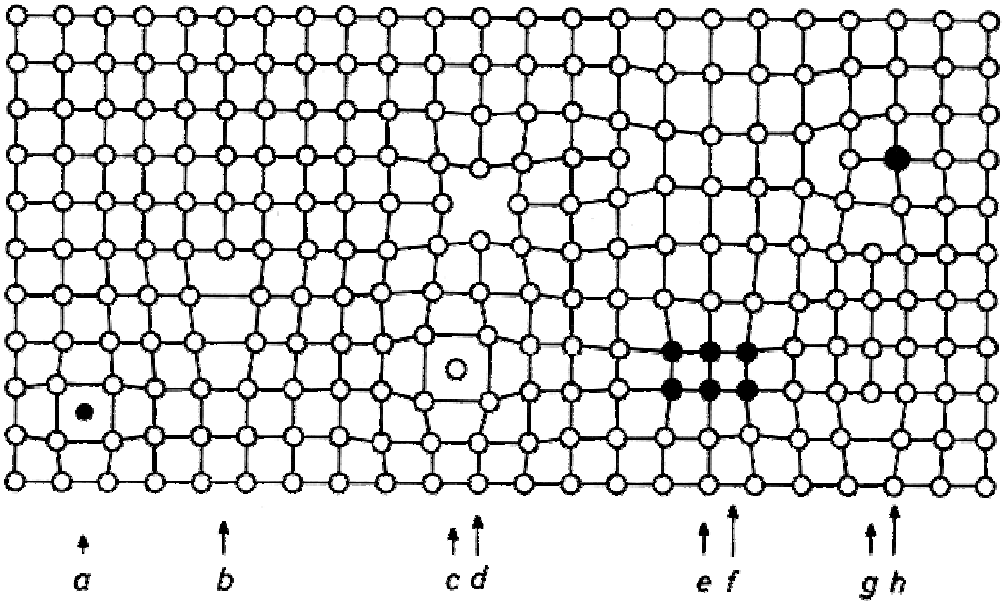


Fig. 2.1. Illustration of crystal defects, namely (a) interstitial impurity atom, (b) edge dislocation, (c) self-interstitial atom, (d) vacancy, (e) precipitate of impurity atoms, (f) vacancy type dislocation loop, (g) interstitial type dislocation loop and (h) substitutional impurity atom (Föll, 2009).

Some crystal defects have been directly reported to cause excess reverse leakage current. How crystal defects contribute to the exhibition of excess leakage current will be discussed in Section 3.3. The reported crystal defects as root causes of excess leakage current are hillocks (Umezawa et al., 2006) and oxidation-induced stacking faults (Ohring, 1998). Several works reported crystal defects beneath the device surface. However in such cases, the defect is not uncovered to reveal the exact their physical properties (Barletta & Currò, 2005; Gerardin et al., 2004; Kumaresan et al., 2009).

The type and severity of crystal defects is dependent on the dimensions and type of the device being fabricated. Also, processing conditions and processing history are contributing factors.

2.1.2 Impurity contamination

Another contributing factor to excess reverse leakage current is impurity contamination. The most common undesired impurities present in silicon is oxygen and metallic ions. This is because both oxygen and metallic ions diffuse very quickly in silicon. As an example, copper (Cu) ions diffuse ~ 600 μm per minute at a temperature of 900°C while iron (Fe) ions diffuse ~ 100 μm per minute at 1000°C (Wolf & Tauber, 2000).

For this reason, metallic impurities are widely reported for silicon devices (Schulze & Kolbesen, 1998; Sugiura, 1998). A study found that wet etching, lithography and heat treatment were main sources of metallic contamination during silicon device fabrication (Peykov et al., 1993). Metallic contamination usually exists together with crystal defects. This is because metallic ions attach easily to the crystal defect. In this manner the metallic ions are said to “decorate” the defect.

We now focus on the decoration of defects by metallic ions. Each atom at the edge of a dislocation consists of an unfulfilled dangling bond. The dangling bonds can trap impurity atoms which diffuse through the lattice. Impurity atoms also tend to reside at existing defects as less energy would be required to the displace the already defected area (Wolf & Tauber, 2000).

Although metallic ions are usually contained in crystal defects, their presence is hard to detect by direct measurement. This is because the metallic ions exist in trace

amounts. This lies beyond the detection capability of the EDX (energy dispersive X-ray) tool (Resnik et al., 1991).

As such, the presence of metallic ions is usually deduced by indirect methods. One such method will be described. In a reported work, the I-V characteristics of a diode are measured. Then the diode undergoes a gettering (i.e. mechanical vibrations) process, and its I-V characteristics are measured again. It was found that the diode's I-V characteristics approached ideal behaviour after gettering. Before gettering, the diode exhibited excess leakage current. It was thus deduced that the metallic contamination which caused the excess leakage current had been eliminated from the diode (Suguira, 1998).

2.2 Sources of crystal defects during device fabrication

The previous subsections introduced crystal defects and impurity contamination. This subsection will explore possible sources of crystal defects while the next subsection will explore possible sources of impurity contamination. Typical factors contributing to defect nucleation during device fabrication are furnace-induced thermal stress, implantation damage and surface damage from plasma etching. Also considered is the possibility of crystal-originated defects.

2.2.1 Furnace-induced thermal stress

Silicon device fabrication involves numerous steps where the wafer is exposed to high temperatures in a furnace in order for diffusion or oxidation to occur. Temperatures employed can be as high as 1200°C or more. A silicon wafer can tolerate high temperatures better at the early stages of processing. This ability declines rapidly with

increase of processing steps. This is due to increasing number of oxygen precipitates in the wafer which degrades the crystal strength (Rupp et al., 2004).

A common defect associated with thermal stress on the wafer by high temperatures, is slip dislocation. In the furnace, it is typical for a temperature gradient to exist between the edges and centre of the wafer based on how the wafer is held. As such, different regions of a wafer are forced to expand and contract at the same time, causing differing thermal stress on the wafer. This stress may force planes of atoms to move relative to each other and generate slip dislocations. The location of slip depends on the temperature gradient on the wafer. Slip dislocations tend to occur at the relatively hotter region of the wafer (MEMC, 2009; Rupp et al., 2004).

When inserting a wafer into the furnace, for example, the wafer edge would gain heat faster than its center regions. Therefore, slip occurs at the wafer edge. An alternative scenario could be the temperature is increased too fast inside the furnace. Fig. 2.2(a) illustrates this. Meanwhile, slip would occur at the wafer center if the wafer is removed too quickly from the furnace, or the temperature is reduced too rapidly in the furnace (Fig. 2.2(b)).

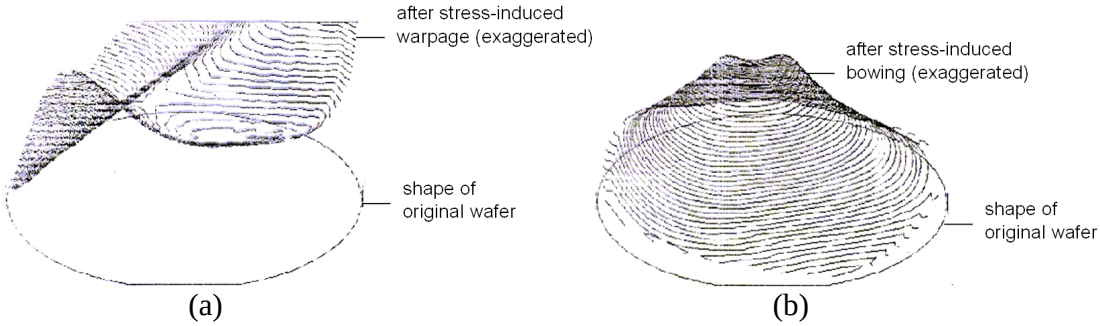


Fig. 2.2. (a) If the wafer edge heats up faster than the wafer center, slip dislocations are generated at the wafer edge. This warps the wafer into the shape of a saddle. (b) If the wafer cools faster at the edge than in the centre, slip dislocations are generated in the wafer center. This results in wafer bowing (adapted from MEMC, 2009).

2.2.2 Implantation damage

The ion implantation process is common in the industry as it allows precise doping control compared to its predecessor deposition and diffusion process (Rubin & Poate, 2003). An ion implanter tool is a high-voltage particle accelerator which produces a high-velocity beam of impurity ions, shown schematically in Fig. 2.3.

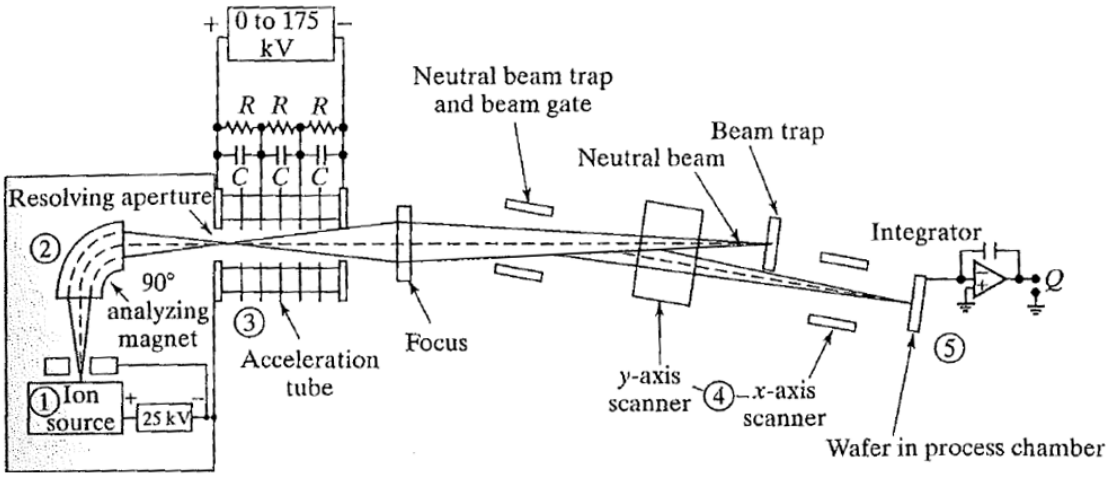


Fig. 2.3. Schematic drawing of a typical ion implanter showing (1) ion source, (2) mass spectrometer, (3) high-voltage accelerator column, (4) x- and y-axis deflection system and (5) target chamber (Jaeger, 2002).

Ion implantation involves bombarding dopant ions into the target material at high energy, thereby potentially causing damage to the target crystal lattice. Due to popularity of the ion implantation process, implantation damage is widely reported in the literature (Dai et al., 2001; Hua et al., 1998; Jones & Rozgonyi, 1993; Mica et al., 2002; Nicholas, 1977; Rahim et al., 2000).

It was known since the 1970s that using a protective layer of silicon dioxide on the target surface reduces implantation damage (Siedel et al., 1977). Such oxide is

commonly termed “scattering oxide”. The scattering oxide also functions to prevent channeling of dopant ions within the target material. Such channeling can occur when the dopant ion travels along planes with few number of atoms. The amorphous nature of oxide eliminates such channeling (Khanna, 2003).

2.2.3 Surface damage from plasma etching

Etching is the removal of material from the wafer surface, for example, to open a lithographic window on the wafer. There are two methods of etching. One is plasma etch and another is wet chemical etching (to be discussed in a later section). Plasma etching removes material from the wafer surface by bombarding the surface with plasma ions. The bombardment of ions of the wafer surface is similar to that during ion implantation and might incur the same damage, i.e. microroughness, of the wafer surface (Wolf & Tauber, 2000). The plasma etch process is additionally a possible source of particle contamination (Moriya et al., 2005).

2.2.4 Crystal-originated defects

This hypothesis considers the possibility that wafer substrates contain in themselves imperfectness that potentially serve as defect nucleation sites during processing. The most common defect related to the wafer substrate is the crystal-originated pit (COP). The COP can form on the wafer during single crystalline growth (Bullis, 2000). However, if the device is built on an epitaxial layer, the effect of COPs become then negligible. This is because during epitaxial layer growth, the COP reacts with hydrogen gases and loses its harmful effects (Borionetti et al., 2000; Bullis, 2000).

On the other hand, the method used to grow the single crystalline silicon can introduce a different concentration of oxygen impurities in the wafer. There are two methods of single crystalline growth. They are the float zone (FZ) and Czochralski (CZ) methods. CZ wafers typically have oxygen concentrations of 10^{18} atoms per cm^3. Meanwhile, FZ wafers have around two order of magnitudes lower oxygen concentration (Khanna, 2005).

2.3 Sources of impurity contamination during device fabrication

Factors contributing to impurity contamination are now explored. They can be generally categorized to come from cleaning operations and etching steps. Both of these would be explored in this final subchapter. In the discussions, contamination is used widely to mean unintended particles or ions residing in the silicon device as a result of the respective process.

Both particles and ions result in deleterious effects on the completed device. Particles left behind on the wafer surface might disrupt the stacking order of subsequently deposited layers – such as metal contacts or epitaxial layers – and nucleate into stacking faults. Meanwhile, unintended ions as discussed in a previous section potentially causes abnormal electrical behaviour.

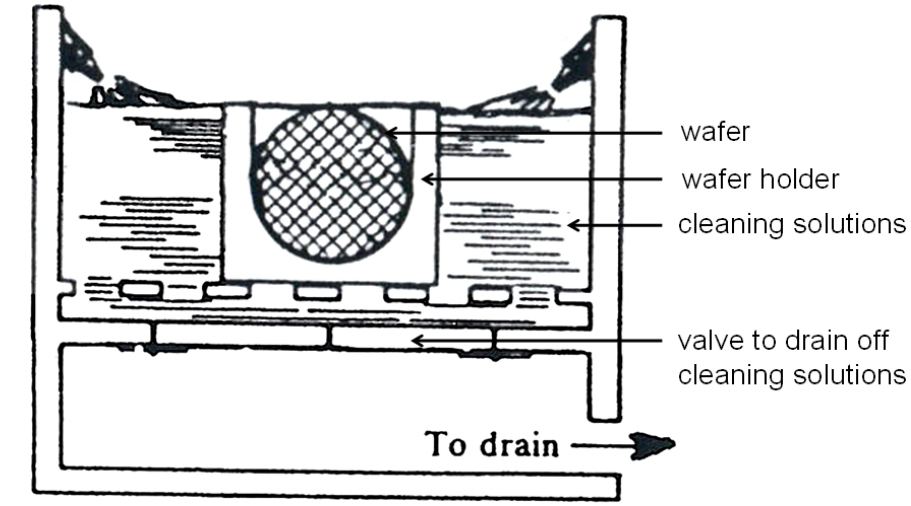
2.3.1 Particle residues from cleaning operations

Cleaning steps are essential in any fabrication process to remove particles or impurities from the wafer surface. This process involves drenching the wafer in carefully prepared cleaning solutions at an appropriate temperature for a certain duration of time. Even though cleaning steps are employed essentially to remove impurity contamination,

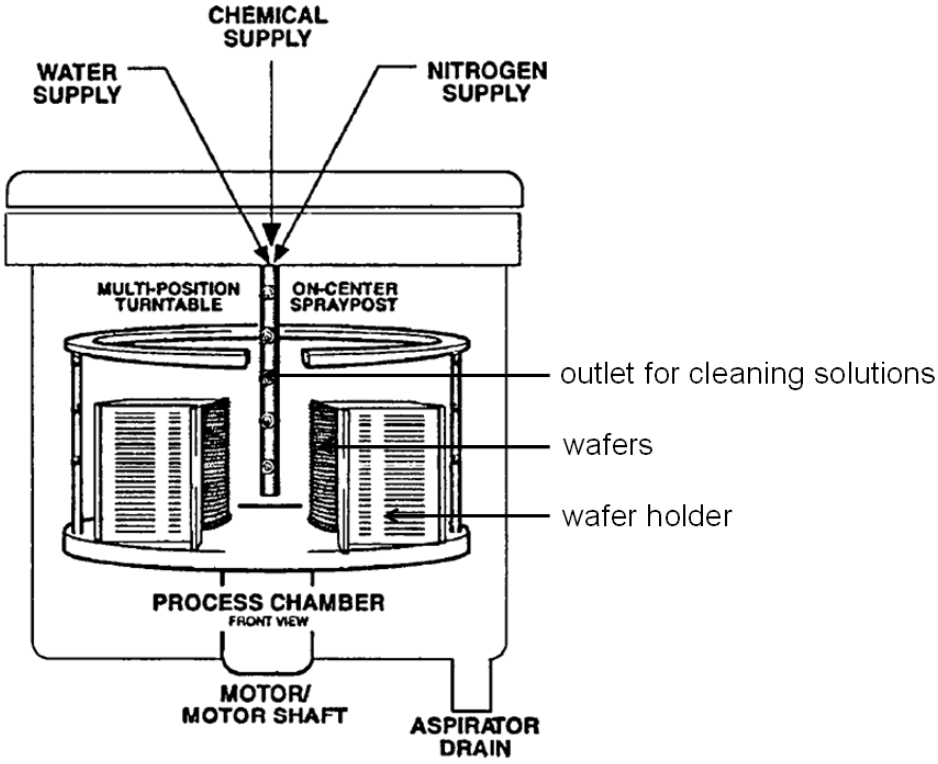
it is unavoidable that the cleaning solutions and tools themselves may generate their own sources of contamination. Cleaning usually employs the use of RCA solutions (see Jaeger, 2002). The quality of the solutions are vital, as any contamination from previous usage would degrade cleaning efficiency. This includes the importance of monitoring the use of the cleaning solution so that its recommended lifetime is not exceeded.

In the semiconductor industry, cleaning tools use either of two methods. The methods are chemical bath and spray cleaning. Fig. 2.4(a) shows a tool employing the chemical bath method. This tool immerses the wafer in a bath of cleaning solutions. The disadvantage of this tool is that the cleaning solutions are commonly re-used for several times. As such, particles or impurity materials left behind from a previous cleaning might lodge onto the wafer at the next cleaning (Wolf & Tauber, 2000).

Fig. 2.4(b) on the other hand shows a spray cleaning tool. For this method, a mist of cleaning solutions are sprayed onto the wafer. At the same time, the cleaning solutions are continuously drained off as fresh ones are sprayed into the chamber. Doing so eliminates the problem of solution contamination related to the chemical bath tool. However, the relatively fast moving parts of the spray cleaning tool are sources of particle contamination. For example, parts of the nozzles and seals can come apart and lodge themselves on the wafer surface. Besides this, watermarks are more common for spray cleaned wafers as its drying method is less efficient (Gale et al., 2008).



(a)



(b)

Fig. 2.4. (a) Illustration of a chemical bath cleaning tool (Wolf & Tauber, 2000). Wafers are immersed in a bath of cleaning solutions. (b) Illustration of a spray cleaning tool manufactured by FSI International (Gale et al., 2008). Mists of cleaning solutions are sprayed onto the wafers.

2.3.2 Particle residues from wet chemical etching

Wet etching is a cheaper, albeit less controllable, etching technique compared to plasma etching. Similar to the chemical bath method of cleaning, wet etching is performed by immersing the wafer in a bath of corrosive solutions. As such, there is a high risk of particle and impurity contamination from wet chemical etching as well (Doyle, *Etching Methods*, slide 3).

CHAPTER 3

THEORY

3.1 Carrier transport mechanisms

The carrier transport phenomena are the foundation for determining current-voltage characteristics of semiconductor devices. Two basic transport mechanisms in a semiconductor crystal are drift and diffusion. Drift is the movement of charge due to electric fields. Meanwhile, diffusion is the flow of charge due to density gradients. We shall assume that thermal equilibrium is maintained despite a net flow of electrons or holes. As such, we assume there is no carrier movement due to temperature gradient in the semiconductor (Neamen, 2003).

3.1.1 Drift

An electric field applied to a semiconductor produces a force on electrons and holes causing them to experience net acceleration and net movement. This net movement of charge due to an electric field is called drift, and the net drift of charge gives rise to a drift current. We consider a hole moving at average drift velocity u_{dp}, the drift current density due to holes is then:

$$J_{p,drift} = qpu_{dp} \tag{3.1}$$

where q is electronic charge and p is the concentration of holes. For low electric fields, the average drift velocity is directly proportional to the electric field *E*. Thus:

$$u_{dp} = m_p E \tag{3.2}$$

where m_p is a proportionality constant known as hole mobility.

Combining Equations (3.1) and (3.2), we get drift current density for holes:

$$J_{p,drift} = qp\mu_p E \,. \tag{3.3}$$

Similarly, we obtain the drift current density for electrons:

$$J_{n,drift} = qn\mu_n E \tag{3.4}$$

where n is concentration of electrons and μ_n is electron mobility. Summing Equations (3.3) and (3.4) beget the total drift current density (Neamen, 2003):

$$J_{drift} = q(p\mu_P + n\mu_n)E \,. \tag{3.5}$$

3.1.2 Diffusion

Diffusion is the process whereby particles flow from a region of high concentration toward a region of low concentration. The net diffusion of charge gives rise to a diffusion current. The derivation of the diffusion current is quite involved in mathematics and will not be reproduced here. For a one-dimensional case, diffusion current density for electrons is:

$$J_N = qD_N \frac{dn_p}{dx} \tag{3.6}$$

and the diffusion current density for holes is:

$$J_P = -qD_p \frac{dp_n}{dx} \tag{3.7}$$

where D_N and D_p are diffusivity constants for electrons and holes respectively (Neamen, 2003).

3.2 Ideal diode equation

We now derive the current-voltage characteristics of the ideal diode. Consider a *p*-*n* junction diode which is infinitely long in the x-direction, as illustrated in Fig. 3.1. A depletion or space-charge region exists in the intersection of the *p*- and *n*-doped regions. This depletion region has edges $-x_p$ and x_n in the *p*- and *n*-doped regions respectively. Electric field is assumed to be zero in the *p*- and *n*-doped regions. As such, drift effect is neglected and only the diffusion of minority carriers are considered (Neamen, 2003).

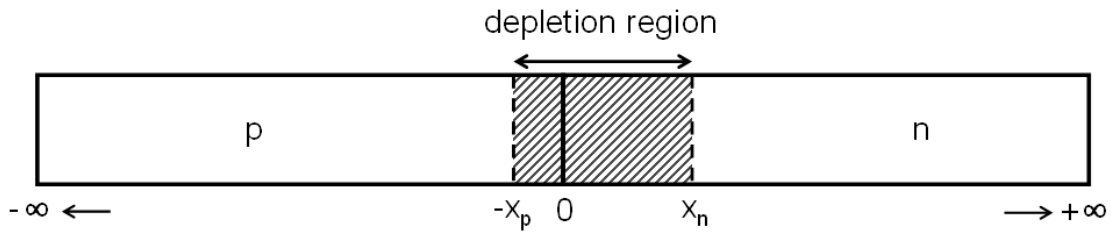


Fig. 3.1. Illustration of a *p*-*n* junction diode.

Minority carrier diffusion equations are derived from the continuity equations after making a series of assumptions for semiconductors under specific conditions. The minority carrier diffusion equations denote the rate of change in minority carrier concentrations with respect to time and space. In the *p*-doped region, the minority carriers are electrons and hence minority carrier diffusion equation in the *p*-doped region is (Torres et al., 2009):

$$\frac{dn_p}{dt} = D_N \frac{d^2 n_p}{dx^2} - \frac{n_p}{t_n} + G_L \tag{3.8}$$

where the left-hand side of Equation 3.8 represents the rate of change in electron concentration n_p. D_N denotes the electron diffusivity constant and t_n the mean recombination lifetime of the electrons.

On the other hand, holes are minority carriers in the *n*-doped region. Thus the minority carrier diffusion equation for the *n*-doped region is:

$$\frac{dp_n}{dt} = D_P \frac{d^2 p_n}{dx^2} - \frac{p_n}{t_n} + G_L \tag{3.9}$$

with the symbol meanings analogous for holes from Equation 3.8.

Two main assumptions here are made for the *p*-*n* junction diode (there are other assumptions not mentioned here for simplicity). The first assumption is that the diode is in the dark, meaning there is totally no contribution of carriers from external light sources.

$$G_L = 0 \tag{3.10}$$

Secondly, the *p*-*n* junction diode is assumed to operate in steady-state conditions. This means that minority carrier concentrations do not change with respect to time or space.

$$\frac{dn_p}{dt} = \frac{dp_n}{dt} = 0 \tag{3.11}$$

By substituting both Equations 3.10 and 3.11 into Equation 3.8, we get:

$$D_N \frac{d^2 n_p}{dx^2} - \frac{n_p}{t_n} = 0 \tag{3.12}$$

for the *p*-doped region. Substituting the same into Equation 3.9 begets, for the *n*-doped region:

$$D_p \frac{d^2 p_n}{dx^2} - \frac{p_n}{t_n} = 0\,. \tag{3.13}$$

From Equations 3.6 and 3.7, diffusion current density at the *p*-doped region is:

$$J_N = qD_N \frac{dn_p}{dx} = qD_N \frac{\frac{n_i^2}{N_A}\left[\exp\left(\frac{qV}{kT}\right)-1\right]}{L_N} \tag{3.14}$$

and for the *n*-doped region:

$$J_P = -qD_p \frac{dp_n}{dx} = qD_p \frac{\frac{n_i^2}{N_D}\left[\exp\left(\frac{qV}{kT}\right)-1\right]}{L_P} \tag{3.15}$$

where q is electronic charge, n_i is intrinsic charge concentration, and N_A and N_D are the numbers of acceptor and donor carriers respectively. k is the Boltzmann constant and L_N and L_p are the diffusion lengths of the electrons and holes respectively.

Hence, the current density in the depletion region is:

$$J = J_N(-x_p) + J_P(x_n) = q\left(\frac{D_N n_i^2}{L_N N_A} + \frac{D_P n_i^2}{L_p N_D}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right] \tag{3.16}$$

and multiplying this current density with the cross-sectional area of the diode A, we obtain the current through an ideal diode:

$$I = JA = qA\left(\frac{D_N n_i^2}{L_N N_A} + \frac{D_P n_i^2}{L_p N_D}\right)\left[\exp\left(\frac{qV}{kT}\right)-1\right] \tag{3.17}$$

Letting

$$I_R = qA\left(\frac{D_N n_i^2}{L_N N_A} + \frac{D_P n_i^2}{L_p N_D}\right), \tag{3.18}$$

we obtain

$$I = I_R\left[\exp\left(\frac{qV}{kT}\right)-1\right] \tag{3.19}$$

which is the ideal diode equation.

The significance of Equation 3.19 is that it highlights that current is dependant on temperature and voltage, since other values are constants. For an actual working diode, an ideality factor *n* is added to the equation (Ohring, 1998):

$$I = I_R\left[\exp\left(\frac{qV}{nkT}\right)-1\right]; \qquad 1 \le n \le 2 \tag{3.20}$$

A typical current-voltage (*I-V*) behaviour is sketched in Fig. 3.2. It can be seen that I_R represents the reverse saturation current of the working diode. A deviated behaviour from the ideal curve indicates excess reverse leakage, or leaky for short. This means that the diode is flowing excess current in the reverse bias mode before the breakdown voltage V_{BD} is achieved. There are several reasons a diode can be leaky, namely due to presence of crystal defects and/or unintended impurity ions (see Chapter 2).

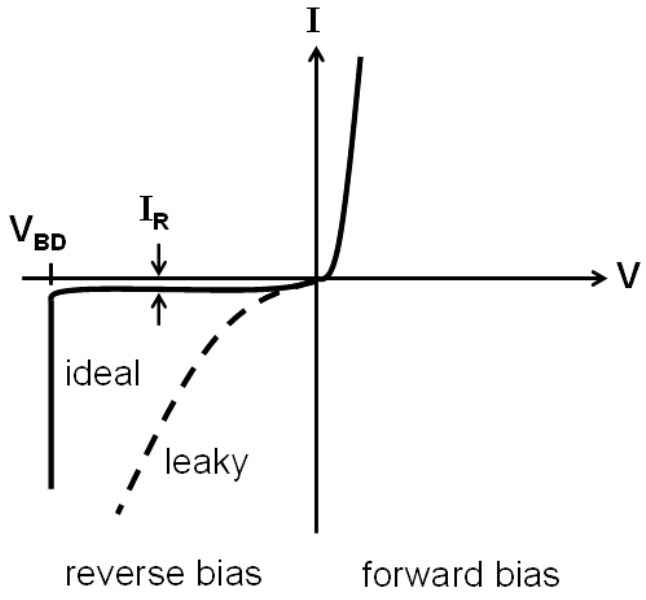


Fig. 3.2. Typical *I-V* curves of an ideal real diode and a leaky diode (adapted from Ohring, 1998).

3.3 Defect-assisted generation-recombination in diodes

In the real world, single crystalline silicon wafers contain many imperfections – crystal defects – in its lattice arrangement. If a crystal defect exists in the diode, it is highly likely that impurity ions are decorating the defected region. Thus the diode might exhibit excess reverse leakage current. The defect basically acts as a center for carrier generation and recombination, or recombination center, for short.

We consider a recombination center having a single energy level E_t, which can be either neutral or negatively charged. There are four possible steps for recombination to occur. They are electron capture, electron emission, hole capture and hole emission, Fig. 3.3. The diagram can be interpreted as follows.

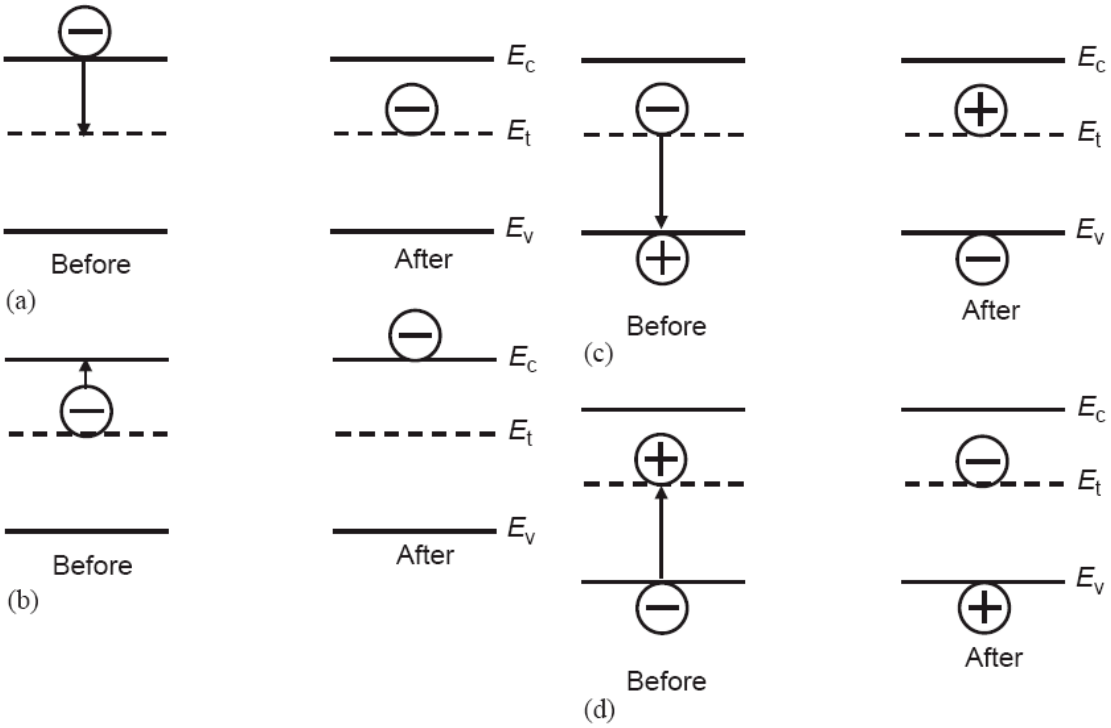


Fig. 3.3. Four possible steps of generation-recombination via a single defect energy level. (a) Electron capture, (b) electron emission, (c) hole capture, (d) hole emission (Khanna, 2005).

In an ideal (non-defected) semiconductor, an electron would need to gain an energy of at least equal to the semiconductor bandgap (1.12 eV for silicon) to excite from the valence band E_v to the conduction band E_c. However, with the presence of the intermediate center level E_t, it is now possible for the electron to excite from E_v to E_t (Fig. 3.3(d)) followed by E_c (Fig. 3.3(b)). It is obvious now that the excitation energy needed by the electron is much less than if the intermediate level was not present. A similar discussion holds for holes, correspondingly.

At steady-state conditions, the rate of recombination is (Khanna, 2005):

$$-U = s n_{th} N_t \frac{\left(pn - n_i^2\right)}{(n+p) + 2n_i \cosh\left[(E_t - E_i)/kT\right]} \tag{3.21}$$

where $s n_{th}$ is the constant of proportionality [with thermal velocity of carriers $n_{th} = \sqrt{\frac{3kT}{m}}$ (k: Boltzmann constant, T: temperature in Kelvin and m: mass of carrier) and the value of s determined from experiment], N_t is the recombination center concentration in the semiconductor, while p and n are free carrier concentrations, E_i the intrinsic energy level and n_i represents the intrinsic carrier concentration. At steady-state, the free carrier concentrations are:

$$n = n_i \exp\left(\frac{E_F - E_i}{kT}\right) \tag{3.22}$$

and

$$p = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \tag{3.23}$$

where E_F is the Fermi energy level.